Analog Electronic Circuits
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Lecture - 57
The Two-Stage Opamp

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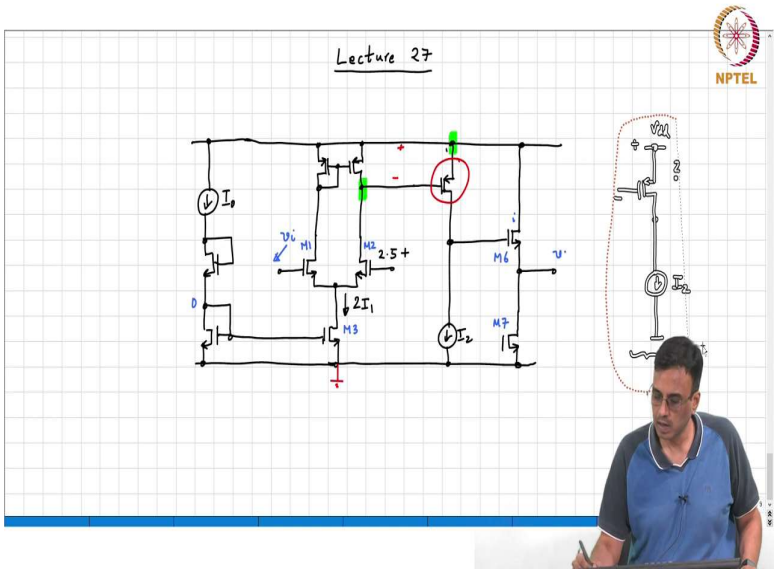

In the last class, we were at the tail end of the last class we were discussing. We were discussing this aspect which is what happens. I mean we earlier said that in a MOS transistor the drain current is the effect in these gate sources and the source gate voltage depending on. Whether it is a PMOS or NMOS transistor as the case may be the gate drive is the cause and the drain current is the effect, alright. And, so, what but here we seem to be pumping or pulling current out of the drain of this transistor right and expecting that.

This gate voltage developed to whatever you know given by the formula, right. The question is, you know clearly, we seem to be contradicting ourselves. So, where is the contradiction that is what I wanted you to think about yesterday. How do we know the voltage I mean? How does the differential pair know that this is exactly the voltage it needs to give is exactly enough to support I_2? Do you understand, do you see the question or I mean do you see the problem or you I mean is the problem obvious to you that we have a problem is clear. I hope that is clear, correct?

So, all along we have been saying that you know you cannot simply pull current out of the drain and expect voltage at this source gate to develop magically, right. So, what are we I mean, but here we seem to be doing exactly that which is evidently a contradiction of what we have been saying in the past. So, where do we resolve this? So, ok it is some current.

I understand we know how to get I_2, correct. I mean in other words what I am saying is that ok. So, if I asked you this question now, which is V_{dd} I_2 what is this voltage, what is the difference between this isolated circuit and this one. So, what is the; what is the source gate voltage here? I take a PMOS transistor to pull a current I_2 in the drain, what is the source gate voltage? This is the third time you are going through this.

Now, you are saying here it is magically when we put it in the circuit how can I suddenly start working? Alright. So, let us assume that this current changes by some infinite amount, right that I_2 was supposed to be I_2, but slightly you know less or more. Now, what comment can you make? How does this transistor know that the current being pulled out has increased by? So, therefore, what is the resolution of our seeming contradiction?

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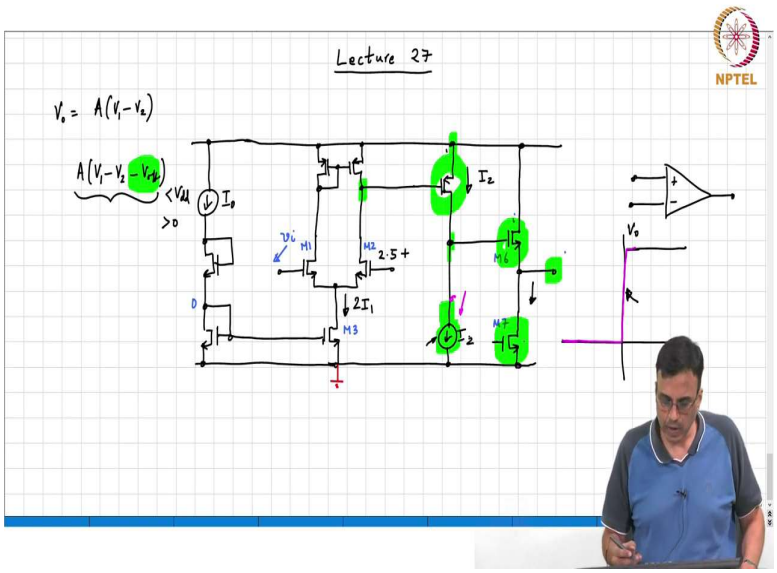

So, basically the resolution of this thing is that the op-amp is never meant to be operating in never meant to be operating in the op-amp is never meant to be operated without feedback. For example, let us say you know. Let us say you know if everything is perfect let us assume that somehow this voltage is developed, I mean is developed such that magically somehow this current equals I_2. Now, in reality you can never get exactly I_2 or even temperature, maybe

I_2 changes a little bit, right. If the amplifier is operating open loop this current remains I_2 this current has increased slightly. So, what comment can you make about the potential of that node?

It goes down pushing , eventually pushing this transistor into the triode region where the gain of the operational amplifier is very small, right? So, basically the open loop characteristic if you plot the differential input voltage V_d right as a and plot the output voltage V_o ok. There will be a positive saturation limit, right that is when this node voltage goes up. The highest this can go in this particular case is what is the highest ever that voltage can go to? What is the highest potential that that gate can go to? Approximately V_{dd} - of which transistor?

Student: M6.

Where is M6 man? Yeah, the gate of M6. What is the highest it can go to?

Student: ΔV.

So, alright. So, the highest this can ever go to is I mean it is a V_{dd} minus the drop across that transistor. And if you want to make it very approximate the highest this can ever go to is V_{dd},. So, what is the highest this can go to? V_d -V_d -something I mean. So, you know a good approximation is basically just say I mean V_{dd} -V_d is good enough right ok. So, and what is the lowest this voltage can go to? Ok, if this node has to go low, what must happen here?

Student: This should be in triode.

This should be in triode. So, this voltage will be very small. So, what will happen to M6 therefore? If the gate of M6 is close to ground what will happen to M6? It will go into cut off. If this goes into cut off what region of operation will M7 operate in the linear region. So, what will this voltage be? What is the current flowing through M7 therefore? If M6 is gone to cut off what will M7 do? What is the current in M6?

Student: 0.

What is the current in M7 therefore?

Student: 0.

And what is the gate source voltage of M7? Where is M7's gate coming from?

Student: From some mirror.

So, what region is M7 operating in?

Student: Linear.

So, what will be the voltage across the drain source?

Student: 0.

So, what will be the minimum voltage?

Student: 0.

So, the voltage the output will look like something like this when V_d you know about approximately 0 we will have a huge gain and then it goes that right. When V_d is infinitesimally greater than 0 then what happens the input differential pair steers more current ones one way and less current the other and this is what happens, correct.

If more current flows here and less current flows here which is what will happen when Vi is slightly positive, then what happens? More current is flowing here less current is flowing here and therefore, this node voltage will attempt to go up and therefore, cut I_2 off. If I_2 gets cut off this voltage will go to if I_2 is off I mean if that transistor is off then I_2 is 0, so, what comment can you make about that node potential?

Student: 0.

if this is 0, then M6 is off. M6 is off and M7 will be in the triode region. And, the voltage will be 0. If V_i is infinitesimally negative then what happens? Less current is here, more current is there, less current is there what comment can you make about this node?

Student: Decreasing.

It will keep reducing, right and this transistor will be in the PMOS transistor will be in the gate voltage is following down. So, it is attempting to push more current. So, this node voltage will go up. Eventually pushing this transistor into the PMOS transistor into the triode region. So, this M6 will basically you know have a potential which is close to V_{DD} the gate. So, the output voltage will go to V_{DD} - V_T, is this clear? So, and in the middle, I mean finally, the voltage therefore, infinitesimally small negative you know V_{DD} was V_I was 0 for

infinitesimally positive stuff it is V_{DD} -V_T in the middle it must I mean it cannot go there and come this way no it has to go this way correct, ok.

So, you can see that if there is any small change somewhere this you know for example, two transistors are mismatched and so on basically this curve will shift to the left or the right, ok. So, when you apply, I mean you should never take a high gain op amp you know. Even though the equation says the output is A times V_1 -V_2 where A tends to infinity right you should go and put $V_1 = V_2$ V therefore, it is 0. V_1 -V_2 = 0 and therefore, the output must be 0 ok.

That is not correct because in reality what happens is that the output V o is some A times V_1 -V_2, right and this is only true in the in that in this region, alright. In reality what it will be is even in that region it will be of the form V_1 -V_2 -some offset because non idealities inside the op amp most of the time this is because of mismatch in thresholds and so on, right. And, this is only true you know provided this quantity is less than V_{DD} and greater than 0. So, in other words, the output of the op amp can be modelled as a straight line only over an extremely small window of input voltages right, ok and why extremely small that is because the gain of the op amp is very very large, alright.

I mean if you have a million as the gain and if V_1 -V_2 is 1 milli volt, the expression is telling you that the output is going to be 1000 volts, but you would be completely mistaken. If you go and put 1 millivolt and expect to see 1000 volts at the output of the op amp, right. It will saturate to V_{DD} or ground depending on the polarity. And, even if you put $V_1 = V_2$ =0, V_1 -V_2 = 0, you still have this unknown offset term which will drive the op-amp either into positive saturation or negative saturation if you operate it open loop, ok.

If you actually were paying attention, you would have noticed that if you just know just power ON an op-amp. And it seems like the output should be and even if you connect the two inputs short the two inputs together and connect them to a potential some potential you will have found that the output is either + or - V_{DD} ok. So, then we went and calculated the gate source voltage of this transistor using the formula. The assumption is that what is the assumption?

The no the assumption is that all transistors are operating in saturation which is only possible when the differential input is very small which can only be ensured by a negative feedback, alright. So, let me take an example which is then the inverting input of the op-amp on the left

side. So, let us say we put 2 and half volts here which is $V_{DD}/2$ and then we close the loop as a voltage follower, correct. Now, let us say I mean there is you know we yesterday we went and calculated the quiescent voltage here. It is 2.5 + 1.2 = 3.7 volts ok, alright. Now, let us say I deliberately suddenly increase this current by? By small amounts.

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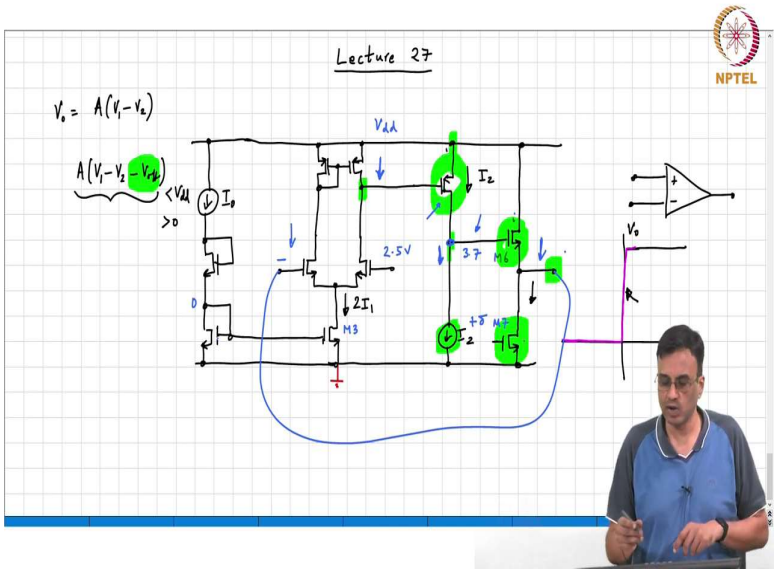

So, what will happen to this potential? What will it tend to fall down or go up?

Student: Fall down.

So, it will tend to fall down if this falls down. What comment can you make about that voltage? If the input that stage the second the third stage is basically a common. It will tend to fall. If this tends to fall this is the same node so that falls. If that falls, what comment can you make about that guy falling down or going up?

Student: Falls down

Falls down, alright. Alright if that node falls down what is happening to the source gate voltage of that transistor?

Student: It is increasing.

Increasing the current so as to keep this node potential from fall, alright. So, there is indeed negative feedback. It is now I mean only and, but there is negative feedback only when you

close the loop when the op amp is enclosed inside a negative feedback. You understand? ok and this is a subtle thing that you know a lot of textbooks do not even bother to talk about, right and you know they will do the analysis just like we did. You know this is unsaturation of all these voltages, that is perfectly all correct provided the op amp is sitting inside a negative feedback, alright. So, alright. So, that is what completes our discussion on the DC properties of op amps.