Analog Electronic Circuits
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Lecture - 56
Swing Limits of the Two-Stage OTA

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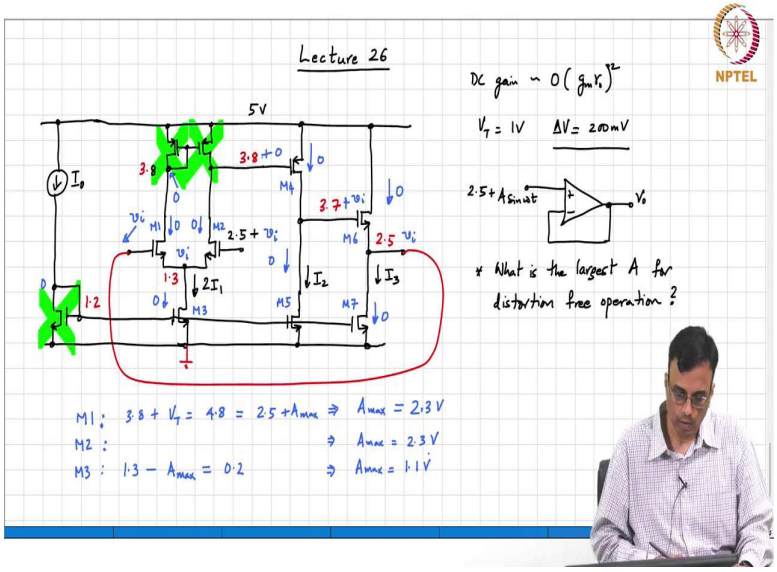

So, now you know which transistors do we need to worry about swing at all swing limits? Which of these transistors do we need to worry about? Ok. Let us start from the left with this guy. Well, the incremental voltage is 0 the incremental current is also 0. So, it does not change at all. So, that we are fine with. What about this chap here? We need to worry about it or not. Why? Why is there no incremental voltage across a transistor?

Student: No incremental current.

So, what? What about V_{DS}? Is the V_{DS} constant or is it changing? I mean you can safely ignore only if the incremental V_{DS} is 0 and the incremental. V_{GS} is 0 which is equivalent to saying incremental current is 0. So, then we need to worry about that character. What about M1 do we need to worry about or not? We need to worry about it because the gate is jumping up and down whereas the drain is at a constant potential right. So, we need to worry about the transistor getting into the triode region ok. So, M1 we have to worry about what about M2?

M2 also we have to worry about. What about the PMOS loads, what about the one on the left? The diode connected to the PMOS load. Why?

Student: Drain voltage.

The source drain voltage is not varying at all right, but what about the incremental current? Is there a possibility that the transistor goes into a cut -off? Is everybody clear that this transistor is not of concern at all? What about the other transistor on the right? The incremental voltage of the drain is 0. So, basically V_{DS} is not changing incremental current is 0 current is not changing therefore, this we do not worry about this as first swing limits are concerned right ok what about the next transistor this guy?

Student: Drain is swinging.

The drain is swinging. So, we basically need to worry about that chap. What about the tail current? The current I_2, current in source transistor I_2? See as we need to worry about it, what about the output stage?

Student: (Refer Time: 03:01) constant source (Refer Time: 03:02).

So, the drain source voltage is changing or the gate drain voltage is changing. What about the I_3 transistor? Change. What about the currents through any of these transistors?

Student: At the back sides.

What comment can we make about the current through any of these transistors as a V_I is changing? So, this incremental current is 0 anyway M2s incremental current is also 0, the tail currents incremental current, is this incremental current is 0, this incremental current is 0, this incremental current is 0. What about this incremental current?

Student: 0.

This incremental current?

Student: 0.

This incremental current?

Student: 0.

This incremental current?

Student: 0.

So, what does this mean? The currents are not changing in any of the transistors in this particular circuit. So, what does that mean? So, we do not have to worry about this?

Student: Cut off.

The cut off limit at all for any of the transistors right. So, your job becomes easier by a factor of 2 alright. Now there is no magic to it I mean of course, if you can look at the circuit and figure out which is the problematic transistor, I mean you know good for you right otherwise we go simply go transistor by transistor and figure out what the limits are ok alright.

So, let us start with M1 first. Let me label the devices M2, M3, M4, M5, M6, M7. So, M1 what is the triode limit? How high can the gate go before M1 goes into the triode region? What is the drain potential? Drain potential.

Student: 3.8.

So, what is the highest voltage that the gate of M1 can go before M1 goes into the triode region?

Student: 4.8.

It is basically 3.8 + 1, which is 4.8 right which is nothing but V_I which is 2.5 + A_{max}, which means that A_{max} is as far as M1 is concerned A_{max} is 2.3 volts. What about M2? Well, M2 is the same A_{max} is 2.3 volts. What happens in M3 is when A is positive or when in the positive half of the input cycle or the negative half of the input cycle? When the input goes down. This common source node also goes down and therefore, you are in the danger of M3 going into the triode region. Is that clear? So, what is the lowest that ah. So, the voltage this is the lowest voltage at the drain of M3 is nothing but 1.3 - A_{max} which must be equal to?

Student: 1.1.

And what is the smallest voltage that you can have between the drain and the source? This is the overdrive voltage which is 0.2 volts which means A_{max} is 1.1 volt.

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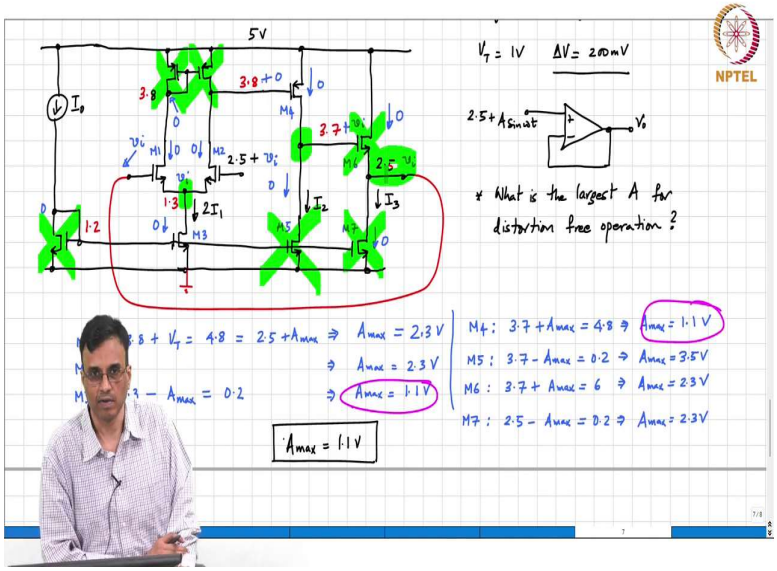

1 volt. What about M4? What is the highest the drain can go to? So, that is 3.7 + A_{max} must be equal to?

Student: 4.8.

Which implies A_{max} = 1.1 volt. What about M5? What is the lowest voltage that the drain of M5 can go to? That is basically 3.7 - A_{max} must be equal to 0.2 volts which basically means that is 3.5 volts. So, is M6 in trouble? In the positive half of the input cycle or the negative half of the input cycle?

Student: Positive.

When A is positive the gate is going up whereas the drain is sitting at the same potential. So, the transistor is going closer towards the Triode region. So, for M6 it is 3.7 + A_{max}. What is the highest it can go to? What is the highest the gate of M6 can go to before the transistor gets into the triode region? The drain potential is at 5 volts. How high can the gate go? Yeah. So, that is 6 volts which means that A_{max} is 2.3 volts. Alright. What about M7? 2.5 -A_{max} is the lowest that the drain potential can be?

Student: 0.

This must be equal to 0. So, A_{max} is nothing but?

Student: 2.3 V.

2.3 volts alright. So, which of these things do you think is the most problematic? So, you basically say that the two transistors M3 and M4 basically go into the triode region at exactly the same point in this particular circuit and therefore, A max is the minimum of all these voltages and that is basically 1.1 volt. As you can see there is no rocket science here, this is the same thing that we have been doing for all the single transistor circuits: first job, find the operating point, then replace all transistors by their incremental equivalents and do the small signal analysis. Once you do the small signal analysis you find you can find the incremental voltages.

Everywhere and the incremental currents in every transistor and then you know the quiescent value you know the incremental value. So, you can find the total current in every device and the total voltage in the total gate source voltage in. So, total gate source voltage is total drain source voltage everywhere. With that you can go and find the swing limits for each transistor right and therefore, you can find the swing limits for the entire circuit.

With a little more experience I mean you know I mean if we did not kind of here we were already able to see that three of the transistors do not contribute at all right and for the other transistors which can potentially mess you up we saw that the cut off limit need not be checked in this particular circuit right.

So, if you stare at it you know I mean more pieces of information will fall out. For example, we are only interested in the transistor going into the triode region. One thing you can notice is that the voltage at the drain of M3 is $1.3 + v_i$ the other one here is nothing but $2.5 + v_i$ correct. So, which do you think is deeper in trouble? So, then does it even make sense to consider M7?

Yeah. So, basically you know before M7 goes into trouble. You can know that you are already finished right. So, there is no point in considering M7 right. So, therefore, you know you are now reducing your job to you know finding the stuff for you know 1, 2, 3, 4, 5 transistors now what about M5? Yeah. Well, if M7 is not in trouble then m5 is definitely not in trouble right. So, you can remove that guy also ok. So, just like I said in your lab experiment where 10 guys are sitting around doing one experiment right is only follows doing work or one or two chaps right all the other guys is just there you know what do you

call to bring tea and like you know tell you what you missed in Kapil Sharma comedy show the previous night you understand right.

So, you can see here that the only four transistors that cause potential problems are M1, M2, M3, M4 and M6. In fact, M6 can also be eliminated. Why do you think so? What is the voltage across the drain source voltage of M6? The drain is at 5 volts, the source is at $2.5 + v_i$. So, it is $2.5 - v_i$, right. So, if, but you know. So, M3 or M6 which one is the drain source voltage of M3 is $1.3 + v_i$, the drain source voltage of M6 is $2.5 + v_i$ which one is going to be in trouble first?

Student: M3.

So, there is no point in even considering M6. So, with a little bit of experience you will be able to just simply throw away the majority of the transistors and only look for you know a small subset of transistors is basically what is going to limit your speed you understand alright. But you know if you do not practice enough and basically you know you are stuck in an exam the sure short way in which to do the problem is to make one observation. I would like to make it that nothing here is arbitrary right there is a reason why.

You know every transistor is there is a reason why every transistor is sized a certain way there is a reason why you know every transistor is chosen to be the type it is ok alright. I mean you know just like you know if you buy a car and you open up the hood right this is every there is a reason for in every part that is there.

The automobile manufacturer is not trying to confuse you by putting like you know four boxes there which do not do anything correct ok. Same thing with circuits alright and I do not know if some of you are exposed to the 741 op amp. How many of you have seen that in your undergrad at all? If you have seen it ok.

So, alright and that circuit looks you know as you can as you will probably agree looks a lot more complicated than this one right. We will eventually get there, but for starters this is a good starting point and this is a very commonly used circuit for CMOS op amps and the only thing that is left to be solved is that as we discussed one of the problems with having you know multiple stages is that, it turns out you know as you can imagine that nothing in the world is instantaneous correct.

So, it is not that you know one problem with our model for the MOSFET is that we assume that you apply V_{GS} immediately drain current will flow right it turns out I mean without any going into you know any detailed physics I mean somebody told you that you know you apply voltage and instantaneously current starts flowing you will say a nice try correct ok.

So, there is always every stage every transistor is associated with the delay right in vague terms ok now to get gain what are we doing? So each amplifier stage has got some delay. When you cascade amplifiers you get more delay. I mean , why did you cascade amplifiers in the first place to get gain correct, but along with gain comes delay right if you want more gain. You get more delay and now if you attempt to close the if you have a negative feedback loop with a lot of delay in the loop alright. What can potentially happen?

Student: Output will reach infinite.

No, what infinite time, I am telling you there is only finite delay no. You have a feedback loop and there is a lot of delay. I mean for example; I mean you know in exam quizzes and you know you know course quizzes and you know mid semester exam and assignments etcetera are all basically for your feedback correct. So, what if I decided to kind of give you graded papers, I do not know what I mean two years later?

So, basically you do not know you know I mean hopefully you should, but I mean you know because if you do not get your marks, you do not know whether you understand the stuff or you do not correct. So, similarly I mean to say complaints right.

So, let us say you know something is not working for you in the department right. So, your first step would be to go and complain to your faculty advisor right then say nothing happens, then that is only one stage of gain correct then you go and complain to the head right that is two stages of gain right?

So, you complaint to the faculty of the advisor complaints to the head, now then nothing happens and then the head complaints to the director right that is three stages of gain and so, as you can see each stage takes time right ok alright and if that does not work you go complaint to the prime minister's office and that is like you know that you know the gain from there to here is like you know infinite right.

But the delay is so much delay alright that you know if you hope that the prime minister is going to solve every one of your problems I mean you know nothing is going to happen correctly. So, if you have a negative feedback loop with a if you have a feedback loop with a lot of delay what will happen?

Student: When the feedback will come the input will change.

Yeah. So, when the feedback has come, that is corresponding to the feedback is based on the input like you know three years ago alright. Now things have changed completely, but then the feedback says no you do this, but then you say well no I solved my problem three years ago then the feedback does not know that says no never mind you do it anyway right and then your error goes completely in the opposite direction right.

And so, it is basically going to be unstable, correct ok. I mean a simple thing that you know I am sure all of you have experienced this with online classes and stuff like that is what? So, well if the teacher has got speaker phone on and what do you call of course, his MIC is on and the student has got MIC on and speaker on then what do you see? You will see I mean you know if the system is marginally stable you will see somebody the teacher says hello and then you see hello right if the gain is too much you will see I mean the whole thing you will see if the whole system starts singing correct ok alright.

And the more the delay in the network, you will find that the frequency of oscillation is lower alright. The feedback loop is closed through base station Airtel . Maybe with zoom it is going to Europe and coming back and like you know the loop is closed that way, but there is a lot of delay in the whole process ok.

So, whenever you have a high gain negative feedback loop, you have to always worry about stability. Nothing comes for free, alright , ok. So, in this attempt to get more and more gain you pay you know the price you are paying is that you are picking up more and more delay and when you close the loop you get more and more you get this you end up with this potential for unstable alright. So, this basically you know is all I had to say about the DC properties of at two stages. This is a two stage operational amplifier right and I mean you know if in many cases the gain may still not be sufficient can you simply tell me a simple or rather a straightforward way of increasing the gain by another factor of $g_m r_o$ without adding another cascaded stage the no either the M6 is there to give you low output resistance. So, that does not work. Why are we ok? Let me give you a hint: what is the gain of this stage?

Student: - g_m r.

- g_m r. So, I mean if you want to increase the gain you either increase g_m or you increase r_o right. How can you increase r_o?

Student: Cascode.

So, basically an improvement over this is basically to add a cascode here ok.

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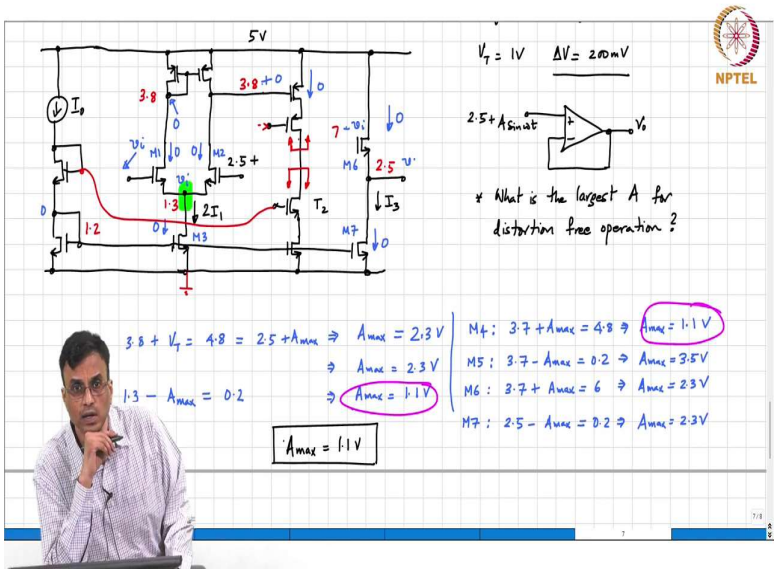

And you know one way of biasing this node is to simply do that correct. We have seen this in your class as well as in your tutorials right. So, this is a cascode. What is the output impedance looking in here? $g_m r_o^2$ alright. So, what comment can you make about the looking impedance up this way I mean let us assume that this bias appropriately. So, that all the transistors are in saturation, what is the output impedance looking up?

Student: $g_m r_o^2$.

So, if you look at the second stage what is the gain now? Incremental gain?

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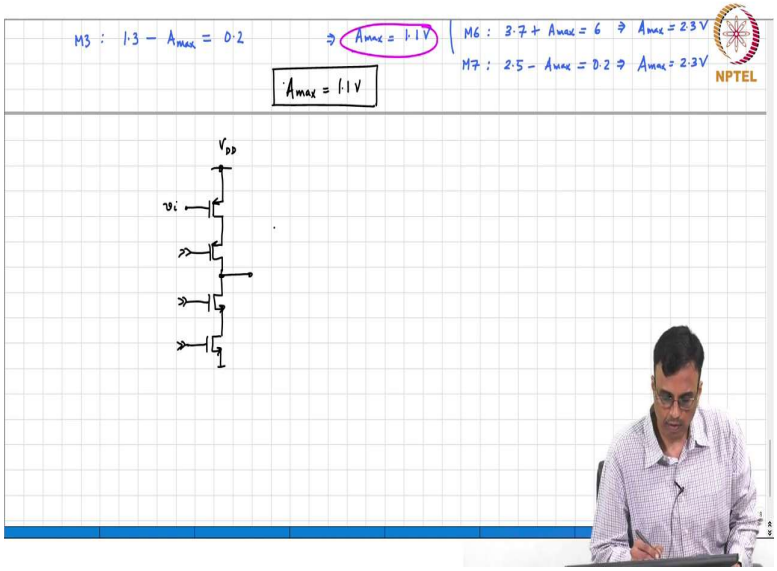

Let us take a look at the stage again, this is V_{DD}. This is appropriately biased, all these are bias voltages appropriately chosen that is what this means. So, the question is, what is the incremental gain? So, what do we do? We find the Norton equivalent correct.

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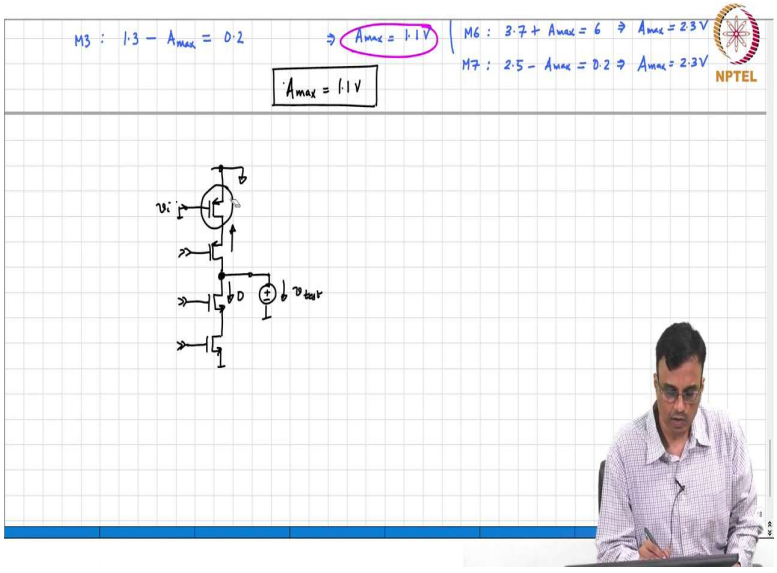

So, if we find the incremental equivalent this becomes ground to find the short circuit current, we connect v_i to incremental ground and measure the short circuit current. What is the short circuit current? This is v_i. What current is the incremental current flowing there?

Student: 0.

Why?

So, the V_{GS} of all these transistors is 0. So, basically this incremental current is 0 when we put v test here the incremental current here is 0 what comment can you make about the incremental current there? This is basically nothing but a common source amplifier feeding into a common. We discussed this in the context of a cascode before: what is that amplifier?

Did we discuss the cascode clearly? So, it is a common gate amplifier. So, what comment can you make about the incremental current here? That incremental current is g_m v_i g_m v_i. So, what is the incremental current here?

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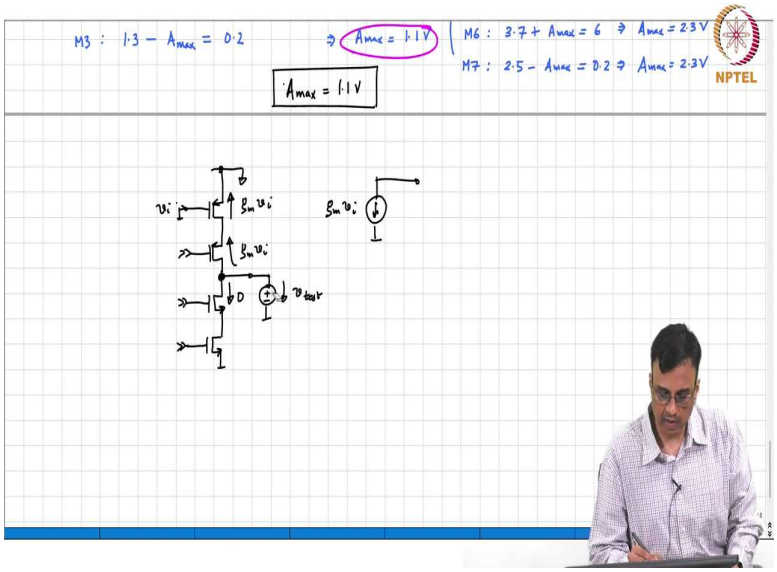

Student: Same g_m v_i.

So, what is the Norton short circuit current? So, this g_m v_i flowing in that direction alright. So, what is it? To find the Norton resistance what do we do? We basically ground this ok.

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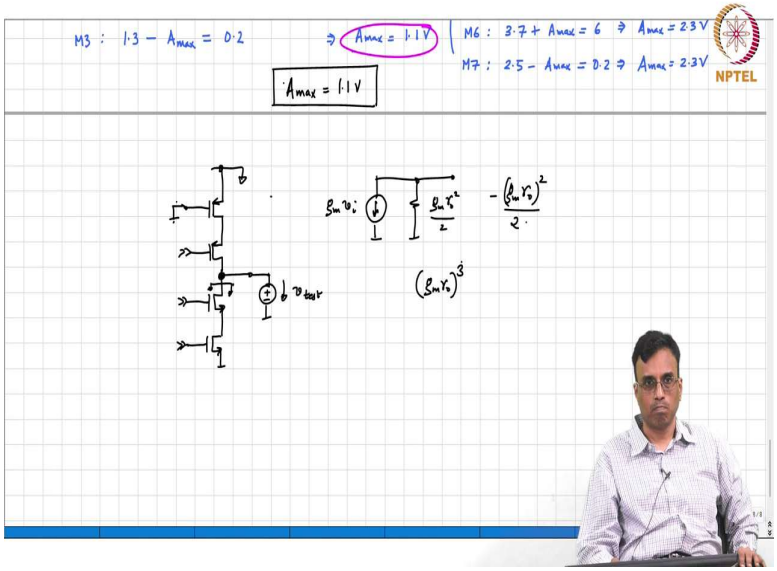

So, what is the output resistance? It is just the parallel combination of these two output resistances. Basically, it is roughly of the order of $g_m r_o^2/2$ assuming all the g_ms and r_os are the same. So, what is the gain that you get?

Student: $-g_m r_o^2/2$.

So, what is the gain of the total operational amplifier? So, basically you get something of the order of $g_m r_o^3$ right. So, if the gain of each stage is say if $g_m r_o$ is I do not know 30^3 is some 27000, ok our last piece of the last question before I conclude this stuff on op-amps.

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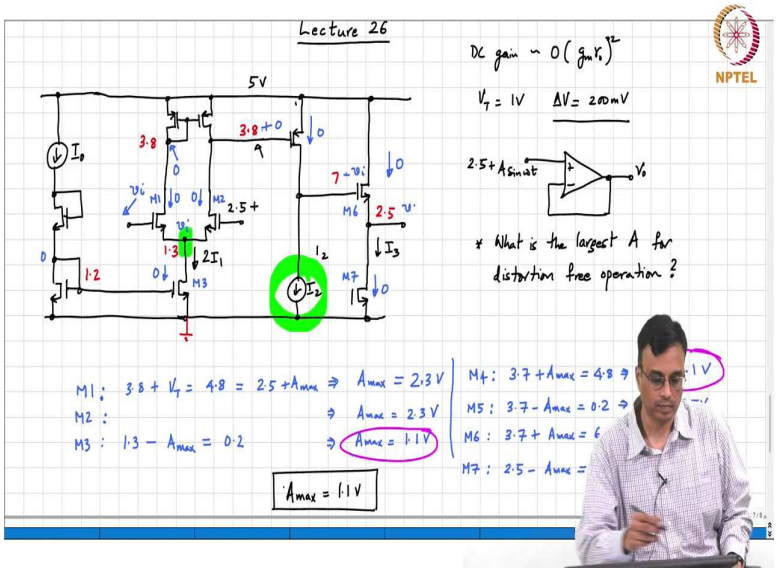

So, this lets me abstract it out as a current source I_2. So, we said the gate voltage here is simply nothing, but you know whatever source gate voltage is needed to support a drain current of I_2 right, but we also had this discussion where we said that you cannot force current into the drain of an op- into the drain of a transistor and expect the gate source voltage to develop, but that is exactly what we are doing?

Student: If the biasing is proper, what is the meaning of biasing is proper? Alright. Think about it we will talk about in the next class. Thank you.