Analog Electronic Circuits
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Lecture - 54
The Two-Stage Opamp (continued)

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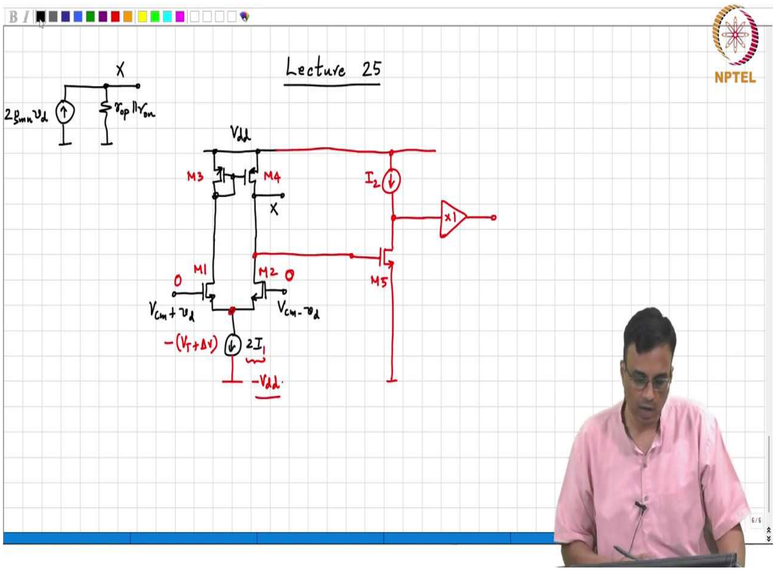

Alright. So, now, the next point is ok. So, this is our you know version 0 op-amp. Let us again assume that this is ground. We already know what to do when we have to operate this with a single supply. Now, the question is what are the signs of the op-amp?

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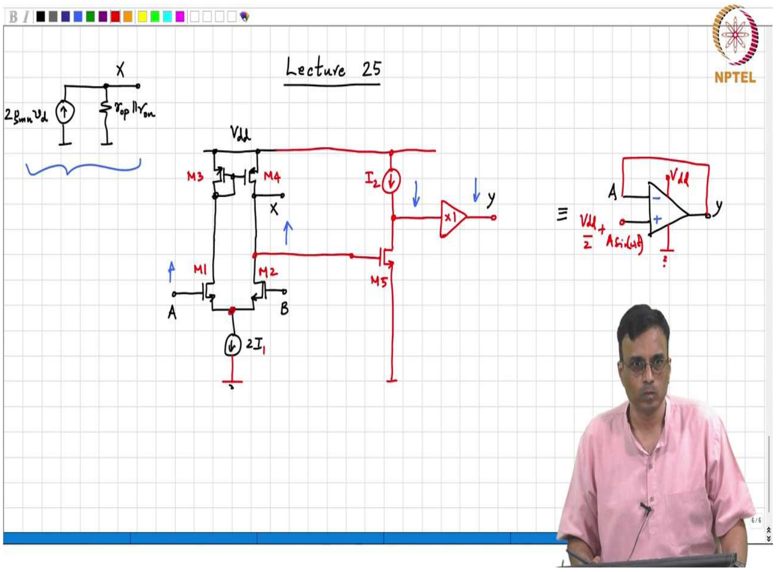

So, this we claim to be an op-amp, correct. So, let us call this terminal A, let us call this terminal B and let us call this terminal Y. So, is A the positive terminal of the op-amp, is it the non-inverting terminal or the inverting terminal? How will we figure it out? You yank A up, if that node A goes up, what comment can you make about node X?

Student: Goes up.

Ok, some fellow says goes up, some fellows says goes down. So, if node A goes up, node X?

Student: Goes up.

Goes up, if node X goes up, what comment can you make about the drain of M5?

Student: Goes down.

Goes down. So, if node if the drain of M5 goes down, what comment can you make about why?

Student: decrease.

Decrease. Alright, so, is A the inverting terminal or the non-inverting terminal?

Student: Inverting.

Inverting, alright. So, this is a, you know this box, I mean, you know, assuming that V_{dd} and ground are all ok. This is basically at, you know, claims to be an op-amp. So, these two terminals come in and one terminal comes out, correct ok. Now, how do we know that this is actually a good op-amp? How do we know that this is good enough? Alright, man. You guys go and order an iPhone from Amazon, ok. You will get some packet, ok.

You will open it, there it seems something like a phone? How do you know that it is not, I do not know, I mean, some imitation that the seller is trying to give off to you. How do you know it is not within code its toy iPhone, which looks like an iPhone, but it is not a cell phone. It could be Hamam soap with a cell phone pasted on it, huh? How will you know? What will you do? You will turn, you know, you will attempt to turn it on. If it turns on, it does not mean anything, right? It could just be some bunch of lights that they have put inside. It could not necessarily be a cell phone. What will you then do? You will try to make a phone call, you will try to download something, you know, you will try to install an app, right?

If everything works, right, I mean, if this box does everything an iPhone can do, ok, even if it is Hamam soap with a picture of an iPhone pasted on top of it, it is an iPhone. Isn't it? There is no way of knowing. I mean, you know, you are just taking it on faith, ok. Alright ok.

Same thing here this is a, I mean, you said I want an op-amp, you know, I have given you a triangle with two input terminals, one output terminal, right. How do you know it is an op-amp? It seems like, you know, he says, well, input impedance is infinite, output impedance seems 0. Good. I mean, here is my 10,000 rupees, give me the op amp, right. What will you do?

Student: Taste it.

I do not know, this guy is saying, taste it. No, no, that is not, huh? Not taste it, you must?

Student: Test it.

Test it, ok, alright. So, what will you do? You pay, you know, you put this op-amp in all possible circuits that you can think of, and if it does everything that it is supposed to do, then it is very likely an op-amp inside the box, right? The simple circuit you can think of as he points out is voltage follow, because you do not do anything, right. You just have to connect the output Y to the inverting terminal like this, ok. And then what will you do?

You apply V_I and then, you know, some voltage, ok. And what do you call, remember our discussion, this V_I must now be, because it is, our op amp is operating between V_{dd} and ground that V_I must be centred around $V_{dd}/2$. So, basically, we add $V_{dd}/2$ plus some sin wave, right. Some, I am going to call this some a sin, omega t, correct. I mean, is this logical or not?

Student: Yes sir.

Right. This is what you will do, correct. Alright. so, now what do we do, which is why we needed to figure out which was the inverting terminal and which was the non-inverting terminal. So, where will we put it, where will the output Y be connected?

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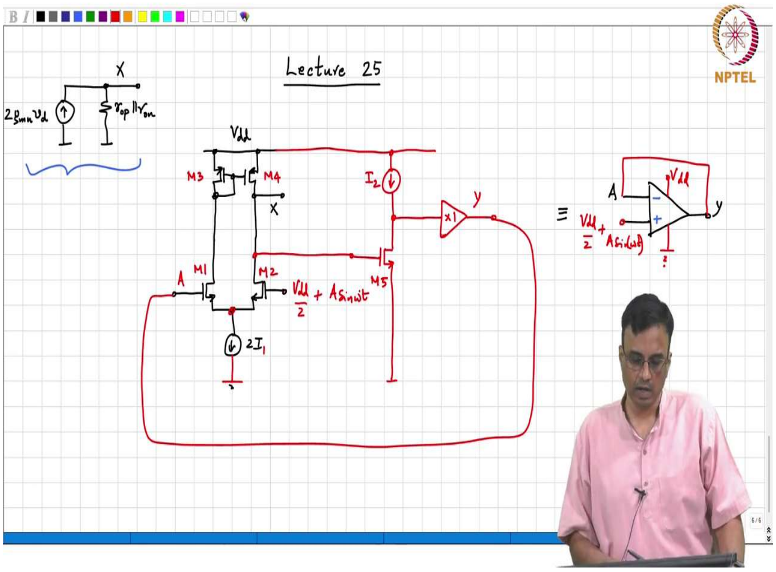

This was A. So, we will go and connect Y to A. Correct? Alright. Then what will be connected to the gate of M 2 $V_{dd}/2$ + A sin ωt. Alright. Ok. So, for argument sake.

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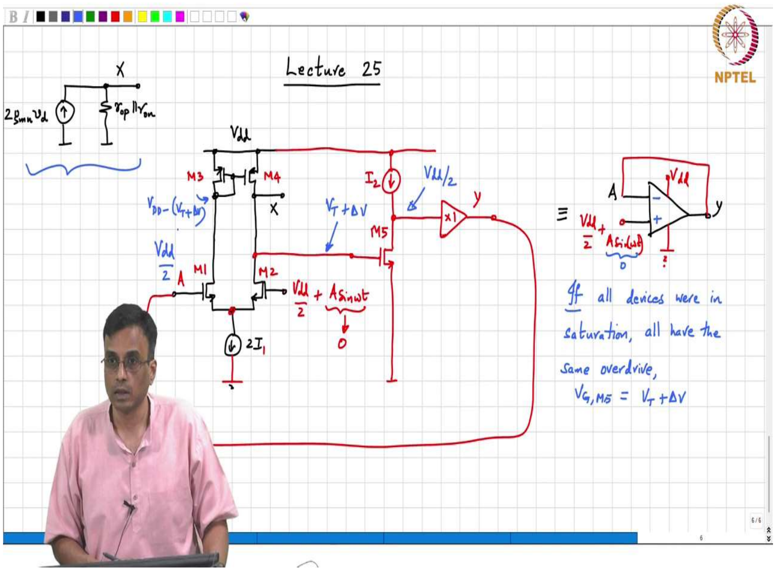

Let us assume that the overdrive of all transistors is the same, some ΔV. The first thing to do is the operating point, right. I mean, if this is, let us say A is 0. Then what comment can you make about this guy? This becomes 0. Alright. So, assuming the op-amp is working properly, right, what comment can you make about the potential of A? Let me mark all these voltages in some other color, blue. Ok. What is the potential, quiescent operating point? What is assuming the op- amp is working properly? If this is 0, what will be the old potential at A?

Student: $V_{dd}/2$.

Very good. If this is $V_{dd}/2$ and all the transistors are operating in saturation, what comment can you make about that potential? What is the current to the transistor M 5? It is I_2, we assume that all transistors have the same gate overdrive when operating in saturation and if the op amp is working as intended, correct. What comment can you make about all the transistors? All the transistors must be working in saturation.

So, if all devices were in saturation, what comment can you make about the gate of M 5? Have the same overdrive, V_G of M5 must be at what potential?

Student: $V_T + \Delta V$.

Alright. Ok. So, and what comment can you make about this character, that voltage?

Student: $V_{dd}/2$.

Why?

Student: Because the end is connected from VCVS.

Yeah. So, the output is $V_{dd}/2$. So, and that is a VCVS of gain 1. So, it means that the input must have been?

Student: $V_{dd}/2$.

$V_{dd}/2$. Alright. Ok. So, we have found the potential at all nodes. I mean, this node potential is nothing but V_{DD} -V_T -ΔV. Or V_T + ΔV. Correct? All node potentials are no. Now, we have to verify and see if these potentials were all found predicated on the fact that all transistors are operating in the op amp is working well, which means that all transistors are working in saturation, right and therefore, the gain of the op amp is close to infinity. That is what that is the assumption behind which we have found the potentials everywhere. Now, given that these are the potentials, we have to go and verify our assumptions namely all the transistors are in saturation. So let us go device by device M1. If it kind of helps you, maybe you can just take some numbers.

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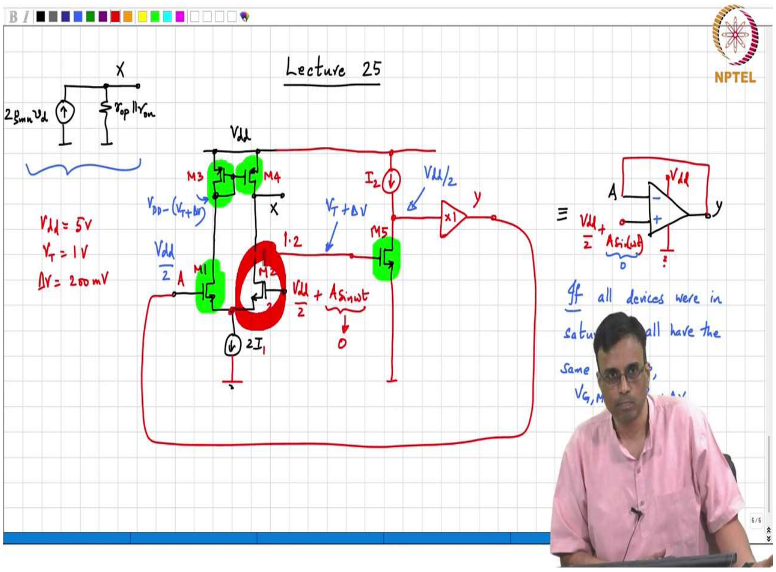

So, say V_{dd} is say 5 volts, V_T is say 1 volt and ΔV is say 200 millivolts ok. Whether its NMOS or PMOS, V_T is 1 volt. Let us assume ok. Now, M1 gate is at 2.5, drain is at 3.5. So, are we good with M1? Is M1 in saturation? So, that is green. What about M3? Gate and drain are connected to each other. Ok. Alright. So, what is the M4? What is the potential at its drain? $V_T + \Delta V$?

Student: 1.2.

1.2., is M4 in saturation or not, Kuldeep?

Student: Yes sir

Sure. Ok. So, M4 is good. What about M5? The gate voltage is at 1.2. The drain voltage is at 2.5. So, that guy is good. Right. What about M2? The gate voltage is at 2.5. Drain voltage is at 1.2. Alright. So, what comment can you make about M2?

It is not in saturation. Ok. Alright so, what is the conclusion of our story? I mean, is this going to work as an op-amp or not? Because assuming it works as an op-amp, we went and found all the node potentials everywhere. The quiescent voltage is everywhere. And we find that already there is a device in trouble. It cannot be in saturation, which means that you cannot have a high gain, which basically means that, therefore, this is not an this is not an op-amp. Ok, right. Just because, you know, the input impedance is infinite and output impedance is 0. And if all the devices operate in saturation, right, then this is a, then this is an op-amp, right. Just like how?

Just because something looks like an iPhone, it is not an iPhone. Isn't it? So, clearly using an NMOS common source amplifier, hey, what can I say? It did not work out. And now, hopefully, we understand why. Why I mean, intuitively, can we see why you are choosing, I mean, can somebody look at it and say, I mean, this was a stupid idea to begin with I mean, you know, why did we even bother? Ok. If you have a NMOS common source amplifier, what comment can you make about the quiescent voltage of the input? Will it be close to ground or will it be, will it be, you know, close to V_{dd}?

This NMOS transistor expects a quiescent voltage, which is close to ground right. So, if you cascade the NMOS common source amplifier directly with the differential pair, then the differential pair's output voltage, quiescent output voltage is constrained has to be close to ground in order to be able to make it to be able to ensure that M5 is happy. In other words, the output quiescent voltages of the first stage and second stage are simply not compatible. Correct? Ok. So, I mean, it does not mean that the second stage is bad or the first stage is bad right. It is just that these two stages are simply not compatible. Isn't it? Ok. So, if you want the two stages to be compatible, what do we want to ensure therefore I have spelt out the root cause. What is the fix?

Do not jump steps. The two stages are not compatible. Correct? So, what is the fix? You have to make sure that the quiescent voltage that the second stage needs at its input is acceptable to the first stage output. Correct. Ok. So, what suggestion can you make? So, clearly the NMOS, what is the problem with the NMOS second stage? The input quiescent voltage that the NMOS stage needs is close to ground. And, but what we actually need is a common source stage whose input quiescent voltage is close to V_{dd}. Right. Ok. So, what comment can we make about the second stage therefore? What should we do?

I know that is what I understand, but what suggestion do you have? You replace it?

Student: NMOS.

I mean, see, the answer is a no-brainer simply because remember that NMOS and PMOS transistors act in a complementary fashion. If a certain amplifier stage made with NMOS transistors, you know, requires say a low input quiescent voltage, if you just convert the NMOS stage to a PMOS stage. The behavior will be complementary. So, it will need an input voltage which is high. So, what do we do now, therefore?

You remove the NMOS. Ok. Now, somebody help me fix this diagram. What should I do?

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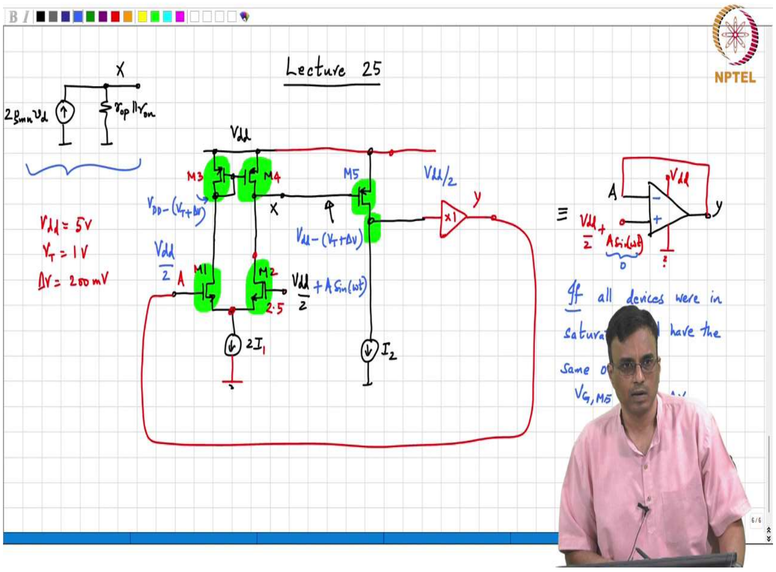

We need a common source. Active load will eventually be an NMOS transistor, but at this point we just basically say I 2. Alright. And this goes here. Ok. Another alternative we could have tried was if you wanted to if we insisted on using an NMOS common source stage in the second stage, what could we have done? Do you understand the question? We you I mean we now we have gone and changed the second stage from an NMOS to a PMOS. If we insisted on keeping the second stage as an NMOS common source amplifier, is there something we could have done to make the output levels of the first stage and the second stage compatible? So, basically, we could have as well used a PMOS input differential pair with an NMOS active load and drive an NMOS common source second stage. Do you understand now man? Right. Ok. So, now let us see if this works. So, if this is $V_{dd}/2$, alright.

Quickly let us go through all the quiescent voltages. What is this voltage going to be now? $V_{dd} - V_T + \Delta V$, alright. And all the other potentials you know remain the same. So, let us figure out quickly device by device if this is ok. So, M1, ok, not ok?

Student: Ok.

M2?

Student: Ok sir.

The drain potential is close to V_{dd}. It is actually in the example for instance we are at 3.8 volts; whereas, the gate of M2 is at 2.5 volts. So, the drain is much higher than the gate. So, the M2 is ok. What about M3? M3 drain and gate are shorted anyways, never a problem. M 4, gate potential and the drain potential are the same so, M4 is not a problem. What about M5? What is the drain potential?

Student: $V_{dd}/2$.

$V_{dd}/2$, ok. So, basically the M5 is also fine. Is that clear? Ok. So, basically this is a workable amplifier ok. And if so, this just makes sure that the quiescent points all seem to be ok. Then when we add a sine wave at the input, I mean there will obviously be a maximum amplitude before which device or the other goes into the triode region ok. And what comment can you make? So, now that we fix the second stage, what do we do about the third stage?

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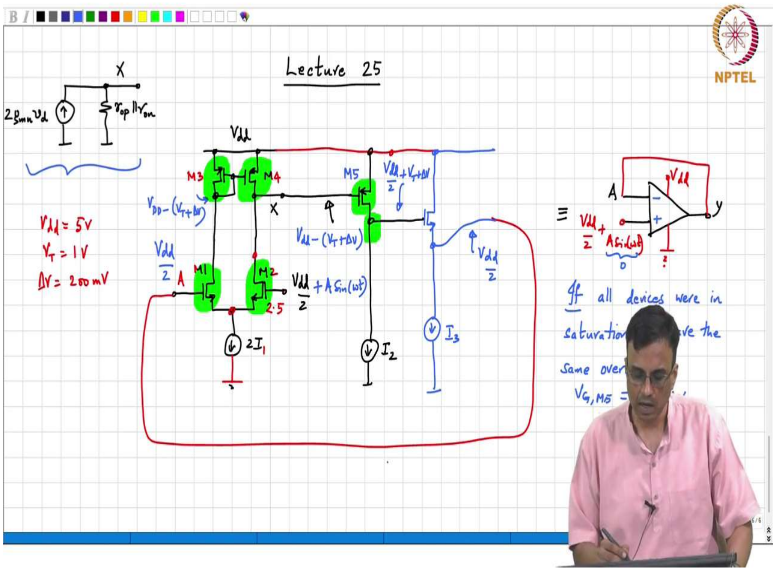

A common drain I mean is that you can use either NMOS or PMOS. So, let us say this is I_3. Alright. So, now what comment can you make about this potential?

Student: $V_{dd}/2$.

Still $V_{dd}/2$. What is this potential? This is $V_{dd}/2 + V_T + \Delta V$. Ok. Now, when we add and. So, this is basically. So, this is workable. CMOS op-amp ok. Except that we have to worry about stability which we will do later. But at this point, from an incremental DC gain point of view where the DC gain is large, this is the inverting terminal.

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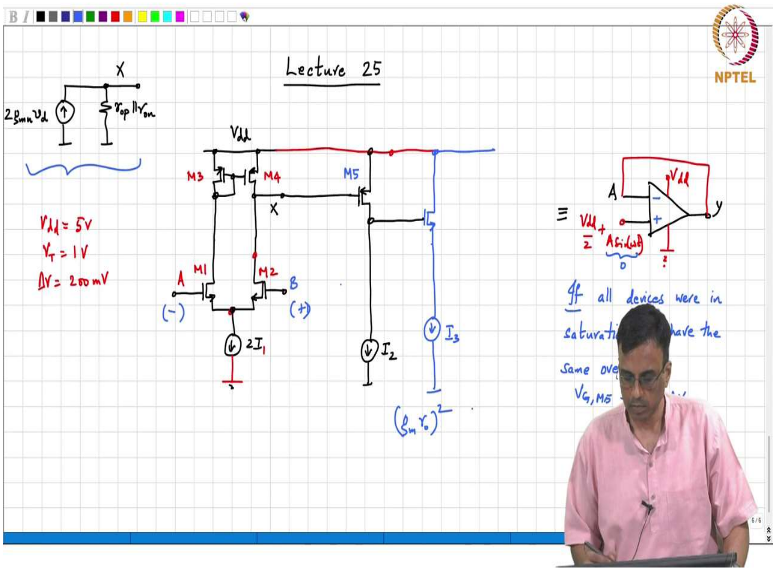

This is the non-inverting terminal. And this is a two-stage operational amplifier with a gain of the order of $(g_m r_o)^2$. Alright. So, we will stop here. We will continue in the next class.