Analog Electronic Circuits
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Lecture - 53
The Two-Stage Opamp and Single-Supply Operation

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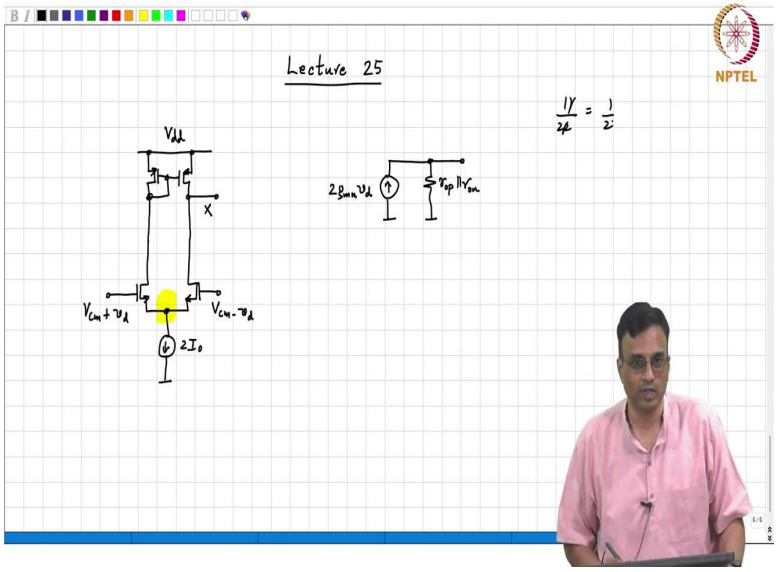

Alright. Good morning and welcome to Analog and Electronic Circuits, this is Lecture 25. So, in the last class we looked at the differential pair with an active load. And after a fair bit of analysis, we basically concluded that as far as the small signal equivalent is concerned this is $V_{cm} + v_d$ and this is $V_{cm} - v_d$ the this node x if you look at it the Norton equivalent is what is the short circuit current? It is 2 g_m of the NMOS transistors times v_d and the output resistance is $r_{op}//r_{on}$, right.

And we also recognize that even though it is possible to get this result using fake analysis like for instance if you assume that the virtual ground there, I mean that the common source node is incrementally grounded. You will still get the same result, though it just happens to be what you call a serendipity, right.

It is just like saying 11 by 22 is basically 1 by 2 right, ok and sure enough you do 111 by 222 and you cancel 2 of them also it looks the same. You can even cancel the hundredth place and the unit's place and still everything will look the same just because the final answer is correct

it does not mean that the process is correct, ok. So, this is one more of those things, but it is a good thing to remember that the answer is the same. So, that you do not scratch your head when you have to find the answer, alright. So, our aim is to make an operational amplifier.

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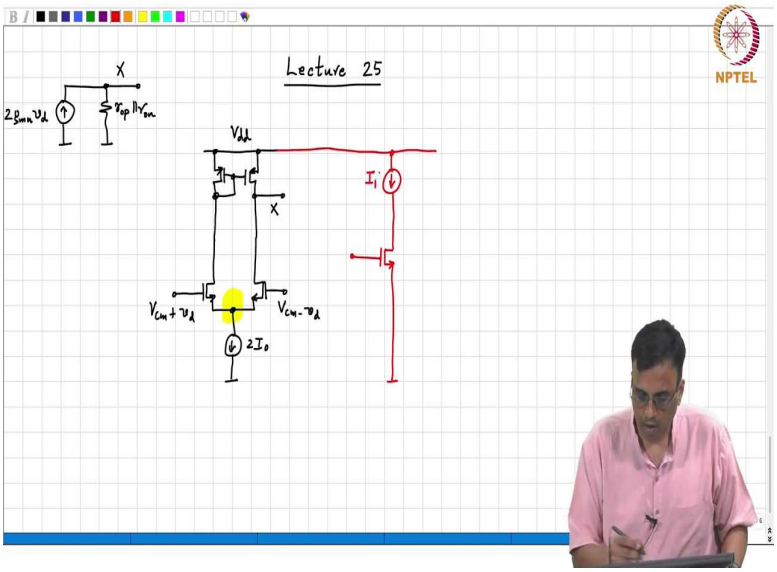

And, the next order of businesses is to get more gain because as you can see the incremental gain that is possible from the differential amplifier right is about of the order of $g_m r_o$, alright which is maybe 30, 40 something like that and we have to increase the gain. So, we have to cascade it. One way of fixing that is to say that if we cascade this gain stage with another gain stage with again the maximum gain, we can get a common source amplifier with an active load which will give another roughly another factor of $g_m r_o$. And so, if you have say 40 and 40 you basically have 1600, right for the gain which is a respectable, right.

And, after that we would the op amp is basically remembering a voltage controlled voltage source with a lot of gain. We have gotten a lot of gain right, but after that we will need to make sure that we need to get a voltage-controlled voltage source that has a very low output impedance, right? So, we need to make sure that whatever we build not only has high voltage gain, but also has a low output impedance. It does not help to have a very large gain which goes to 0 as soon as you load it up with some load resistance ok, but first things first we will have to let us just simply figure out how to get high gain, right. So, the consensus is that we need to cascade it with another high gain stage. The simplest high gain stage we know is the common source amplifier. So, the question is what kind of and we know that common source

amplifiers can be made with either PMOS transistors or NMOS transistors. So, the obvious question now is should we use a PMOS based common source amplifier or an NMOS based common source amplifier correct, that evidently two possibilities are ok. So, if you use a PMOS I mean when we do not know what we do?

Yeah, well I mean there are only two possibilities, right. If there was 2000 possibilities then you have to be smart about it and figure out what you will try, but if there are only two possibilities rather than spend time trying to figure out how to be smart you might as well try both the alternatives and then see if any of them work I mean it could turn out that none of them work in which case you have to scratch your head and figure out and look at your neighbor's question paper or answer paper, right. If both of them work or it is great. So, we know that there are more than one ways of doing it and if only one of them works well bingo I mean we know that only one way works ok.

So, we have started everything with NMOS. So, we might as well do this with NMOS. So, what I will do is basically say ok here is a common source amplifier and we need an active load. So, what do we do with the load? We need a PMOS current source and I am going to just draw like this just otherwise you have to draw transistors in the mirror and all that. So, I will just simply say what you call it.

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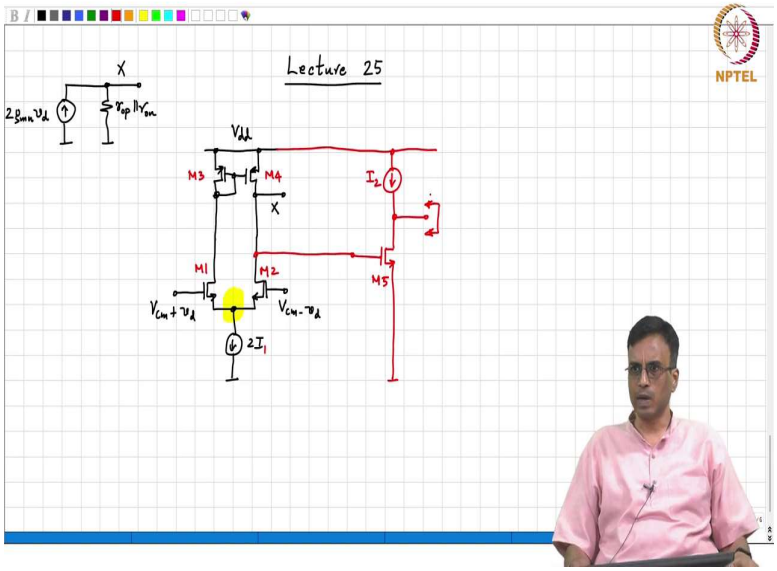

Or let me do one thing let me call this I_1 which stands for the first stage and I_2 which stands for the second stage alright and what do you call I will cascade the common source amplifier. It has an active load right, ok.

And, this will give me an incremental gain when all transistors are operating in saturation : M 2, M 3, M 4, M 5. What gain will it give me approximately assuming all the transistors are operating in saturation? What gain will we get $(g_m r_o)^2$, right and what comment can you make assuming everything is operating in saturation? What comment can you make about the output resistance looking in there? Yeah, what will it be? It will be the order of r_o of the NMOS transistor in parallel with the output resistance of the current source. I mean in this again let me remind you that I 2 is marked as a current source, but it in reality is going to be implemented by a PMOS transistor.

So, the effective output resistance looking at the drain of M 5 is going to be assuming everything operates in saturation is going to be large. So, we have a large gain, but we have a large output impedance which is no good because if you have a large output resistance then simply loading the output is going to reduce the gain big time, correct. So, what do we do? We have a large gain large impedance. We want to get large gain, but we want low output impedance. So, what kind of controlled source will you put there?

A voltage controlled voltage source and what is the simplest voltage controlled voltage source ? The common drain amplifier.

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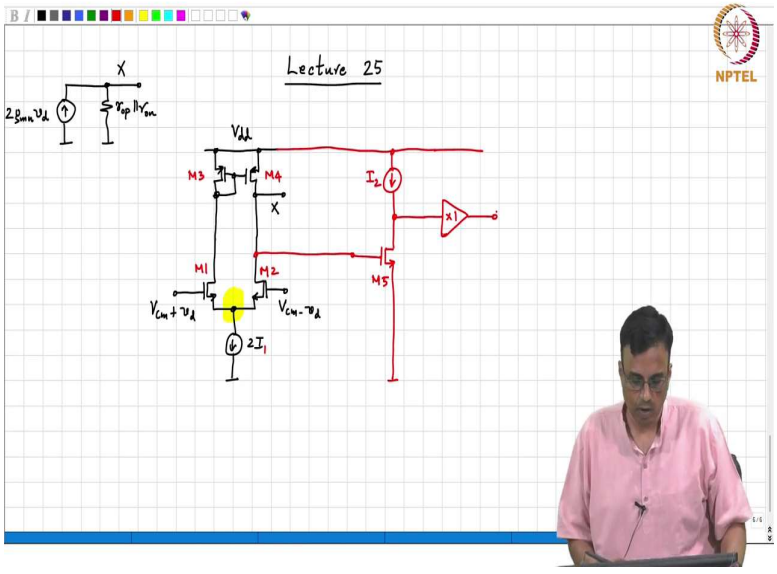

So, we will figure that out as we go along, but at this time let us say we have a common voltage controlled, a common drain amplifier is basically a voltage controlled voltage source ideally with a gain of 1 right. So, let us assume that somehow we will figure this out later. At this point let us assume that we have an ideal VCVS with a gain of 1 right with the insurance that we know how to make this, alright. So, this is my code: what do you call a first cut operational amplifier? We need to figure out whether this is feasible as an op-amp or not ok.

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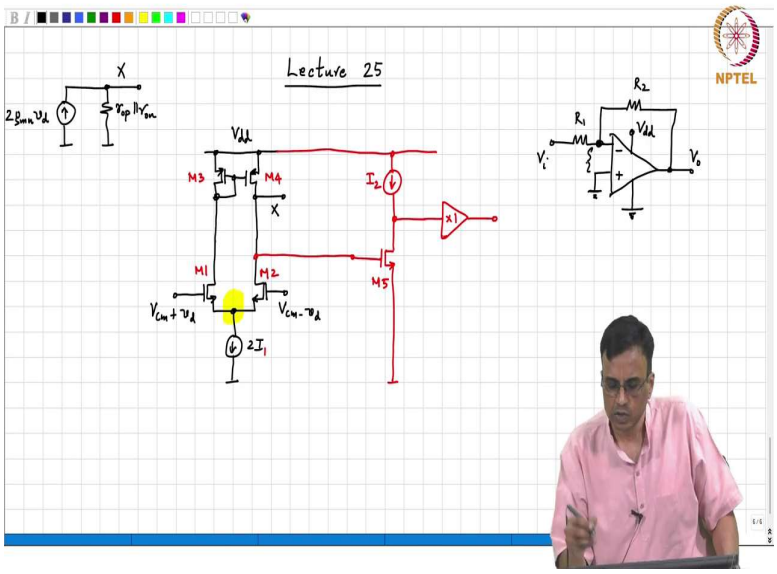

Now, the first thing that I would like to point out is the following and this has got to do with a lot of the circuit diagrams that you probably exposed to in the past and you see routinely in books and papers. And, for example, here is your common inverting amplifier which is V_o/V_i $-R_2/R_1$, but clearly you do not expect the op-amp to work without any supplies, correct? So, what is the implication of drawing this picture?

So, if this is grounded correctly, this must be v_{dd} and what comment can you make about the negative rail of the op-amp? Can this be 0? Well, here is a power source for the op-amp. So, if you did not know the internals of the op-amp. I mean I would not blame you for not knowing this, but now we do know what goes into the at least the first stage of the op-amp is a differential pair like that the one shown on the in the on the left correct.

Now, the question is can this be ground and can the negative rail also be ground, alright. We do not know, let us try to figure it out ok assuming it was ok alright assuming that the positive supply rail of the op-amp is v_{dd} and the negative rail is ground which is 0 let us see if this

inverting amp works, correct. So, for example, if the op-amp was working what does it mean to say the op-amp is working? What does it mean to say the op-amp is working?

Yeah. So, the easiest thing to figure out whether the op-amp is doing its job is to measure these two voltages and see if they are the same, right? If that is ensured then all this R_2/R_1 everything will follow, correct?

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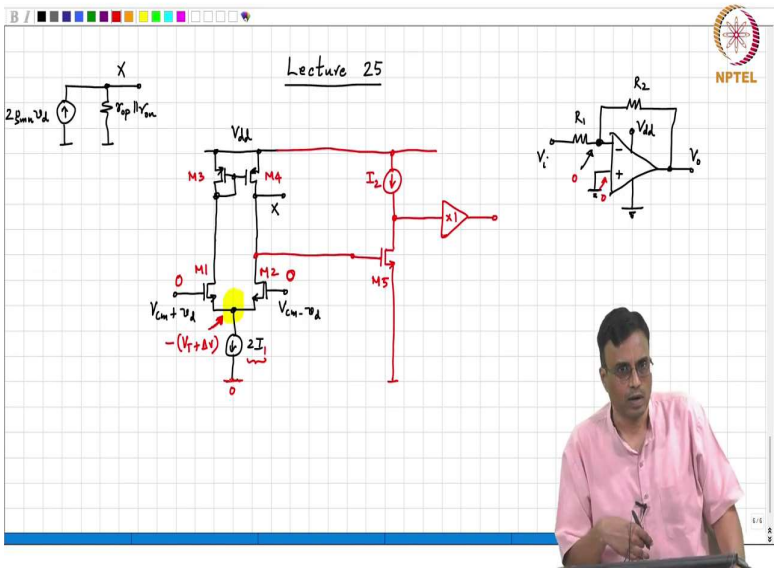

So, if this op-amp is working what comment can you make about that potential?

Student: 0.

That potential is 0, ok. This potential is also obviously 0 correct. So, what. So, if you go into the op-amp the first stage you are going to have a differential pair, correct? So, this voltage is 0. This voltage is 0, correct?

Student: Yes, sir.

Ok if the negative rail is also 0 if the op-amp is working all transistors are operating in saturation. If these two input nodes are 0 what comment can you make about that voltage? What is the current flowing through M 1 and M 2? If the transistors are operating in saturation what are the currents flowing between M 1 and M 2.

Student: I_1.

If I_1 is flowing in M 1 and I 1 is flowing in M 2 what comment can you make about that source node? It will be -(V_t + Δv), where Δ v is the overdrive ok. Now, look at this current source: how it must operate? It must pull current from a node whose potential is lower than the other node, correct. So, is it possible?

Student: No.

It is not possible and therefore, the negative rail cannot be at ground. It must be much lower, right ok and so, that is why. So, when people draw these diagrams correctly, they simply show this and a lot of students really do not understand that you cannot have this situation where you connect the non-inverting terminal to ground and the negative rail of the op-amp is also at ground.

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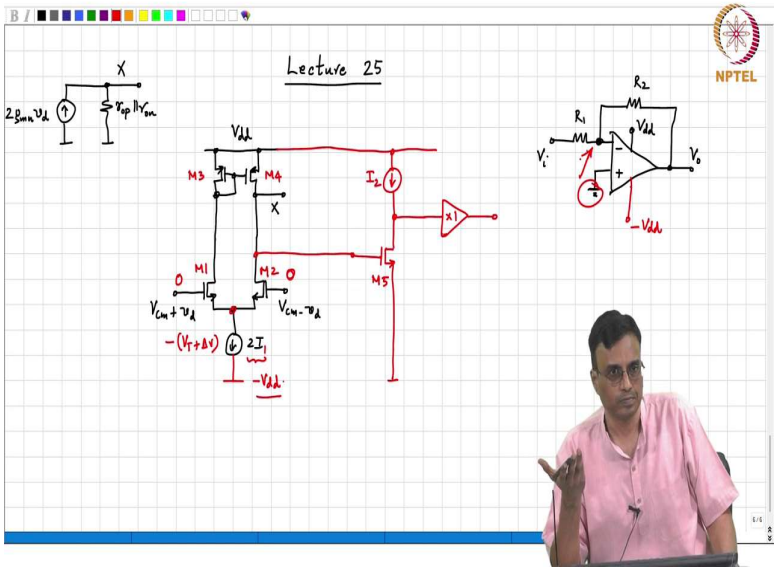

The only way this can work is if this is at some voltage, let us say - v_{dd} that is acceptable because if this is - v_{dd} then, this voltage is –(V_t + Δv) this is -v_{dd} which is much lower and therefore, this current source will be able to function. In other words the common mode voltage that you apply to the input of the op-amp right must be within the common mode range of the differential pair. What do we understand by the common mode range? So, basically if you keep increasing the common mode voltage at the gates of M 1 and M 2 they will eventually go into the triode region; if you keep pushing the common mode voltage lower and lower the transistor I_1 will go into the triode region, right?

So, the common mode range is basically that which keeps all transistors in saturation and clearly as you can see if you use a negative rail of 0 and that is also 0, we end up with a contradiction is clearly not possible to have all the transistor the input stage working which basically means that the gain of the gain of the op-amp cannot be if the transistor input stage transistors do not work what comment can we make about the gain of the op-amp?

There will be no gain, correct? If there is no gain then what comment can you make about that potential there? It will not be the way you will not see a virtual shot right which is a contradiction. So, we said that we are seeing a virtual shot which basically is predicated on the fact that all the transistors are operating in saturation and we go through that line of reasoning and we find that it is not possible for all the transistors to operate in saturation. So, therefore, when people draw diagrams like this it is understood that what you have you have dual supplies.

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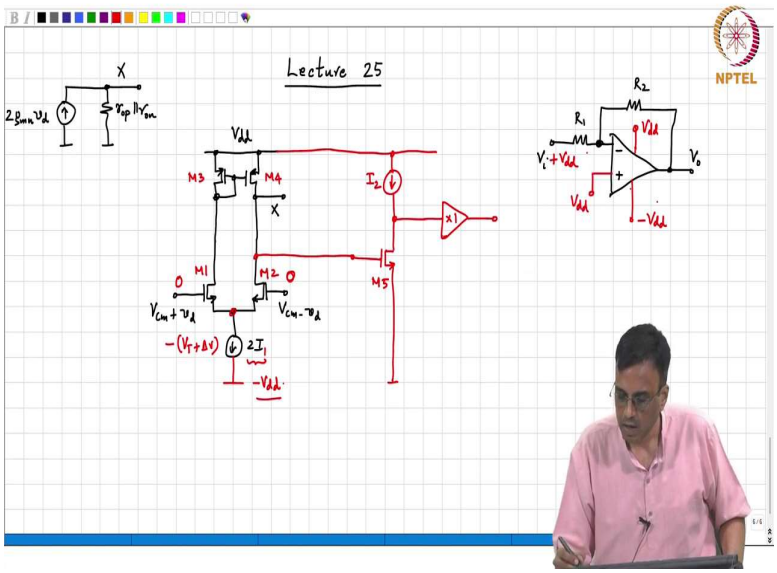

Alternatively, so, again we come back to our usual trick if we do not like negative supplies let us say this is - v_{dd}, what do we do? Add v_{dd} to all the nodes. So, in other words V_i instead of riding on ground right we will ride on v_{dd}. This will be v_{dd} this will be ground, and that will be $2v_{dd}$?

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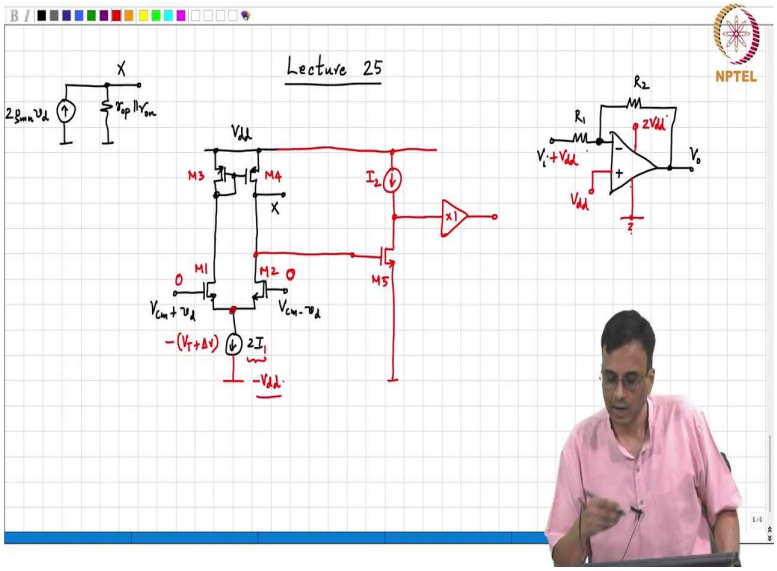

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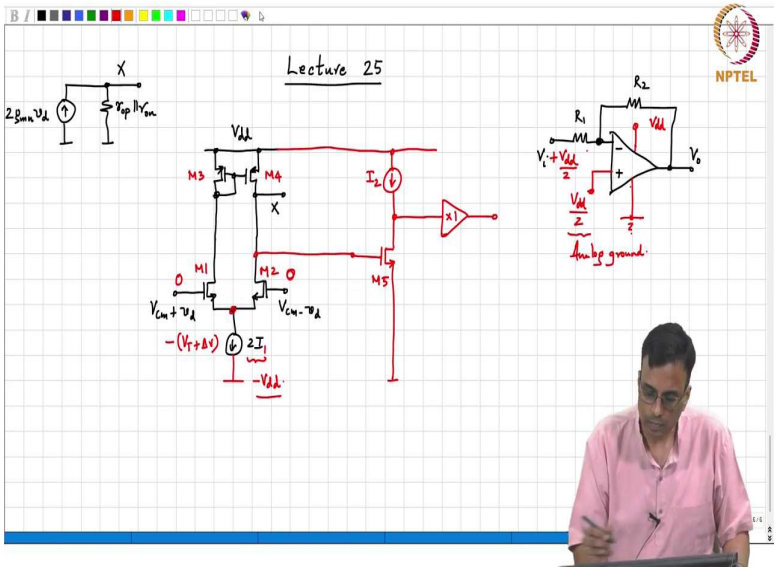

And instead of calling this $2v_{dd}$ we call this v_{dd}, then what will we call the other $v_{dd}/2$ ok does it make sense. So, this is sometimes called to differentiate it from. This is sometimes called analog ground, ok alright and as I said it is not immediately apparent why this must be $v_{dd}/2$, right unless you understand the internals of the op-amp. There are special op-amps which can basically go where their common mode range can be all the way from 0 to v_{dd}, right and such op-amps are called rail to rail op-amps. But they are within codes designed using special

techniques where they recognize this problem and try to fix it ok alright. But, for a general purpose op-amp the common mode range will not be 0 to v_{dd} ok anyway.

So, that is basically something that we have to be aware of whenever we design an inverting amplifier or any amplifier with a with a virtual ground right that virtual ground I mean where any of the input terminals of the op-amp is grounded you must make sure that the common mode voltage that is so developed at the input of the op-amp must be within the common mode range of the differential pair, is that clear?