

Analog Electronic Circuits  
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Lecture - 51  
The Differential Amplifier with Active Load Part 2

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The slide contains two hand-drawn diagrams on a grid background. The left diagram shows a differential amplifier with an active load. It consists of two NMOS transistors, M1 and M2, whose sources are connected to a common source node with a tail current source of  $2I_0$ . The gates of M1 and M2 are connected to a common gate node. The drains of M1 and M2 are connected to two PMOS transistors, M3 and M4, which are connected to a supply voltage  $V_{DD}$ . The gates of M3 and M4 are connected to a common gate node. The output voltages are  $V_{out} + v_d$  and  $V_{out} - v_d$ . The right diagram is titled '\* Simplified analysis:'. It shows a small-signal equivalent circuit for the active load. It includes a PMOS transistor M3 with a gate-source voltage of  $v_d$  and a drain current of  $i_x = ?$ . The equivalent circuit is shown to be a current source of  $2g_m v_d$  in parallel with a 0V source, which is then simplified to a current source of  $2g_m v_d$ .

$\lambda_n = \lambda_p = 0$

$i_x = 2g_m v_d$

$2I_0$

$V_{DD}$

$M_1, M_2, M_3, M_4$

$V_{out} + v_d$

$V_{out} - v_d$

$v_d$

$i_x = ?$

$2g_m v_d$

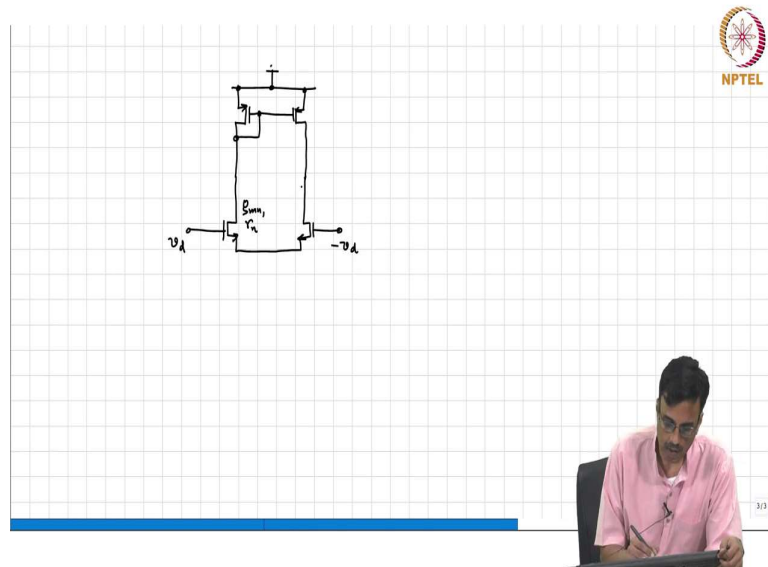
$0V$

$2g_m v_d$

NPTEL

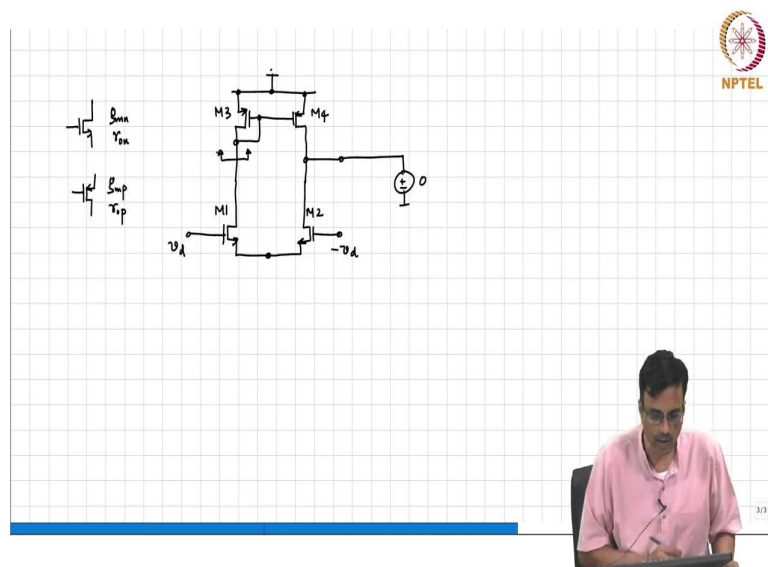
Alright now, what is the next thing to do?  $\lambda_n = \lambda_p \neq 0$ , right? That turns out to be actually somewhat involved. So, I want you to all be awake.

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And this is I think the first time you are actually looking at circuits with more than 2 transistors, where both transistors are doing some work. In fact, we are looking at 4 transistors now. The incremental equivalent is all I am going to draw; we are going to go from there. Alright so that is ground. So, as usual I am going to this is  $v_d$ , this is  $-v_d$  and so this is  $g_{mn}$ ,  $r_{on}$ , ok.

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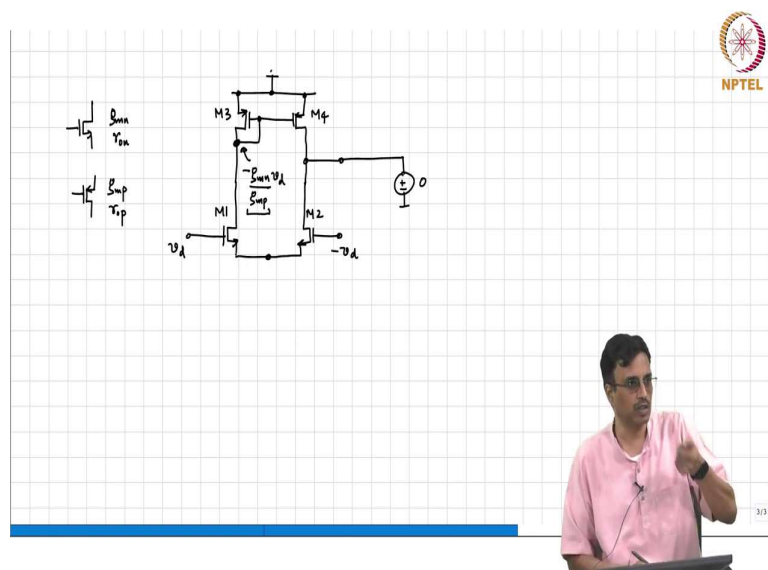
So, the NMOS transistors I am not going to mark it there, because it becomes very cluttered. So, this is  $g_{mn}$ ,  $r_{on}$  is the output resistance of the NMOS transistors, the PMOS transistor is  $g_{mp}$

and  $R_o$ , correct? Now, what are we trying to find? We are trying to find  $V_o$  or the gain equivalently. So, as usual, what will we do? How will you find the gain? What are we? What did we do in the previous case?

You find the Norton current and then find the Norton resistance and then you know I do the same. So, the Norton current is pretty straight forward. So, what will we do? We will put a 0 here ok and technically speaking you know the output resistances of the transistors M1, M2, M3 and M4 are not.

The output resistance is not infinite. So, technically it is that there is no this node here is not is not 0 potential, right? However, what comment can you make about the incremental voltage at that node? So, basically right I mean we know that this is going to be not 0, but it is going to be only close to 0.

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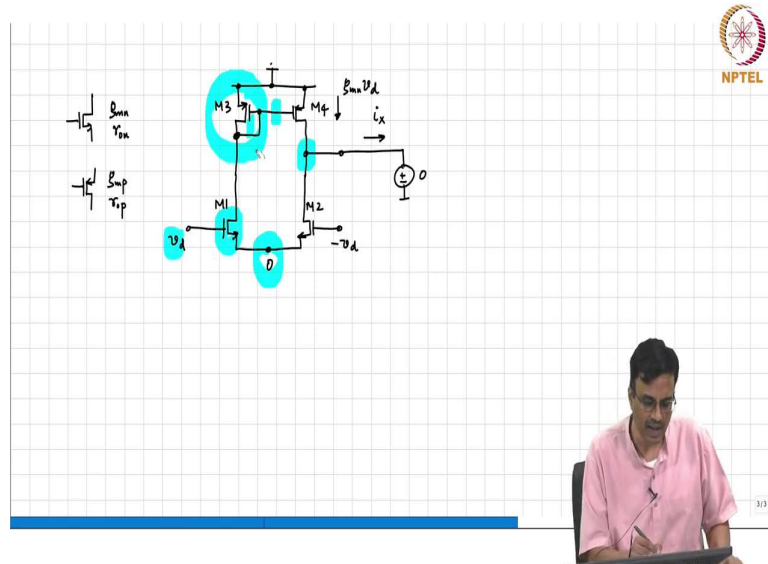
So, basically you know if you assume that then you can see that this voltage is going to be some  $-g_{mn}$  approximately  $-g_{mn}/g_{mp} V_d$ , right? Which is of the same order as what comment can you make about that quantity folks?

Roughly same order magnitudes that is also going to be roughly about  $V_d$  and if  $g_m r_{on}$  and  $g_m r_{op}$  are large numbers. If the drain changes by a small amount, what comment can you make about the effect of it on the source potential? It is going to be divided by some large number, so basically for all practical purposes.



there is also  $r_o$  of that transistor. But those, but those  $g_m r_o$  is a large number and therefore we neglect it.

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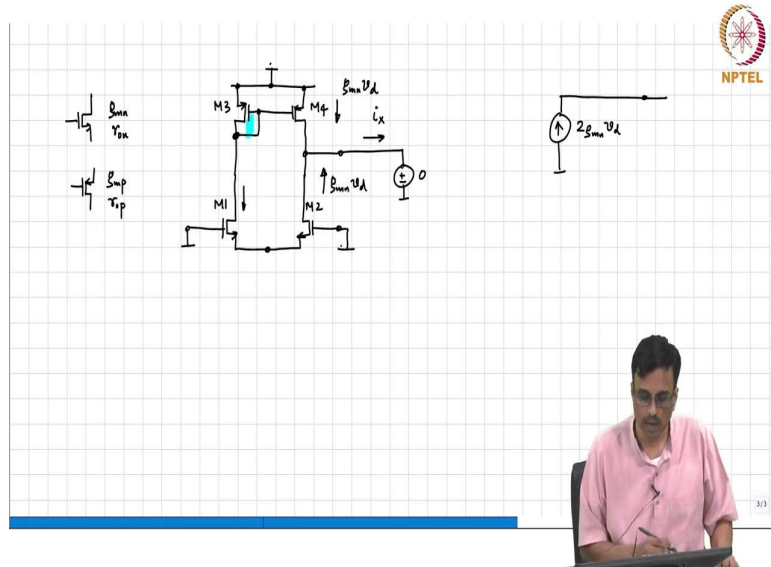


So, what is so effective for all practical purposes therefore, this current is nothing but  $g_m v_d$  just like in the case with infinite  $r_o$ , ok? Let me reiterate there again, right? Technically speaking the circuit is no longer symmetric. So, you cannot assume that this voltage is 0. In fact, it is not 0. However, because this is 0 and this resistance is small or basically this incremental resistance is of the order of the  $g_m$  of the NMOS transistor, right? We see that the voltage swing here is going to be small just like  $v_d$  ok.

So, if the drains of both these M1 and M2 are pretty much not swinging, M2 of course is absolutely not swinging, M1 is swinging very little for all practical purposes therefore, the remember that the effect of a drain voltage swing gets divided down by the  $g_m r_o$  of device when it comes to the source.

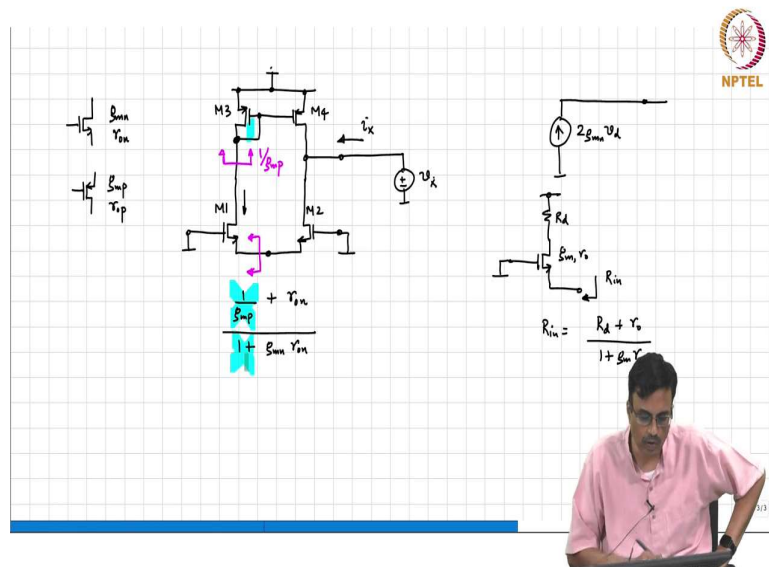
So, since the drain is swinging very little to begin with, its influence on the source potential is negligible and therefore for all practical purposes this voltage will be 0, right? So, what will be the; what is the current in M2?

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Sorry, this current is in the opposite direction, this current is sorry, sorry that is correct. Because,  $g_{mn} v_d$  this is in the opposite direction this is  $g_{mn} v_d$ . So,  $i_x$  as before is  $2 g_{mn} v_d$ , alright? Ok now, is the hard part which is well what is the output resistance to find the output resistance what do we do? We removed all the both the independent sources. So, this is ground, this is ground, ok. So, what should we do here?

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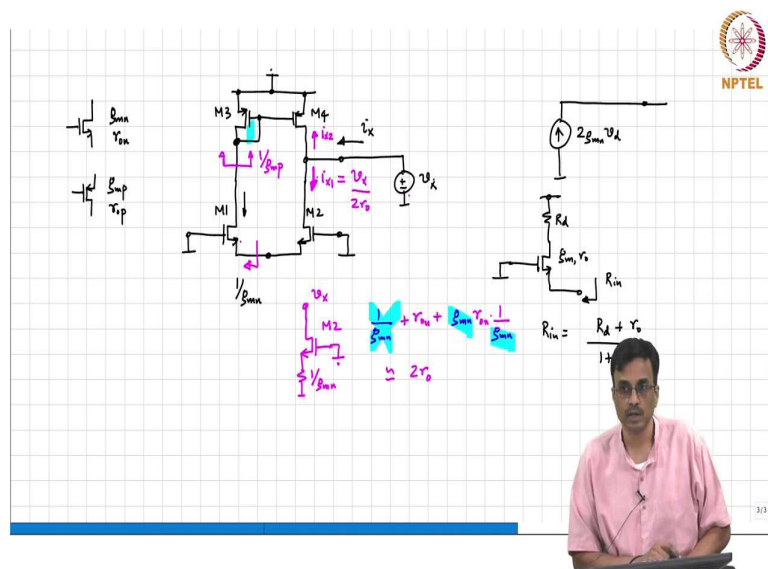


We inject, we apply a  $v_x$ , I will just write call it  $v_x$  and measure this is  $i_x$ , ok alright ok. Now, to do this let us mark down. So, what is the impedance looking in here approximately if  $1/g_{mp}$ , correct? Ok. So, what is it exactly?

$(1/g_{mp})//r_{op}$ , but that  $g_{mp} r_{op}$  is a large number, so we neglect  $r_{op}$ . So, this is that looking in impedance approximately  $1/g_{mp}$ , ok. So, what comment can you make about the looking impedance here? Remember again let me draw your attention to this which we have done before. Let us say you have  $R_d$  here and the transistor has got some output resistance is some  $g_m r_o$ , what is  $r_{in}$ ?  $r_d + r_o(1 + g_m r)$ . This we did in class right, not what you are saying right ok. So, if a sanity check if  $r_o$  is the infinity what should be the input resistance  $1/g_m$ , alright. Does that turn out to be right here? If  $r_o$  tends to infinity it is you can neglect  $r_d$  and therefore, the input resistance becomes  $1/g_m$  alright. In our case now what is  $r_d$  here is  $(1/g_{mp} + r_{on})/(1 + g_{mn} r_{on})$  ok. So, what can we approximate this as? Which is larger? In the numerator which term can be neglected?

You can neglect this guy in the denominator you can neglect 1. So, what do we have?  $1/g_{mn}$ , ok.

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So, even though there is a resistance in the drain, because that resistance is small compared to yeah because it is small compared to the output resistance of M1, right. You basically have no influence on it. This is equivalent to saying exactly the same argument. I do not know if you

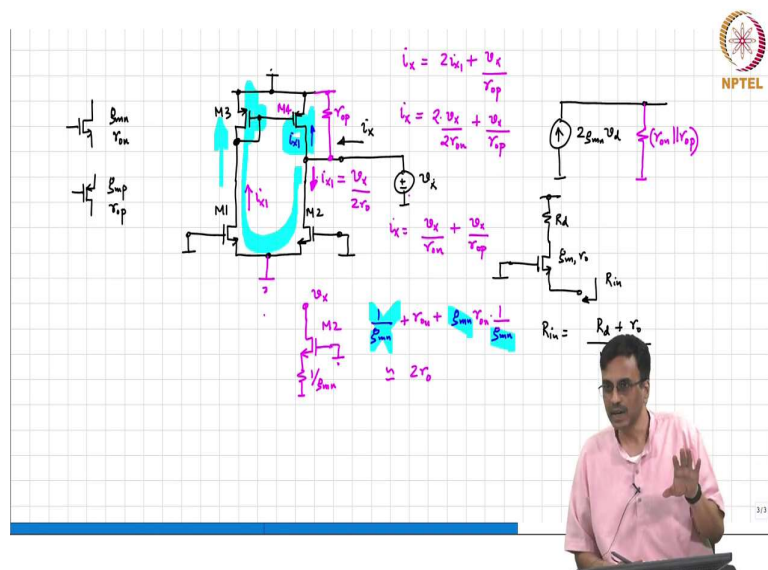
are able to perceive this, but this is exactly the same argument we made for when we did the Norton equivalent we said even though the circuit is actually asymmetric, right.

The for all practical purposes we can assume that that source common source resistance the common source point is has 0 potential, because I mean the looking in impedance on the left side is approximately  $1/g_{mn}$  which is what we would have got if  $\lambda_n$  was 0, correct and the what is the resistance looking in into the source of M2.  $1/g_m$ , right. There is of course another you know  $r_{on}$  in parallel, but again that is small. So, is that clear? Ok so this is  $1/g_{mn}$ , alright. So, now I mean why are we doing all this? Because we are applying a voltage  $v_x$  here the  $i_x$  has 2 paths one is like that one is  $i_x$  is a sum of 2 currents, we want to find both the current so that we can find  $i_x$ .

So, to find this current here let us call that  $i_{x1}$  that is  $i_{x2}$ . How will you find  $i_{x1}$ ? We have to find the resistance looking down from the drain of M2. So, for M as far as M2 is concerned therefore, basically to calculate  $i_{x1}$  this is M2. What is there at the source of M2?  $1/g_{mn}$ . So, we are applying  $v_x$  here. So, what is the current and what is the output resistance looking in from the drain of M2?  $1/g_{mn} + r_o + g_{mn} r_{on}(1/g_{mn})$ .

So, this can be neglected, this goes away and this is approximately  $2 r_o$  does make sense ok. So,  $i_{x1}$  is therefore nothing but  $v_x/2 r_o$ . So, where will that current  $i_{x1}$  flow? It will flow through the drain of M2 where must it flow out through? Where must it flow out of source?

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It must go through the source of M2. So, this is  $i_{x1}$  and then what happens to that current it flows through the source of M1 where must it get out? It must get out to the drain of M1, so this is  $i_{x1}$ . So, if  $i_{x1}$  goes into M3. M4 also. So there must be a saying that the M4 is a little bit tricky. You have to be careful, because M4 is got you can think of it as an ideal MOSFET without output resistance and ROP in//correct. The  $g_m$  part of M4 will give you that  $i_{x1}$  right alright and so the total  $I_x$  will therefore, be equal to  $2 i_{x1} + v_x/r_{op}$ . Is that clear? They are actually quite subtle and I mean anyway I will come to the final result and then we will discuss it. So, what is  $i_{x1}$ ?  $2 v_x/r_{on} + v_x/r_{op}$ . Where did you lose me?

See there this is going through the mirror, this  $i_{x1}$  is coming through like this and going through creating a voltage drop at the gate of M3, but M3 and M4 form a mirror. So, that is going to cause that is going to cause that that  $g_m V_{gs}$  of M4 is going to pull the current you are pushing a current into M3.

So, the mirror will basically pull a current in the same direction. Is that clear? Ok so at the end of the day therefore you know after all this work  $I_x$  is therefore nothing but  $v_x/r_{on} + v_x/r_{op}$ . So, what does the resistance look like here? What is the Norton resistance?  $r_{on}/r_{op}$  right. A lot of people would basically say why do you have to go through all this you know this analysis for this? Well, why would not it be ok if we just assume that this is ground then you will get anyway  $r_{on}$  parallel.

Student:  $r_{op}$ .

$r_{op}$  so do you need all this, but you see that it I mean you can happen to get the right answer, but the analysis is actually wrong ok. So, basically that would predict that this  $i_{x1}$  would be 0 right the that would predict that the current flowing incremental current flowing through M3 is 0 that is not correct actually right ok though you get the same final answer.

So, this is a great interview question because you know right somebody asks you to analyse this and basically you will say well this source is grounded and then and then you have  $r_{on} r_{op}$ . Obviously, the answer is  $r_{on}/r_{op}$  and then the interviewer will ask you.

You know how you ground the source of the common source node and then you will scratch your head and say by symmetry and then they will say well output resistance is not 0 where did you get symmetry and then you scratch your head and then say I do not know right. Alright you understand.

So, but this is a great way of remembering the final formula which is  $r_{on}/r_{op}$  ok. So, at the end of so you know after a lot of algebra basically we see that finally the answer is  $r_{on}/r_{op}$ . So, what is the output voltage?

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Handwritten analysis on a grid background:

- Circuit diagram showing a differential pair with a current source and load resistor  $R_d$ .
- Equations for current  $i_x$ :
 
$$i_x = 2i_{d1} + \frac{v_x}{r_{op}}$$

$$i_x = 2g_{m1}v_d + \frac{v_x}{r_{op}}$$

$$i_{d1} = \frac{v_x}{2r_o}$$

$$v_x = \frac{v_x}{r_{on}} + \frac{v_x}{r_{op}}$$
- Input resistance calculation:
 
$$R_{in} = \frac{R_d + r_o}{1 + \beta}$$
- NPTEL logo in the top right corner.

$2 g_{mn} (r_{on}/r_{op}) v_d$ , so the gain incremental gain.

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Handwritten analysis on a grid background:

- Circuit diagram showing a differential pair with a current source and load resistor  $R_d$ .
- Simplified analysis:
 
$$\lambda_n = \lambda_p = 0$$

$$i_x = 2g_{m1}v_d$$
- NPTEL logo in the top right corner.

Therefore is nothing but  $2 g_{mn} v_d (r_{on} // r_{op})$ . Does it make sense? Ok so, that basically covers the differential pair with active load right. Now that I mean so, that finishes the discussion on the small signal properties of the differential pair.