Analog Electronic Circuits
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Lecture - 47
The CMOS Inverter (contd)

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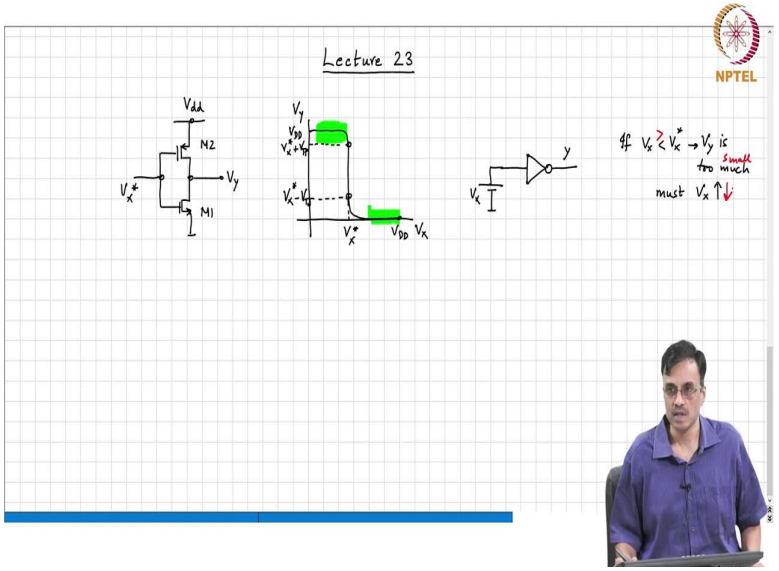

In the last class, we looked at the CMOS inverter and we found that at some magic voltage V_x*, both the transistors M1 and M2 are in saturation. And in theory you get infinite gain since the lambda of the transistors is 0. In practice, because the channel and modulation factor is non-zero, you will get some finite gain. But the hope is that the gain is large; so, if you plot V_x versus V_y, you get a characteristic like this.

So, this is V_{DD}, this is V_{DD} and this is some large slope and that value is the magic voltage V_x*. And this lower limit of swing at the node Y to keep both the transistors in the saturation region is (V_x* - V_{Tn}) right. And on the positive side, it is (V_x* + V_{Tp}) ok and so, the next question is the following. Let us say you are in a lab and the symbol for the CMOS inverter, of course, you all know, is drawn like this.

It does not mean that there are no other terminals, I mean the fact that there is a supply and a ground are understood right, and that is simply not shown to avoid clutter in the diagram. So, let us say you are in a lab right and you basically need to find the magic voltage V_x* right; so, what will we do? How will we go about it? Measure V_y ok.

Ok, so, one you know, one way to do it is basically say, you know well, we know that V_x is the point at which the characteristic has a very sharp slope. So, if you plot V_x versus V_y right, then and obviously, you look at the characteristic and tell me why you can tell us what we can tell we can tell you what the value of V_x* is right. If you do not want to plot the characteristic explicitly, do you think there is any other way of finding this magic voltage? I mean, I hope you understand the question.

You know the answer. You plot the characteristic, you look at the characteristic, you tell what that V_x* is correct. The question I am asking you is, is there a, is there another way of doing this without actually having to plot out the entire characteristic and then find what that V_x* is?

Student: From the current equation find the derivative.

But you are in a lab, I mean, what is the current equation?

Student: we can find the derivative.

That is what he is saying, no.

Student: Yeah sir.

Finding the derivative of the output characteristic is like saying, first I find the output characteristic, and then I differentiate it, right which seems even more complicated than finding the characteristic itself. So, one way to think about it is that if the input, let us say we have some voltage, we put some arbitrary voltage V_x ok. And if the voltage $V_x < V_x$*, what do we expect V_y to be? We expected to be very high, right, because we are somewhere, you know, somewhere here, ok. Then what do you know, I mean, if you put in some arbitrary voltage and you find that the output voltage is too high, right, if its V_{DD}, then you know that the input voltage is less than V_x*, if you put in a voltage which is greater than V_x*, what do we find? The output voltage is too low, so, what should you do then? So, if V_x is less than, is less than V_x*, V_y is too much.

And therefore, you might what must you do? Must increase V_x; on the other hand, if V_x is greater than V_x*, V_y is too small and we must therefore reduce V_x. It makes sense, right? So, if we, if the output is too high, we must increase V_x, if the output is too low, we must decrease V_x; so, what, what do you think we should do?

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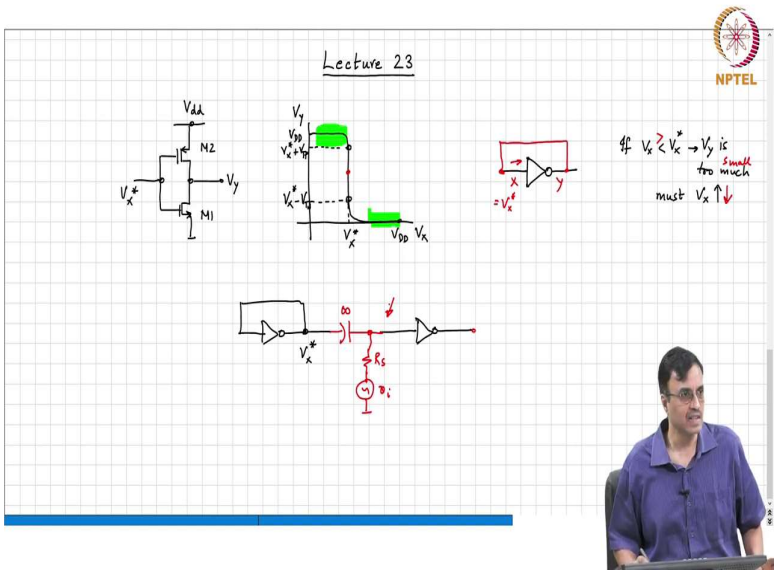

One way to do it is to simply connect nodes X and Y together, ok alright. But when you do something like this, you must also make sure that the quiescent points of the transistors are not disturbed in any way, right? In other words, you know, what do you call, if the node X draws current right, then the node Y will get the potential of node Y will get disturbed, right.

But in this particular case, what comment can we make about the current drawn there? It is 0, right. So, connecting Y to X is not going to rob any current from node Y, right. And as it stands, we see that if V_x is equal to V_y, then, which is equal to V_x*, then both the transistors are indeed operating in saturation alright. So, this is a, you know, this is a common, this is a clean way of establishing, finding that, that V_x*, ok.

And so, one way of making an amplifier therefore, is basically, if you have identical inverters which is possible on a chip; so, one way is to get the magic voltage V_x*. Now, if you want to make an amplifier with a large incremental gain, what do we do? We know how to find the V_x*. So, what do we do? If you want to make the equivalent of a common source amplifier, what do we do? Where do we want to apply this, I mean so, we need to bias this inverter at the right place. What is the right place?

Student: Gate.

Gate, ok at what voltage would we want to V_x* ok and then, on top of it, you must add a small signal. So, we know how to find V_x*; so, now, how do we make the amplifier? Very

good; so, basically, you say, ok, if we take another inverter, ok. The voltage here, the total voltage here must be V_x* plus small v_i; so, the question is, how do we generate this V_x* + v_i? Any suggestions? One suggestion is to say; hey well, why not do this? This is our inverter and why do not we simply connect it here and connect it, how? What should I do? So, let us say we have v_i here and some source resistance R_S; What do I do? So, what is the incremental voltage there?

Please, let us think through this, what do we do? We simply replace every transistor with an incremental equivalent; so, let us do that.

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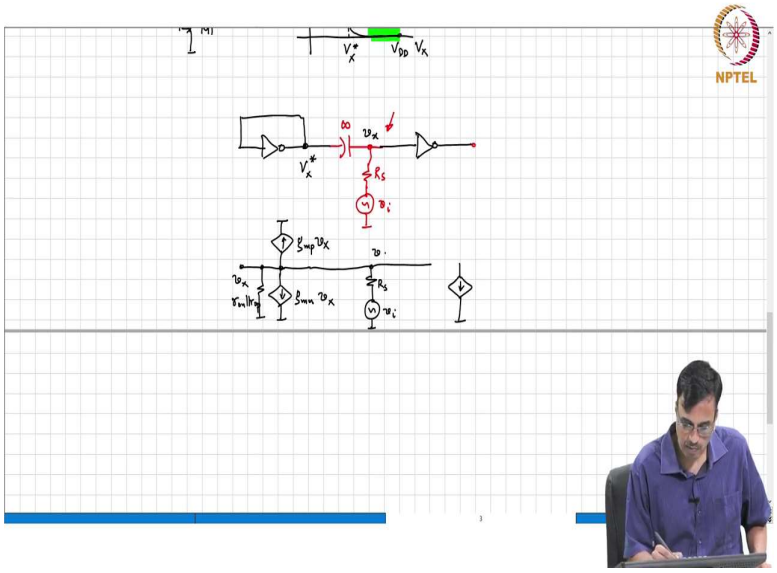

So, so, what is the incremental equivalent of this inverter when the output and input are shorted? So, the NMOS transistor in the inverter is g_{mn} times, let us call this small v_x, alright. This is g_{mp} v_x, this is v_x, alright; sorry, the gate and the drain are connected to each other, alright, then capacitor is a short circuit, this is v_i, this is R_S, and if you have output resistance, I mean, you know, this is r_{on}//r_{op}, this is R_S.

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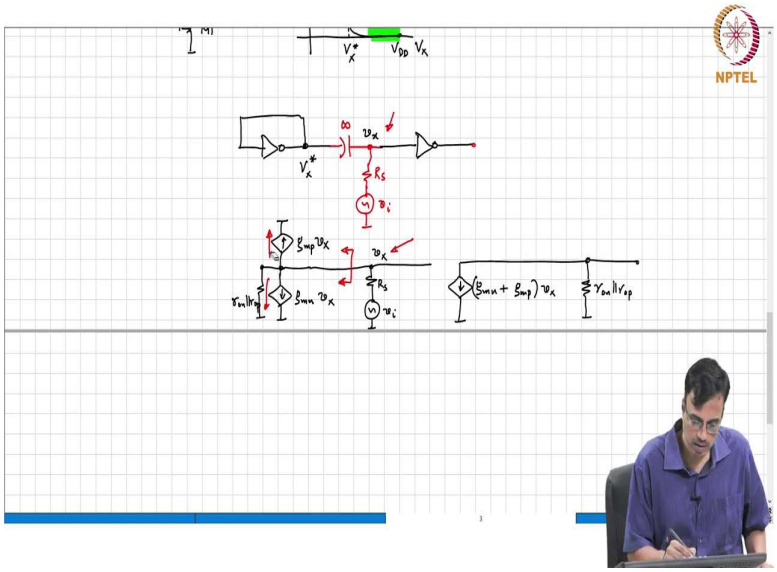

Then you have, this is small v_x anyway, this is g_{mn} v_x, this is $r_{on}//r_{op}$, ok. So, what is the incremental voltage v_x? How does this look by the way? So, you apply voltage v_x here, you are drawing a current g_{mp} v_x there and g_{mn} v_x. So, it is equivalent to having two resistors, $1/g_{mp}$ and $1/g_{mn}$, which are all in parallel.

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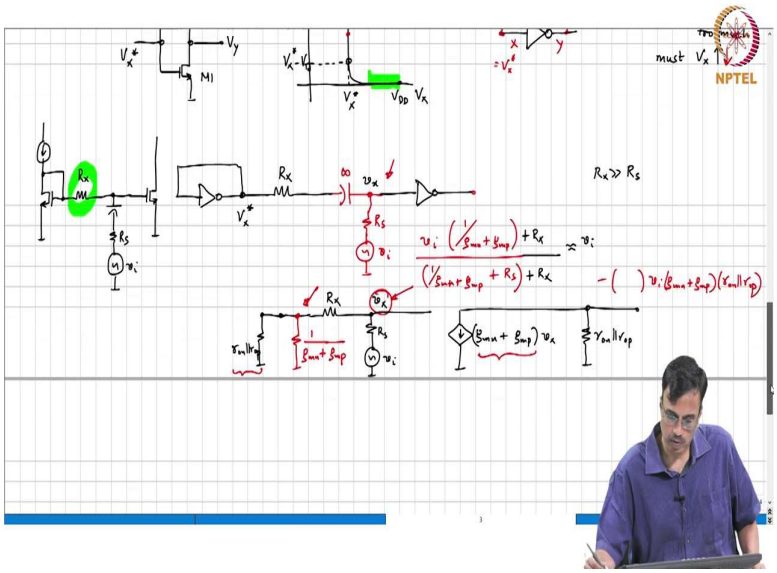

So, basically you can think of this as a resistance, which is $1/(g_{mn} + g_{mp})$, is this clear. So, what comment can you make about small v_x therefore? This is voltage division. So, if you neglect this $r_{on}//r_{op}$, then the voltage there small v_x is nothing but,

$$v_x = \frac{v_i\left(\frac{1}{(g_{mn}+g_{mp})}\right)}{\frac{1}{(g_{mn}+g_{mp})}+R_s}$$

Does it make sense, and then the output voltage will be this multiplied by times minus (g_{mn} + g_{mp}) (r_{on}//r_{op}), does it make sense people. Now, the question is, what happens if, if gain is large, then this g_{mn} + g_{mp} is going to be, I mean you would hope that this g_{mn} + g_{mp} is a large number. Now, therefore, what comment can you make about this quantity? Ok so, the question is, is this even, correct?

We did this before in another context, when do you see the relationship to what we have seen earlier. When we did the common source amplifier, remember, we found a way to bias the transistor in a way such that the current is independent of threshold voltage and all that, what did we do? We use the current mirror right ok, how did we connect it to the common, to the gate of the transistor; now, why did we put the resistor here? To make that voltage independent. Now, does that ring a bell, what is the difference between this and this? Do you see an analogy at least, yes, so, what should we do?

So, what we, therefore, need to do is put a large resistor R_x here; so, in the incremental diagram what happens? You get a large R_x here; so, that becomes +R_x. And if R_x is chosen to be much larger than R_s, this is approximately v_i alright, ok. I mean this is exactly analogous to what we did earlier. I hope you are able to see the connection.

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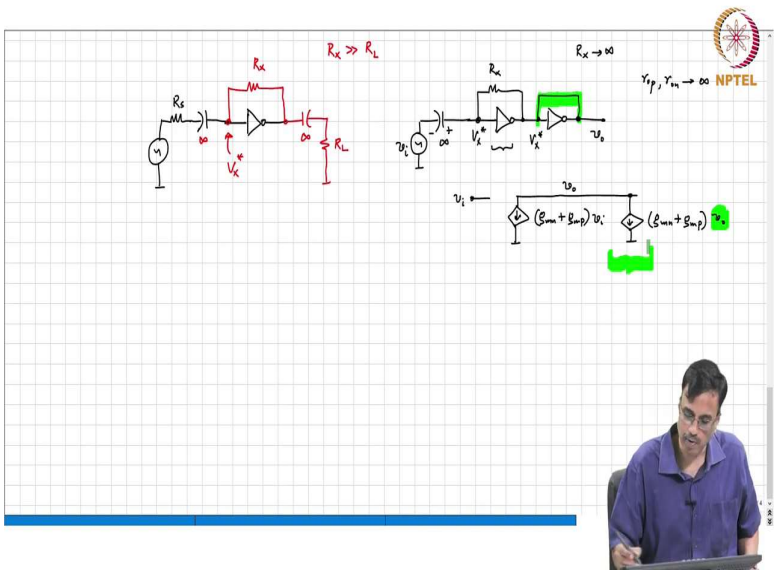

Now, if we want for example, to get a large gain without using an additional inverter right, any suggestions? Do you want to be able to use the input source right and connect it to the inverter? But we want to not be able to use it, let us say we are not able to afford another inverter right.

We have done this before again, if you go and think back to your common source amplifier days, right. One way us to, was to use an additional transistor and a mirror like what we have done here, right. Is there a way of not using this additional transistor, what did we do?

We connected the gate to drain through a?

Student: Resistance.

What resistance, whether the small resistance or a large resistance?

Student: Large.

Very large resistance; so, basically the same thing works here too, right. So, as far as quiescent, much, much larger than for example; let us say, R_L, then what happens? What happens for the operating point? What comment can we make? So, what is this voltage? Quiescent, what is the quiescent voltage there?

Student: V_x*.

V_x* and what comment can you make about the quiescent voltage drop across R_x? It is going to be 0, and that is because the gate does not draw any current. So, you can see that it is very analogous to what we did with the common source amplifier, ok. So, with that the biasing of the CMOS inverter is, that discussion is complete. I may, but there is, I mean so many interesting things you can do with CMOS inverters for example, let us assume this R_x there is very large ok, can somebody look at this and tell me what the incremental output voltage is identical, two identical inverters are there? Let us assume that r_{op} and r_{on} are both infinite and small signal equivalent ok. So, R_x is very large, R_x tends to infinity; So, in a small signal it does not appear. So, this is v_i, what is the small signal equivalent to the CMOS inverter? It is operating, what is the quiescent voltage here? V_x*What is the quiescent voltage there?

V_x* alright; so, what is the incremental equivalent of this, this guy there?

Student: 0.

So, $(g_{mn} + g_{mp})v_i$. So, this will be $(g_{mn} + g_{mp})\ v_o$, ok alright, is this clear? Remember that the drain and the gate of the second inverter are shorted. So, therefore, that is v_o, is this clear, people? So, now what can, what does that guy look like? The voltage across that current source is v_o, the current is $(g_{mn} + g_{mp})\ v_o$; so this is nothing but a resistor of value $1/(g_{mn} + g_{mp})$ alright; so, now what is the output voltage?

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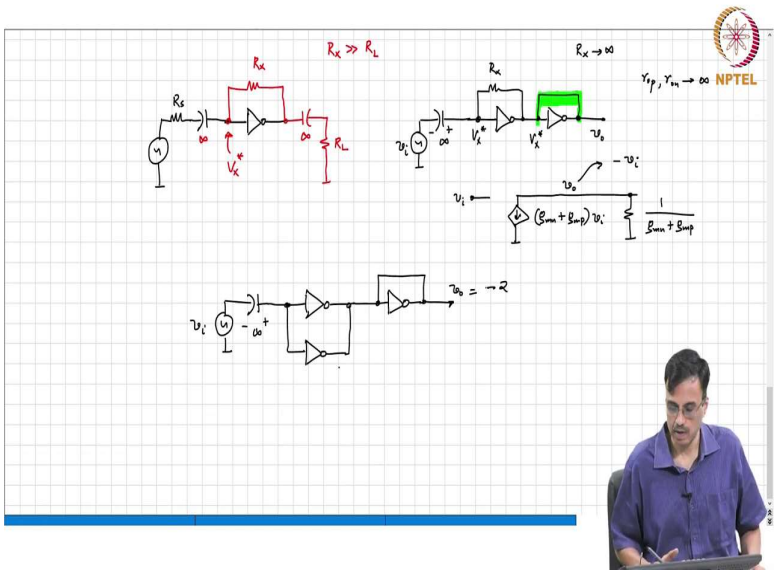

So, this v_o must be therefore, equal to - g_{mp} ok alright. Now, if I take a third identical inverter, now I want to ask you, all the inverters identical, what is v_o? Quick, this cannot be taking that long.

Student: -2.

Instead of two inverters here, I had three 10 inverters in parallel.