**Analog Electronic Circuits**
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**Lecture - 46**
**The CMOS Inverter**

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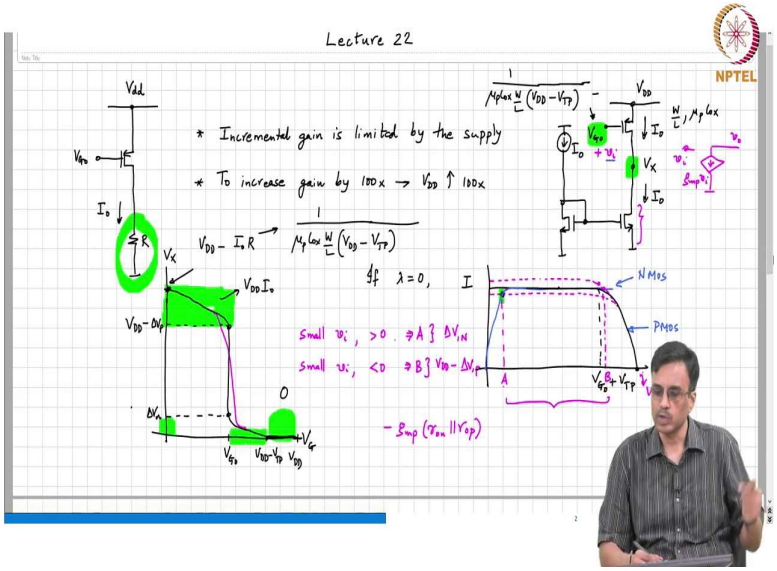


So, this is again you know one of those applications where NMOS and PMOS transistors allow you to do something which would not be possible with NMOS transistors alone or PMOS transistors alone. Of course, nothing prevents us from; here the input was applied at the PMOS transistor and we had an NMOS current source. The same thing can be flipped around. You can have an input applied at the NMOS transistor side and the output at the PMOS. I mean, and the current source being realized using the PMOS transistor. Clear folks, alright. The next thing that I would like to discuss is again taking off on the same theme is another very practically useful circuit.

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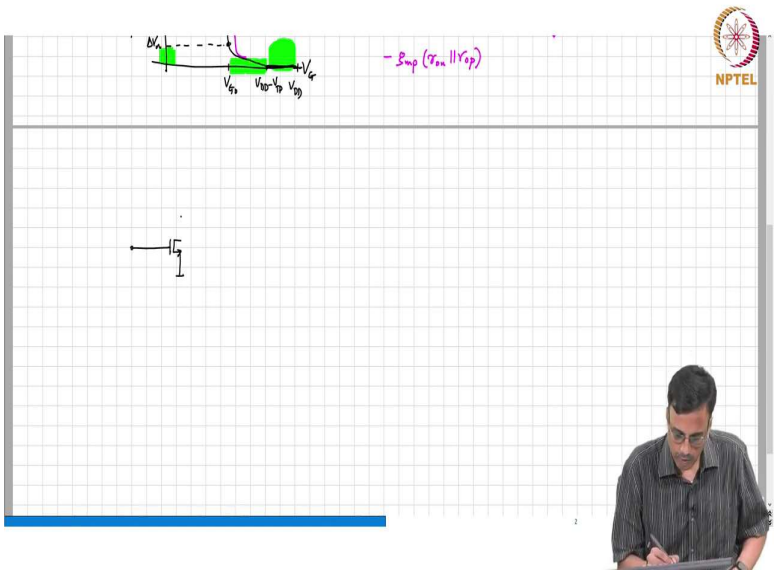


Again, we start with the common source amplifier. I mean if you look at the active load, you know if you want to talk about it as a disadvantage, you see that we need an extra bias current mirror to bias the current source, right. It turns out that there is a way of avoiding that as we will see going forward.

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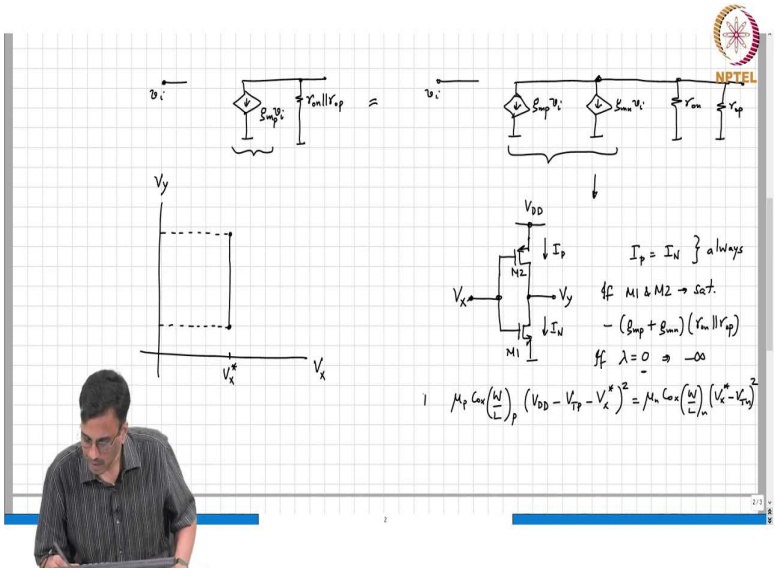


So, let us assume that the common source amplifier that we have seen so far has an incremental equivalent, right. So, this is some $g_m$, and to get a lot of gain we basically you know use a large, you use a as we have seen in the active load, this is $g_m v_i$ and it effectively

goes into some output resistance which in the circuit that we have seen is as a parallel combination of PMOS and the NMOS ok. So, one can also think of this the same nothing happens if we thought of this as the incremental equivalent of $g_m$ p. So, we could have as well interpreted this small signal equivalent and this is $r_{on}//r_{op}$. So, this is $r_{on}$ and this is $r_{op}$. In other words, I am thinking in my mind that this is not coming entirely from the PMOS transistor. It is also coming from the NMOS transistor. So, then now, I mean this is our this is a possibility. And how do we; this is the incremental circuit. So, what comment can we make about the real circuit?

Both the drains of the PMOS in the NMOS, the drains are connected. The gates are also connected. So, basically, the drains are connected, the gates are connected. And what comment can you make about the supply voltage? And I mean what the source of the NMOS transistor is grounded. The source of the PMOS transistor is grounded incrementally, but we know that the current in the PMOS transistor must flow like this. The total current and the NMOS transistor must flow like this. So, this potential must be higher. So, one possibility is to make this $V_{DD}$, correct. So, remember again that this is $I_P$, this is $I_N$, and $I_P$ is exactly equal to $I_N$ always that is irrespective of the region of operation of both the transistors, alright.

Now, if both the transistors operate in saturation, then the gain will be large. What will it be? We have the diagram up already. If both of them M1 and M2 operate in saturation, then the incremental gain is $-(g_{mp}+g_{mn})(r_{on}//r_{op})$, ok. And in and in the special case of $\lambda$ being equal to 0, gain tends to negative infinity, alright. So, to simplify matters let us assume that the $\lambda$ equal to 0, alright. We know that there will be a high gain, but that will only happen at a magic voltage $V_G$. So, if I plot or let me call this capital $V_X$ and $V_Y$, that only happens for a magic value of $V_X$. Why? Both the currents must depend on $V_X$.

If both the transistors are in saturation, what is the meaning of saturation? The currents only depend on $V_X$. And the currents at any rate the currents in M 1 and M 2 have to be equal to KCL. So, there must be only one magic voltage for which both the currents are equal and both the transistors are in saturation. So, how will we find that magic voltage? We will call that $V_X$*.

That would be very simple. We just simply equate the current. So, $\mu_p C_{ox}$ W/L of the PMOS transistor times $(V_{DD} - V_{TP} - V_X^*)^2$ must be equal to $\mu_n C_{ox}$ W/L of the NMOS transistor times $(V_X^* - V_{Tn})^2$. So, if the transistors, I mean if the magic voltage is $V_X$*, the two currents are not

only exactly the same which they have to be, but both the transistors are operating in saturation. So, the incremental gain will be If λ is 0 is Infinite ok. So, basically, the characteristic $V_X$ versus $V_I$ $V_Y$ will basically look like, will be a vertical line, alright. What are the limits of the vertical line? We just did this in another context, just a few minutes back. So, if $V_X$, if the input is infinitesimally greater than $V_X$*, right. So, at $V_X$*, the NMOS current and the PMOS current are exactly the same with both being in saturation. If the input increases beyond $V_X$* by an infinitesimally small amount, what comment can we make if M1 was in saturation? What comment can we make about its current situation? Do you understand the question? If the input $V_X$ was increased infinitesimally above $V_X$*, what is $V_X$*? So, if the input is increased beyond $V_X$*, what comment can we make about M 1's current, if it was operating in saturation? Will it be greater than the PMOS current in saturation or? Ok, let me label this.

Let us say at $V_X$ being the magic voltage $V_X$*. The current flowing in the PMOS transistor which of course, is equal to the current flowing in the NMOS transistor is $I_o$. Now, if I increase the input voltage beyond $V_X$*, what comment can we make about the current in M 1 assuming it was operating in saturation? It will be greater than $I_o$, right? So, what comment can you make about the PMOS current assuming it operates in saturation? It will decrease. So, the PMOS current is now pumping less current, the NMOS current is attempting to pull more current. So, what will happen to the potential of that node Y? It will decrease until both currents are equal. And what will happen to the regions of operation of the NMOS transistor?

If the voltage falls down NMOS will go into the triode region, right. What comment can you make about the incremental gain therefore? As the input becomes larger than $V_X$*What comment can we make about the incremental gain when the transistor goes into the triode region? The incremental gain will decrease. So, the slope will become smaller like this, alright.

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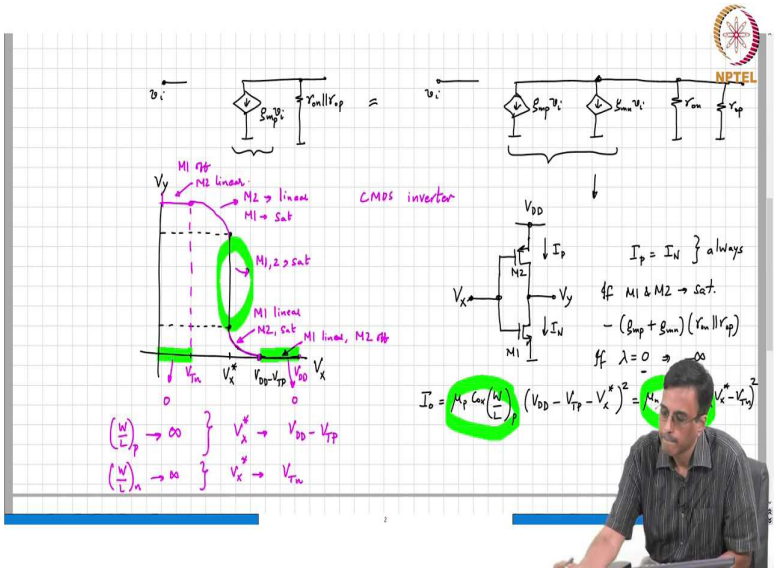


And if we keep decreasing, if we keep increasing $V_X$ further, what will happen? Yeah, as we keep increasing $V_X$ beyond $V_X$*, eventually what will happen? The PMOS transistor will get cut off. And at what voltage will that PMOS transistor get cut off? This is $V_{DD}$ - $V_T$. So, beyond that the output is we are going to remain 0 up to $V_{DD}$, alright. So, in this region what let us finish quickly. The M 1 and M 2 are both operating in saturation. In this region M 1, it is linear. M 2, it is in saturation. Here M 1, linear. M 2 is cut off. Now, what comment can we make about the other side if $V_X$ is less than $V_X$*?

If $V_X$ is less than $V_X$*, the NMOS current will be smaller than $I_o$. And the PMOS current will be more than $I_o$, assuming both are operating in saturation. So, what will happen? That node potential gets pushed up until the PMOS transistor goes into the triode region. So, basically, as you keep pushing you know $V_X$ lower and lower, what happens? Eventually, what will happen? The NMOS transistor will go into cut off, and that happens at $V_{Tn}$. So, here M 2 is in linear, M 1 Saturation. Here M 1 is cut off, and M 2 is in the linear region, ok. So, what is the static power here?

Static power is 0. What is the power here? It is 0. So, that is why this is so important, that is in the static state. There is no power consumption, right? This is an inverter, this is the CMOS inverter, ok. And you often think that an inverter is basically a digital circuit, but you can see that, in this region, I mean it is very attractive for analog designers because it gives you I mean ideally infinite gain, in reality a large gain, alright. And there is and you know this is very simple in the sense that there are no extra nodes. You just have two transistors, no biasing. I mean it is only the supply voltage which you need anyway. And what is $V_X$*? I

mean and $V_X$* As you can see it depends on, what all does it depend on it of course, depends on the strengths of the NMOS and the PMOS transistors, right, their thresholds, and the supply voltage. Sanity check, I mean without looking at these equations intuitively. If the W/L of the PMOS, let us call that of the PMOS transistor, tends to infinity.

In other words, the PMOS transistor is very very strong compared to the NMOS. What comment can you make about the magic voltage? What is it? The answer is correct. $V_D$ $V_X$* tends to $V_{DD}$ - $V_{TP}$. But why does this make intuitive sense? So, basically, that is correct. So, you know if the PMOS transistor is infinitely large, right, so for an input voltage which is even infinitesimally smaller than for $V_{SG}$, which is infinitesimally small you know larger than $V_{TP}$ you will have a huge current flowing. And that will basically, that is enough to cause I mean to support the current that is being pulled by the NMOS transistor, ok. And likewise, when the NMOS transistor becomes infinitely strong, then $V_X$* will tend to $V_T$.

And of course, between these two extremes, you will be able to tweak the threshold between; we can adjust the threshold to tailor the threshold to go between $V_{Tn}$ and $V_{DD}$ - $V_T$ by choosing geometry, alright. So, what is the minimum you know the voltage needed for operation? What is the minimum supply voltage needed if you want to see this inverter characteristic? So, if the supply voltage is less than you know $V_{Tn}$ + $V_{TP}$, then that middle region you cannot have at all, correct ok. So, the minimum supply voltage you need is $V_{DD}$- I mean of course, you can operate some of the transistor and sub threshold and operate below that. But if you want transistors to turn on and work quickly, then the minimum voltage you need is $V_{DD+}$, and minimum $V_{DD}$ is $V_{Tn}$ + $V_{TP}$, alright.

So, with this, I will stop. I will continue in the next class.