Analog Electronic Circuits
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Lecture - 45
The Active Load (contd)

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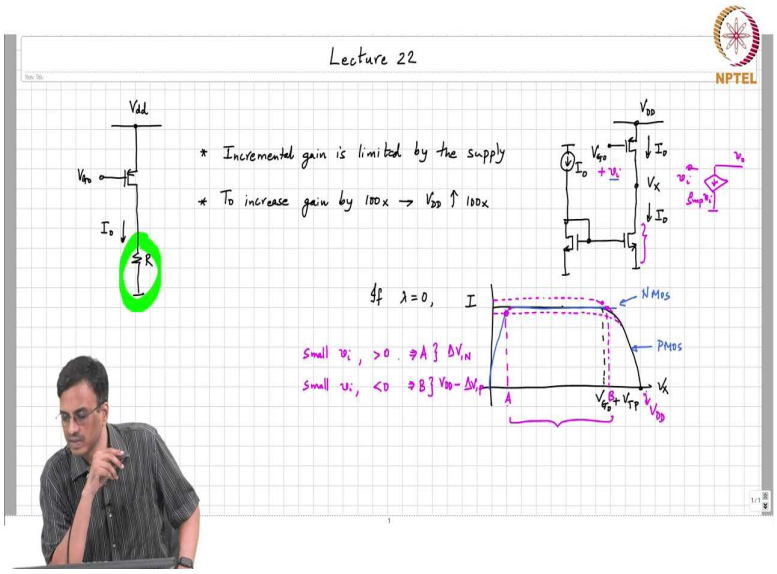

In the last class, we were discussing The Active Load and let me quickly go over that discussion. We were doing this in respect to a PMOS common source amplifier, but the discussion remains largely unchanged with an NMOS amplifier. So, the assumption is that this gate voltage is biased at a potential V_{Go}. The transistor is operating in saturation and carries a drain current I_D I_o.

Now, we said that the incremental gain is of course, given by the negative of g_m r and so, if you want to keep the same bias current and go on increasing the incremental gain, what will we do? What will we do? So, first of all for a fixed V_{DD} and a fixed current, if you want to increase the gain, what will we do? We have to go on increasing R until the transistor just is at the edge of the triode region. Very good. So, but beyond that, it is a point of diminishing return because if you increase the resistance beyond that, the transistor goes into triode where the trans conductance drops and the output resistance goes from being infinite to being some or finite value. And so, graphically also we saw that when we do those lines, we found that the incremental gain is going to fall beyond that maximum value of that resistor.

To fix the problem, therefore, what did we have to do? We had to keep the transistor always at the edge of saturation. So, we had to increase V_{DD} and V g_o by the same amount, so that the transistor continues to stay at the edge of saturation. And we go on increasing R until the transistor, the drain potential you know is exactly such that the transistor is at the edge of at the edge of saturation, right. And therefore, we saw that there is a fundamental limit to the maximum gain you can get with a common source amplifier and that limit depends on the supply voltage, right?

So, if you want to bias the transistor at a given current and get a lot of incremental gain that is only possible by increasing the supply voltage and, we also saw that if you wanted to increase this maximum gain by a factor of 10, the supply voltage has to be increased approximately by a factor of 10, alright.

And, so, basically the key points behind the discussion are that the incremental gain is limited by the supply and B to increase gain by saying I do not know 100x what we need to do? V_{DD} has to go up by 100x ok. And, as you can see, that is a terribly inefficient way because you are going to be burning 100 times the power to get 100 times the gain, alright.

And so, the question is can we do better than this? And last time we saw that if this load element was linear there is no way you can do better. The only way to do better is to replace that load with a?

Student: Non-linear.

Non-linear load and that happened to be. So, this is V_{DD}, this is V_{Go} again and this had to be replaced by an NMOS load and the NMOS transistor must be biased so how should we bias the NMOS transistor? The current in the NMOS transistor must be exactly the same as the current in the PMOS transistor. So, this is I_o and under those circumstances you will get if both the transistors are operating in the saturation region the current here is going to be exactly the same as the current here, alright and what is the incremental gain? So, let us say we add an incremental signal here, what would be the incremental output?

Where is R_o now? So, if the transistors are ideal in the sense that if lambda was 0 for both transistors what comment can we make about the incremental gain?

Student: Infinite.

Infinite why? So, if the output resistance of the transistors is infinite then the incremental gain you can get is actually infinite, right and why does that make sense? Well, there are multiple ways of seeing it. One is to look at the graphical stuff that we saw the last time around. So, let me do that again. So, as far as the PMOS transistor is concerned, if I plot I think we would call this V_X, what do you call V_X? If we plot V_X versus I, for the PMOS transistor it basically does that and this value is going to be $V_{Go} + V_{TP}$, alright. For the NMOS transistor if the NMOS transistor is carrying a current exactly equal to I then the operating point basically will be something like that, right. So, basically you can see that the easy way of looking at it is that if the if v_i incrementally changes by a small amount, right. So, this is the characteristic of the NMOS transistor and this corresponds to the PMOS device.

Now, if the incremental voltage v_i increases by an infinitesimally small amount what comment can you make about the PMOS characteristic? It will drop by an infinitely small amount. I am just for the sake of visual clarity. I am doing something like this. So, this is what will happen if the input was a v_i. So, what happens to the operating point is what will happen to the operating point, right.

And, under these so, if v_i positive what comment can we make: what is the region of operation of the transistors which transistor is operating in in saturation which is in triode?

Student: (Refer Time: 08:07).

PMOS is in saturation NMOS?

Student: Triode.

Triode, alright ok and for I mean this is the operating point let call that A for, but small for v_i, but v_i less than 0, what comment can you make about the operating point? What will happen to the PMOS characteristic? PMOS will move slightly up. So, PMOS goes to the triode region. So, this is actually this operating point that is B. So, you can see that the incremental gain has I mean. So, the PMOS is in triode, right. So, we can see that the output has changed from a voltage which is originally when the for small positive incremental v I where that v I tends to 0, you will see that the output was low, correct almost close to the V_D set of the NMOS transistor, correct.

Now, for a infinitesimally small v_i which is negative the output goes to? V_{DD} - V_D set of the

PMOS transistor, right. So, basically so, this is V_{DD} - V_{DS} is ΔV of the PMOS transistor whereas, this is ΔV of the NMOS transistor. So, you can see that for an infinitesimally small change in v_i the output changes by a by a finite amount which is V_{DD} minus the overdrive of the NMOS minus the overdrive of the PMOS device. So, therefore, you can see that the incremental gain therefore, is infinite, alright.

That is also evident by drawing the small signal equivalent right if you draw the small signal equivalent what do we see? The PMOS transistors incremental equivalent this is v_i this is $g_m \rho$ v_i and that goes into? It is an open circuit that is all, right? That is v_o, right. So, what is the incremental gain? By the way is it $g_m r$ -g_m r?

Student: - g_m r.

- $g_m r$. So, basically the incremental gain is negative infinity, alright.

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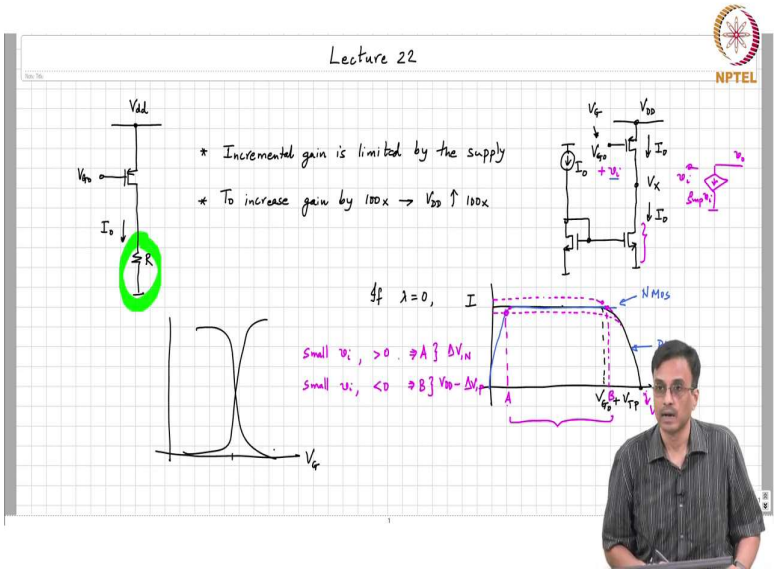

So, therefore, now coming back to where we stopped the previous time. So, if I plot V_G which is the voltage at the gate of the PMOS transistor for a magic value of V_G, the incremental gain will be infinity. What is that magic value? V_{Go}. What is so confusing? Is this clear? Why is it V_{Go}? At operating point V_{Go} the incremental gain is infinite ok. So, how so, will it so, will the curve look like this or will the curve look like that second because this thing is negative infinity, right. So, the incremental gain is negative infinity.

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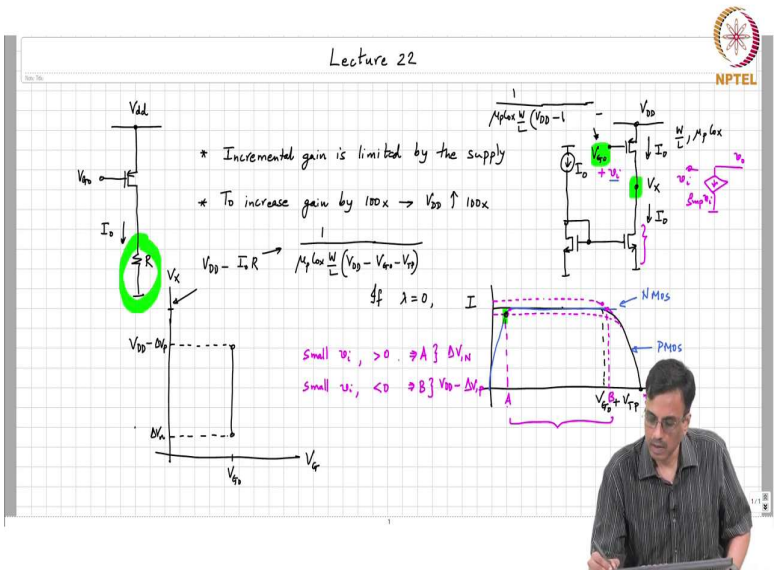

What is this value? This is V_X. This is V_{DD} - ΔV_P, this is ΔV_N, ok. So, beyond this is V_{Go}, for V_G less than V_{Go} how will the characteristic look like, alright. So, but unfortunately the lower current the current pulled by the lower transistor is I_o. So, the PMOS transistor attempts to push more current whereas the NMOS transistor can only sync I_o. So, what comment can you make about the potential of node X?

Student: It will increase.

It will keep increasing until the transistor goes into the linear region, correct. So, for V_{Go} for V_G equal to 0 what comment can you make about the region of operation of the transistor?

Student: Linear.

Linear. So, what comment can you make about the output voltage V_X? That V_X will be when V_G is 0. What region is the transistor operating in?

Student: Linear.

Linear region. I have written $1/(V_{DD} - V_{Go} - V_{TP})$, alright, because deep in triode what comment can you make about? Which term can you neglect? ½ V_{DS}^2, ok. So, alright. So, now, what is the voltage at that point therefore? V_{DD} -I_o R, where R is $1/(\mu_P C_{ox} W/L) (V_{DD} - V_{Go} - V_{TP})$, alright. How will the curve go from there now? What will be the shape of the curve? It will be a straight line V_G by the way is 0 right when V_{Go} is 0, this will be V_{DD} - V_{TP}, alright.

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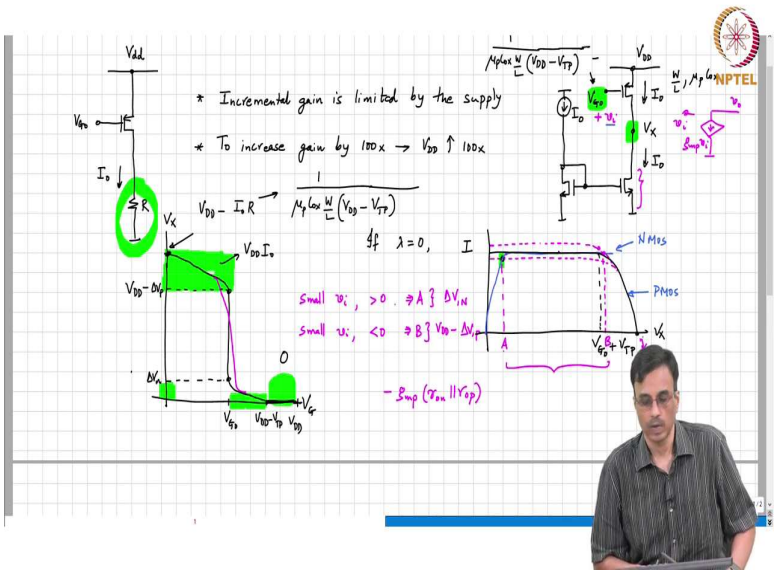

So, when you increase V_{Go} from 0, what will this curve look like? Does it look like something like this, ok and when V_{Go} becomes very very large what happens? When V_{Go} is V_{DD} what happens? The transistor is?

Student: Cut off.

Cut off. So, when will the transistor become alive? So, basically from V_{DD} to V_{DD} - V_{TP}, the output will be 0 ok and it will do something like this, alright. So, if you think of this as a logic circuit what kind of; what kind of behaviour is this? Is an inverter, right, but when the inverter is in the when the input is high the output is 0 right what is the power consumption in that situation when the input is high power is 0, right.

But, I mean if you assume that even this corresponds to a low output you can see that for a part of that characteristic the power consumption is not is not 0, but it is smaller than I_o V_{DD}, correct? Here in this region what comment can you make about the power consumption, when the output is in the logical one state what comment can you make about the participation?

Student: V_{DD}.

So, basically the power dissipated is V_{DD} I_o, ok. So, you can see that even though this shows an inverting characteristic in both logic states there is static participation alright, ok. And this

is the region of interest as far as analog operation is concerned we want that high gain without having to use a high supply voltage ok.

And, what is the peak to peak output swing that is possible without distortion? V_{DD} - ΔV_{TP} -ΔV_A, is that clear? Ok. So, with that the active load discussion is complete in practice of course, what will we have the output resistance of the transistors will not be infinite. So, what comment can you make about any modifications in this curve that we should expect to see when the output resistance is not infinite?

Student: Slope.

Well, the slope is infinite. We will basically have some finite slope things, right and the incremental gain will be - g_m, which g_m? You know the PMOS transistor times $R_{on}//R_{op}$, ok.