Analog Electronic Circuits
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Lecture - 43
Limitations of a Resistive Load

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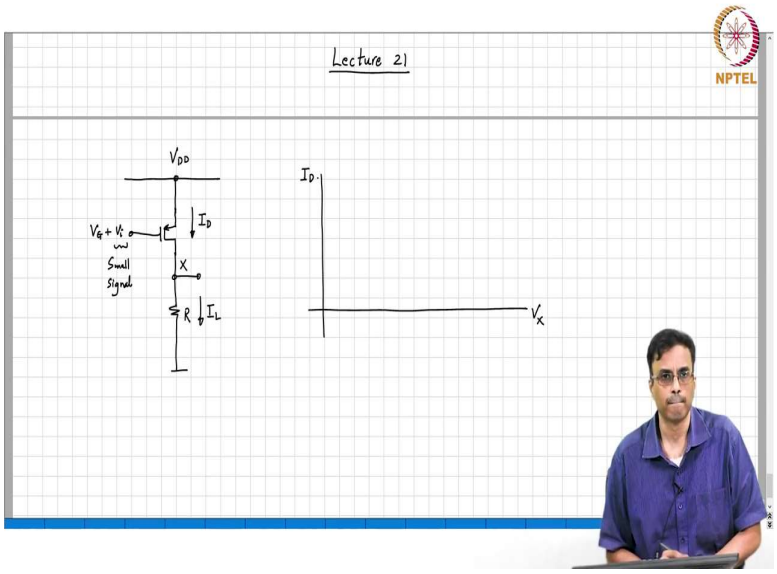

So, in the last class you know we saw an example of how you know NMOS and PMOS transistors can be combined together to build a circuit which you could possibly have built with NMOS transistors themselves, but it would have been a way more messy. We saw a simple four transistor circuit that can be used to generate a bias voltage, a bias current which is such that the trans conductance of the transistor remains constant irrespective of supply voltage as well as temperature right and we derived the circuit from scratch.

So, today we will see you know I mean the rest of the course we basically be using you know NMOS and PMOS transistors together to come up with useful circuits and like in the case with NMOS transistors, the first the simplest amplifier we started off was the common source amplifier.

And likewise in this case also we will start off with the common source amplifier except that we will motivate the reason why this is necessary. I will talk about a common source PMOS transistor and we will go from there. So, remember that eventually we are trying to build

circuits where we are trying to build circuits with negative feedback and the reason for doing that is to make sure that the closed loop gain or the closed loop properties of the system are largely independent of the properties of the transistor.

And the way this is possible is by making the forward path gain as large as possible right, ideally infinity of course, you know you can only you know get close you cannot make it exactly I mean you cannot make it infinite. Now, that basically means that the gains of the individual stages must be as large as possible right.

Finally, you want to get gain and of all the four amplifiers that we have seen right the common source, the common gate, the common drain and the trans impedance amplifier the candidate which allows you to have the largest incremental gain is the common source amplifier right. So, we would like to see how much gain you can get out of a common source amplifier. So, to see that you know as I said you know a picture is worth 1000 words and since we were talking about PMOS transistors let us do it with PMOS transistors the same discussion would have been valid with NMOS transistors too, but you know we since we just started off with PMOS devices it helps to get some more intuition you know on how they work. So, I will discuss this with PMOS transistors.

So, let us consider a common source PMOS amplifier. So, the gate is biased at some V_G right let us not worry about how that bias came about. It could be a resistor string, it could be something else and there is $V_G + V_i$ voltage and this is some R. So, as they say you know a picture is worth 1000 words. So, if we want to find the I mean V_i is a small signal or an increment.

So, first things first. If we have to find the operating point at the output let us call that node X which is also the drain potential of the PMOS transistor. How will we do it? If you want to find it graphically, what will we do? So, basically the idea is to say we know that at the operating point the drain current must be exactly the same as that flowing through the source, but drain current must be the same as that flowing through the resistor right. So, what should I do to get the operating point? I will plot I_D as a function of V_X that is what I need to correct and I will plot I_L as a function of V_X. The place where the two intersect gives me the I will plot I_D versus I mean we know that I_D must be equal to I_L. So, I will plot I_D as a function of V_X and I_L as a function of V_X and you know the two curves will intersect at a point the X my coordinate corresponding to that point of intersection will give me the operating point

operating voltage V_X alright. So, let us now plot your I_D as a function of V_X, when V_X is 0 what is the region of operation of the transistor?

The transistor is operating deep in saturation because the drain potential is way below the gate potential right. So, what will be the so, what will be the current in the transistor? How will we find that current?

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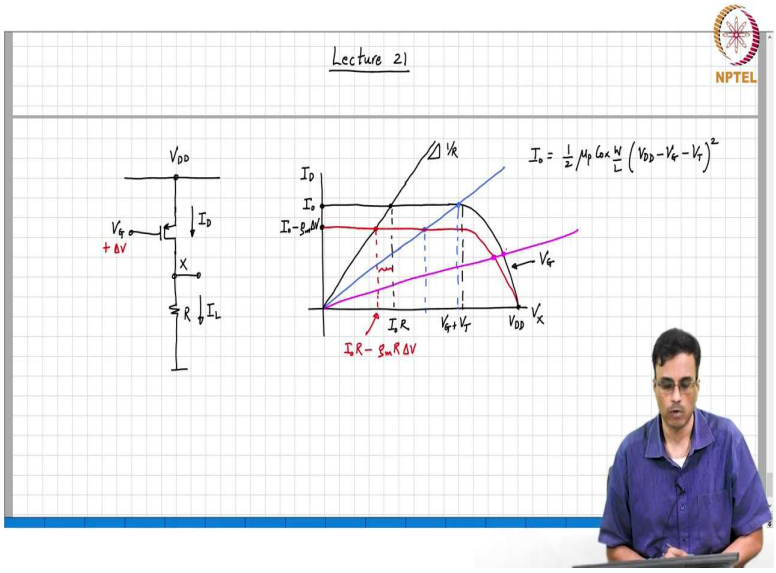

Let me not confuse you by adding V_i. So, let us say this is V_G ok. So, how will we find the current in the transistor? What is I_D when V_X is 0? So, I_o is nothing but half $\mu_p C_{ox}$ W/L V_{GS}, which is $(V_{DD} - V_G - V_{TP})^2$. So, let us call that I_o that is I_o there ok. So, I will go on increasing V_X and what will happen to the current I_D? It will remain constant as long as the transistor stays in the saturation region. At some point what will happen? As V_X becomes larger and larger the transistor will go into the triode region. So, at what value of V_X will the transistor go into the triode region? Very good, $V_G + V_T$, and beyond that what happens? The transistor goes into the linear region. So, what happens to the current? Current drops and eventually it will become 0 when? At what point at what V_X at what V_X will the current drop to 0?

Student: V_{DD}.

When V_{DD} when the current is 0 what is the region of operation of the transistor? It's operating the linear region right, why is it not cut off as he claimed earlier? V_{DD} - V_G is greater than V_T. So, the transistor has not been cut off just because the current is 0 does not

necessarily mean that the transistor is cut off it could be in the triode region right. So, the transistor is indeed operating in the triode region except that the V_{DS} is 0 and therefore, the current is 0 alright. So, the next job is to plot I_L versus V_X ok. So, what will that picture look like? It will be a straight line passing through the origin and what is the slope?

1/R alright. So, what is the operating point? Yeah, the point of intersection that the slope is 1/R. The y axis of the point of the y coordinate of the point of intersection is what?

Student: I_o.

So, now let us solve this challenging mathematical problem and tell me what the X coordinate is I_oR. You would have said what the hell is this. I mean yeah I would have told you this without drawing all these pictures right that is indeed right, but you know it will give us some intuition just hold on a second alright. Now, to see what the incremental gain of the transistor is and again we could have calculated using the formula, but we will know as they say a picture is worth a 1000 words. So, we will draw the picture.

So, if I increase the gate voltage by a small amount ΔV right what happens to and I mean by incremental gain we would like to see what we would like to see is the change in the drain voltage due to a change in the gate voltage that is what incremental gain means correct. So, if I increase the gate voltage by ΔV to find the new potential at the drain what should we do? If you want to look at it on this graph what should we do? This curve corresponds to the gate voltage being V_G. What should we draw now?

We need to draw another curve corresponding to $V_G + \Delta V$ ok. So, the gate voltage is increased by ΔV. So, what comment can you make about how the current has decreased. So, how much has it decreased by assuming it's a small signal, it is reduced by $g_m \Delta v$ ok. So, again I know what happens. So, this characteristic will look like this and again it will fall off when the voltage reaches $V_G + \Delta V + V_T$ ok. So, this is nothing but $I_o - g_m \Delta V$. Let me use another colour.

What now, what is the new operating point therefore? So, that is this point of intersection and that is nothing but $I_o R$. Well that distance is nothing but $g_m \Delta V$. So, the output voltage is $g_m R \Delta V$. The voltage is shifted by that much, correct? Is this clear and this is telling you two things? It is telling you that when you increase the gate voltage, the drain potential is decreasing by how much? $g_m R \Delta V$. I mean it is all stuff you know correct alright.

So, for a given ΔV if you want more incremental gain then what comment can you make then that basically means, if you have more incremental gain that basically means that that distance must increase, is this clear?

Student: Yes.

Alright. So, with this background how will you increase the incremental gain if you want to keep V_G and the transistor the same? If you increase R what happens? Well. You now have a curve for the load which looks like this and as you can see visually as you keep increasing R what comment can you make? The change in the drain potential due to the same change in the gate voltage ΔV is increasing, is that clear? alright. Now, if you get two greedy what happens? You are saying well if I had R, I had some gain, I increased R, I got more gain. So what if I increase even more the transistor will go into the linear region and you end up with this situation there right where as you can see visually the transistor is going into the triode region right and you see that the gain incremental gain has reduced alright, ok So, now. So, as you can see the best bet for you is to make the resistor large enough, so that the transistor is operating at the edge of saturation, alright ok.

Now, given this and if you want to keep the drain current the same right remember I mean I am not constraining V_{DD} I am not constraining V_G, but I only want to make sure that the drain current remains the same if I want to increase the incremental gain what do you recommend that we do? Let us say we are already operating on the blue curve. So, we have the maximum gain that is possible with this V_{DD}. If I want to increase the gain further while making sure that the quiescent current in the transistor remains the same, what choice do I have? The transistor is the same, the quiescent current is the same. So, the g_m is the same. So, that is not a choice.

Now what can you do to this circuit? So, that the incremental gain can be increased beyond what we have right now which is assumed to be the blue curve right R is chosen to be I mean let us assume that R is such that we are operating with the blue curve is that clear? Alright I do not want I_o to change. So, and consequently g_m to change. So, that remains fixed. If I want to increase the gain, what can I do? Increase. If I increase V_{DD} and V_G both by the same amount what happens?

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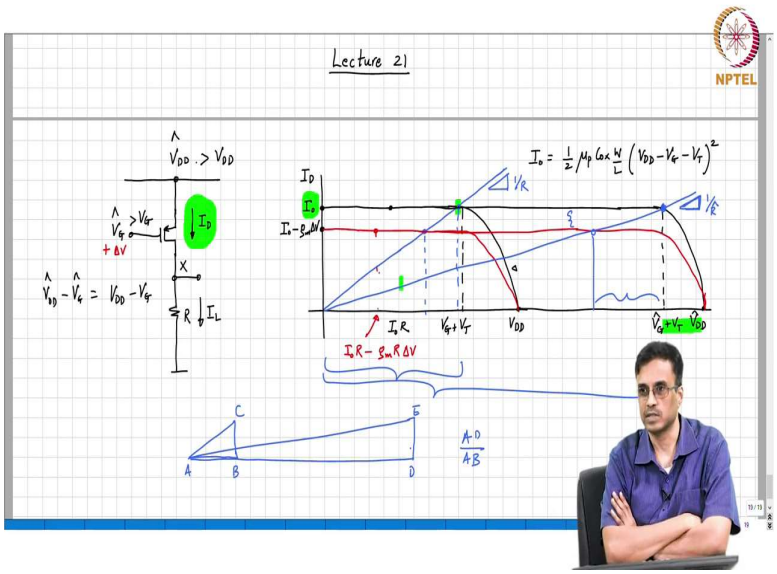

So, therefore, now let us say the new V_{DD} is $\hat{V}_{DD}$ which is greater than V_{DD} and the new V_G is $\hat{V}_G$ which is greater than V_G. So, that $\hat{V}_{DD}$ - $\hat{V}_G$ is the same as V_{DD} - V_G in other words we increase V_{DD} and increase V_G by the same amount. So, what happens now? What happens to this picture? The curve will basically now if we increase, I am going to exaggerate here and increase V_{DD} by a really large amount. So, let us say I double it. So, this is $\hat{V}_{DD}$. So, what happens to the curve now? What happens to the black curve?

This stretches and does that right. So, this is for V_G what happens to the red curve now? It will also stretch and this guy here is $\hat{V}_G$ + V_T alright. So, we have increased the V_{DD} and V_G by the same amount now. What should we do? You increase the resistance right. So, if you increase the resistance what happens? This is the new resistance and as you can see what comment can you make about the incremental gain? It will increase. So, with this transistor having this g_m the only way of getting larger incremental gain with a resistive load is to increase the supply voltage and increase the gate voltage by the same amount. So, the transistor still carries the same current, but you increase the resistance. So, that even with the I mean now with the increased V_{DD} you are operating now at the edge of the saturation region. So, then you will be able to get the maximum possible gain with this new V_{DD} correct and that maximum will be much larger than the maximum gain you could get earlier. Is this clear so far?

Student: Yes.

Alright. So, now using this strategy if I have to increase the gain by a factor of 10 right approximately, how much would the V_{DD} have to increase by? So, in other words originally, we had some V_{DD} we had some maximum incremental gain correct. Now, if I wanted to increase the incremental gain by a factor of 10 look at the picture approximately and tell me how much must V_{DD} increase by?

So, if you assume that V_{GS} is very small compared to V_{DD} alright a V_{SG} is very small compared to V_{DD} what does that mean? That this is very small compared to that alright. So, using that approximation what comment can you make if you wanted 10 times the gain? If I have to increase the gain of a by a factor of 10 what comment can you make about the slope of the new blue line? 1/10. So, what comment can you make about this distance in relation to this distance? 10 times. If this is very small compared to V_{DD} and $\hat{V}_{DD}$ What comment can you make about the new V_{DD}? Roughly 10 times. Is this clear or not? So, what do I mean? With this line we have some incremental gain correct. Now, we want to get 10 times the incremental gain. So, what should we do? We increase V_{DD} to some large value $\hat{V}_{DD}$ right. Now, this incremental gain is increased by a factor of 10. What comment can you make about this slope versus that slope?

This distance is the same incremental gain is basically this distance and that has increased by a factor of 10. What comment can you make about the slope of the second blue line? It will be 10 times smaller, correct. So, if the slope of this blue line let us call this you know 1/R and this is $1/\hat{R}$, the slope of that second blue line is 10 x smaller than the first blue line. Is that clear or is it not clear ok. Now, what comment can you therefore make about this distance versus this distance? Ok let us have a triangle ok. There is now high school algebra. You have a triangle with some slope.

Now, you have a say triangle with a slope which is 10 times smaller. I am asking you if I call this a triangle A B C and I call this triangle A D E. What the question I am asking you is what is AD/AB. BC/AB tan inverse actually, but it's fine. The slope of the second line is AE, and BC and DE are the same. I am telling you that the slope of AC is 10 times higher than the slope of AE alright. So, now I am asking you what is AD by AB? So, AD is 10 times you understand this much ok.

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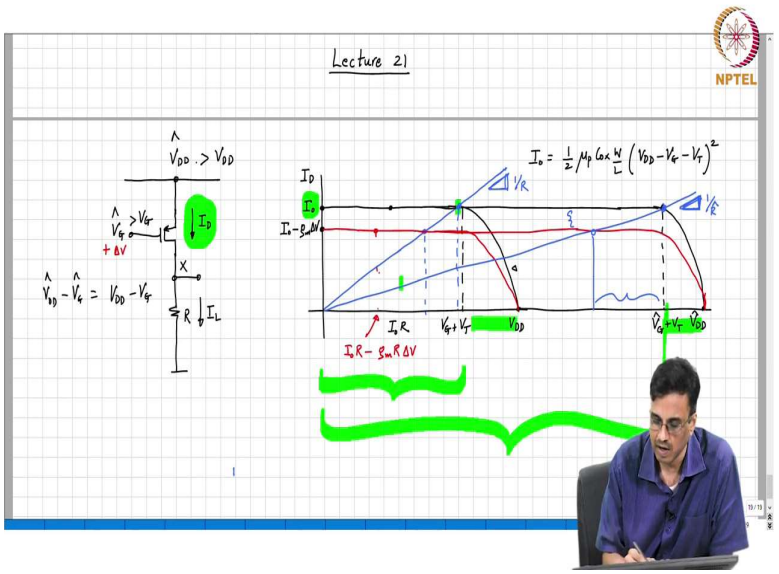

Now, with this background now tell me this slope is 1/R this slope is $1/\hat{R}$ which is which I tell you is one tenth the slope of the first blue line right. It is obviously, these two heights are the same. So, I am asking you the question: what is the ratio of that to that?

Student: It will be 10 times.

It will be 10 times more clear? Alright. Now, if this is very small compared to this distance then you can neglect those small extras and you can roughly say that if you want to increase the gain by a factor of 10 if you want to increase the incremental gain by a factor of 10 while keeping the quiescent current the same then the only way to do it if you want to have a resistive load is to increase the V_{DD} by a factor of 10 alright. Now, if you want to increase the gain by a factor of 100. You need to increase the V_{DD} by a factor of 100, correct. So, basically as you can see, this is a pretty impractical thing to do.

So, if you had a gain of you know if your common source amplifier had a gain of 10 and you wanted to increase it to say 100 ok and if the original supply voltage was 2 volts, you need 20 volts supply to be able to get an incremental gain of 100 if you use a resistive load. And if you want gain enough we just 1000 times larger, this $\hat{V}_{DD}$ will have to go into large. So, you see the problem and this is a terribly power enough and if not at all efficient from a powerpoint of view because the power you will be dissipating is $\hat{V}_{DD}$ I_L.