Analog Electronic Circuits - IITM
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Lecture - 41
Basic Building Blocks with PMOS Devices

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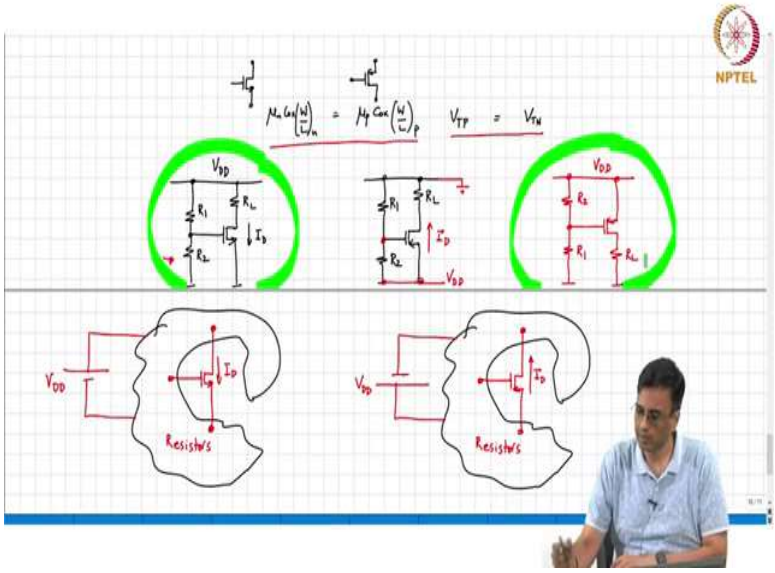

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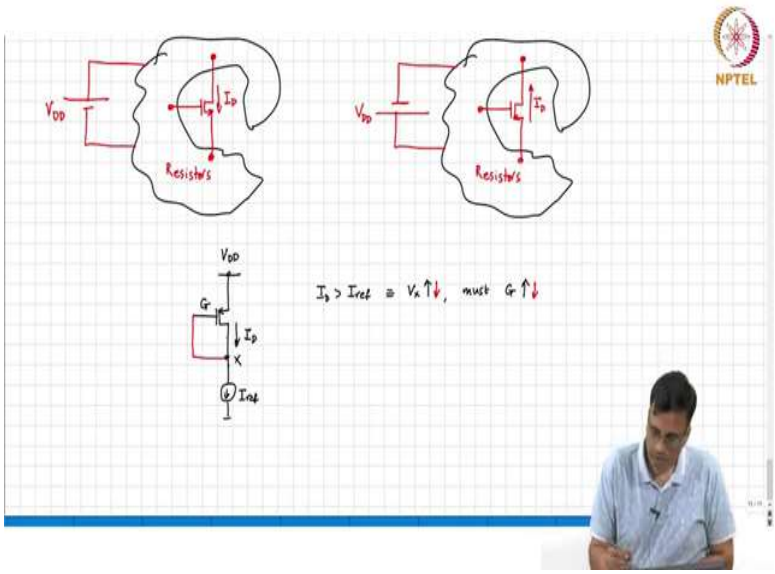

Now, let us run through this basic circuit. So, what is the problem with this common source amplifier the way we biased it? So, this resistive biasing of the gate has problems you know

in the PMOS case just like it does in the NMOS case. So, again we need to basically make sure that you know we use what we do to fix this problem in the NMOS case? We use negative feedback and we are going to do the same thing with PMOS, but the change is that you are going to tell me what we are going to do now.

So, alright. So, the first bias technique was to remember that the PMOS drain current is controlled by the source gate voltage and like in the NMOS transistor, the current can be measured in either the source or the drain. So, say you know not surprisingly you have the same bias techniques that we used in the NMOS case we will apply for the PMOS.

So, the first thing there was we had the grounded in the NMOS case remember we had grounded the gate, we varied V_{GS} by keeping the source fixed vary the gate potential and the first technique measured the current in the drain, right. So, here what do we do? The source must be? The source must be connected to the highest potential V_{DD}, alright and we compare the drain current with a reference current, right and go and kick the gate voltage in the right direction so as to make sure that the drain current is the same as the reference current, correct alright. So, I am not going to write out all that long you know text in words. Now, you should be able to tell me you know so, this is the drain current. We want to compare it to the reference current. So, does the reference current go up or go down?

This is I_{ref} and this node potential X, if I_D is greater than I_{ref} it means so, I_D is greater than I_{ref} is equivalent to saying V_X goes up which means which means what? Which means the gate potential is too high or too low?

Student: Too low.

The drain current is too high, correct? That means, the V_{SG} is too large, but the source is fixed. So, it means that the gate potential is too low. So, the gate potential must go up. So, if V_X goes up you must increase the gate potential, correct and so, if V_X goes down G also must go down, ok. So, what should you do now?

You connect the gate and the drain just like we did before, alright. And so, this is the first way of stabilizing the current bias. So, I mean bias current in the PMOS case then we can use the same potential to other PMOS transistors.

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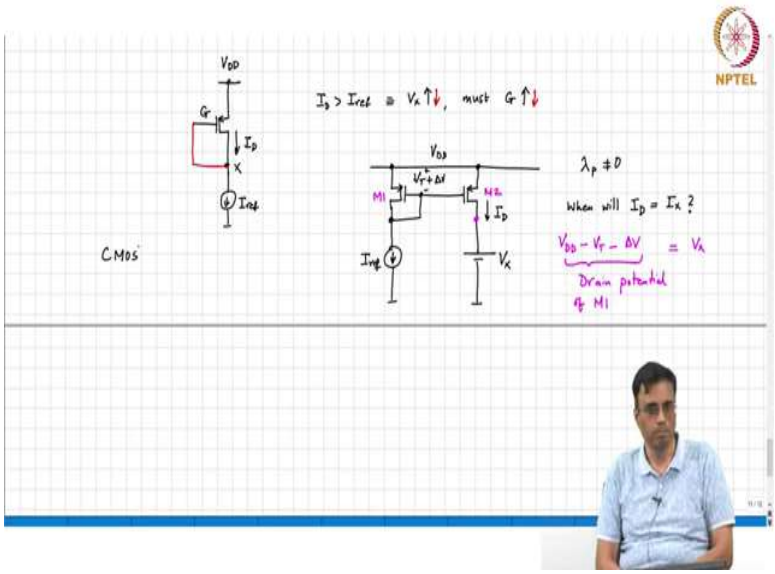

So, this is I_{ref}, this is if lambda is 0 the current will be the same as I_{ref}. if lambda is not 0 then there will be an I_{ref}. So, let us say this is V_X and this voltage is the source gate voltage. Let us call that V_T plus ΔV, alright. So, for what V_X will the current be exactly equal to I_{ref} lambda. lambda V_o equal to 0? When will I_D be exactly equal to I_X? So, that will be only the two will be exactly the same when the drain potential of the PMOS transistors on the right, that is basically M2 is exactly the same as the drain potential of M1. The drain potential of M1 is V_T + ΔV. So, that basically means that what is the potential of what is the drain potential of M1 that is nothing but V_{DD} - V_T - ΔV which is the drain potential of M1 and this must be exactly equal to V_X.

And how do we go and fix you know what do we do to fix the out I mean another problem with this basic current mirror is the output resistance. What is the output resistance?

Student: R_o.

So, what do we do to fix this problem? We connect the CCCS in and all that stuff right, ok. But as you can see this I_D is now pushing current down, right. So, it is actually a current source whereas, the NMOS transistor is pulling current towards ground so, it is a current sink, alright. So, the fact that you have NMOS and PMOS transistors on the same chip lead to what is called CMOS technology and the C stands for complement, right.

And the reason why complementary nature devices help a lot is because you can do things with NMOS and PMOS transistors together which you could not do with a single kind of transistor alone alright, ok.

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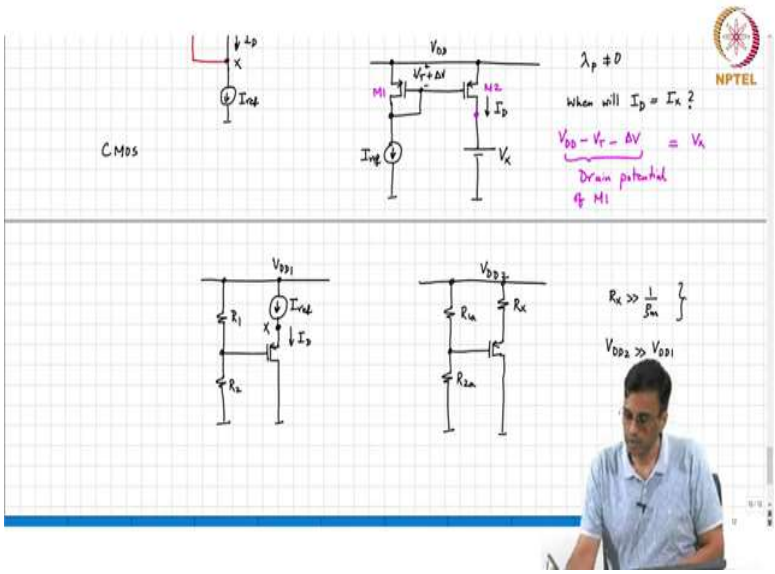

So, the next bias stabilization technique is one where what did we do the second time around. The gate was fixed in the NMOS case, what did we do? The gate was fixed. We varied the gate source voltage. We measured current in the source and varied the source voltage to go and control the current. So, we will do the same thing here. The gate potential is fixed alright and the drain is some low potential. So, we need to compare the current in the source with a reference current and kick the source in the right direction. So, what do we do?

Very good. So, basically very straightforward you put a current source like that and then so, let us call this R_1 and R_2. So, you monitor the potential of this node X. So, if I_{ref} is greater than I_D. V_X will tend to increase, but if I_{ref} is greater than I_D it means that V_X was too the source potential was too small in the first place, correct? And, therefore, you know just the act of connecting that I_{ref} in the source as shown here automatically ensures that V_X will move in the right direction so as to keep I_D equal to I_{ref}, right.

We have seen all of this in the NMOS class, it is a repetition right, but I think it is good to have repetition, alright. And, of course, you know on an IC it is straightforward to make a current source, alright. So, what comment can you make about if you are working with a

discrete circuit and you have discrete components a current source may not be that easy. What do you do then?

What do you do in the NMOS case? Ok. You can pull out some more keywords and then form a sentence and throw it at me. I think you are not listening to the question. The question is if you are making an IC then the current source is ok because it will need a transistor, right and on an IC transistor they are free, ok.

But if you are working with a discrete board where transistors are expensive, what did we do in the NMOS case? This is what I am saying. You know throw all keywords that you have learnt inductor, capacitor, voltage source current control current source. You put a large resistor, right and it is understood that if you put a large resistor what is the meaning of large resistor? If this has to work well and the suggestion is to put a large resistor what is the meaning of large? R_X must be much much larger than $1/g_m$, ok. And, if you still follow the line of thought that will be only possible if R_X is very large right then the drop across R_X also will become large and therefore, it has to be accompanied by an increased supply voltage, right. And, these resistors will also be different, ok so, as to provide the appropriate gate source voltage.

So, V_{DD2} must be much larger than V_{DD1} and that is the penalty you pay for not having a current source, right? So, in the limit that R_X will tend to infinity the V_{DD2} will also tend to infinity and that is when you get you know a true current source behaviour. But, you know, but the insensitivity with respect to changes in the supply etcetera will all depend on this quantity g_mR_X ok, alright. Then what is the third?

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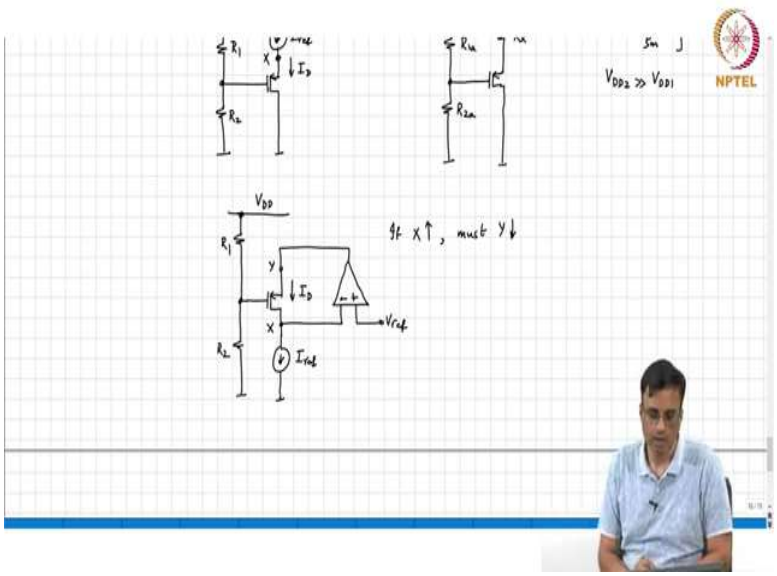

What was the third way of stabilizing the bias? Measure the drain. Let us do that. Now, you know the drain the gate is fixed. So, this is V_{DD} some R_1 some R_2 you measure the current in the drain and vary the source. So, what do you do, what do we do? So, what should I do? Current source and drain is the current source I_{ref} flowing downwards or upwards? Downwards, very good, and this is the potential to node X, if X goes up?

Student: I_D will get into I_{ref}.

It means if I call that Y, if X goes up it means that the drain current I_D is greater than I_{ref}. So, are the source gate voltages too much or too little?

Student: Too much.

Too much, correct. So it should be brought down. So, and vice versa. So, alright the only way I_D will be exactly equal to I_{ref} is when the potential of node X is constant, right. So, basically you compare the potential of node X to a constant V_{ref} and use an op-amp to go and kick Y in the right direction, ok. What might be the signs of the op amp? Minus and plus, ok. Now, to make it a common source amplifier it is very straightforward, the same volt, same volt, right whatever we did with the NMOS case you can do with the PMOS case and the last thing was what?

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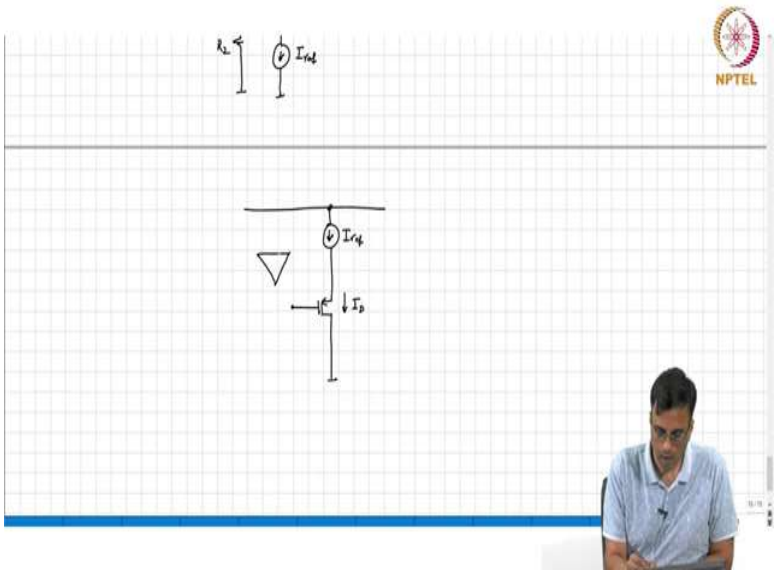

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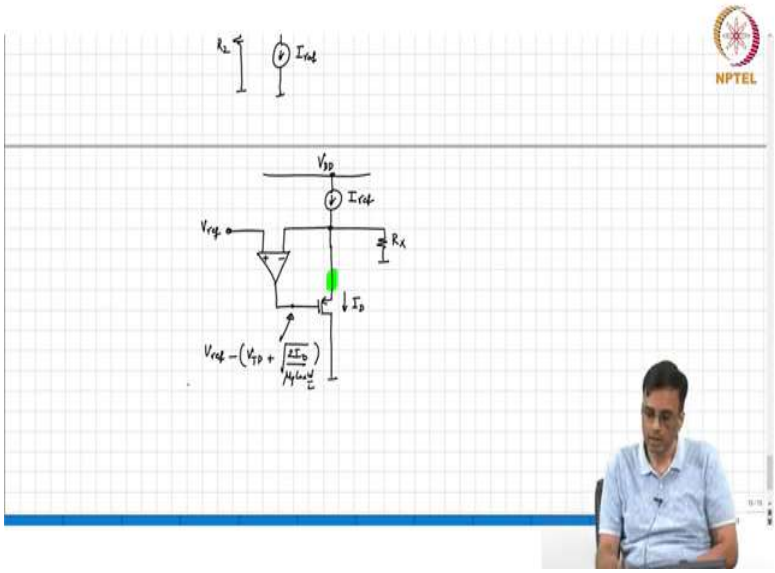

We measured current in the source ok, this is I_{ref} and drain is fixed, what do we do? This is I_D you want to fix the gate potential. So, what do you do? You compare. Ok. You compare it to the constant and go and kick gate voltage in the right direction and what must be the signs on the op-amp? Plus at V_{ref}. Minus at this point, ok. So, what if this is I_D, what is the potential of that transistor at the gate? What is the potential of the gate? What is the V_s?

$$V_s = V_{ref} - \left(V_{TP} + \sqrt{\frac{2I_D}{\mu_P C_{ox} \frac{W}{L}}} \right)$$

This is I_{ref}. So, this is I_{ref}. I_D is equal to I_{ref}. So, that is fine ok. Now, question for you, if I add a resistor there R_X what comment can you make about the current through the transistor? What is the current through the transistor?

Student: I_{ref} - V_{ref}/R_X.

Very good. So, I_{ref} - V_{ref}/R_X, ok. But, the gate will do this therefore, will the current decrease or increase?

Student: Increase.

Yeah, here decrease here increase? It will reduce and the gate potential will still be this formula because we use I_D in the formula not I_{ref}. Does it make sense?

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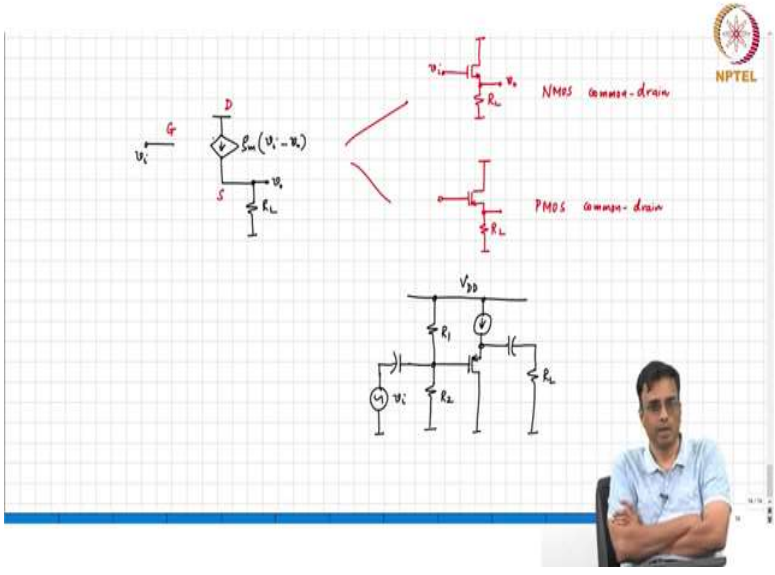

Alright, that covers the biasing of all the PMOS transistors. The next thing is to build the 4 controlled sources. Again, it is the same volt, same volt it is nothing new. So, let us just finish this and wind up. So, the incremental voltage controlled voltage source that was in the NMOS case I mean we went through the whole thought process. I am not going to go through it again. This is R_L this is v_i and this is g_m v_i - v_o and what should the g_m be?

Student: Infinite.

Ideally infinite in practice is very large and what is that very large? g_m must be much much larger than $1/R_L$ and what did we then say that we identified this is the gate, this is the drain. This is the source, correct and then we said that one way of realizing it was what we did earlier. This is the incremental circuit we identified as the transistor, this is R_L, this is v_o, this is v_i, but remember that the incremental circuit of the PMOS transistor is the same as that of the NMOS transistor. So, there is no reason to identify that transistor is being only PMOS, I mean only NMOS it could be. You could think of it as being a PMOS transistor, alright. So, this is the NMOS common drain amplifier, what is this? This is the PMOS common drain amplifier, ok and again you know whether the NMOS or PMOS the g_m R_L must be much much larger than 1, ok. So, the only detail that changes is how you bias the transistor, right.

For example, in this case I again am not going to cover this for this circuit. So, here is one way I mean we have already seen how to bias the PMOS transistor. So, for example, this is V_{DD}, this is R_1, this is R_2, alright. So, how do we do what we do with respect to the input?

Student: Capacitor and input.

Capacitor and input source v_i, similarly low, ok. So, this is an example of a PMOS common drain amplifier. So, this is basically as you can see there is nothing fundamentally new here, right. Once we understand, I mean once we get used to these circuits to the PMOS transistor, it is just the same repeat of the NMOS devices.

And, just like how you cannot make an incremental CCVS with a grain with a gain greater than 1 in the NMOS case, what is the reason? It is not a 4-terminal you know voltage controlled current source. It is a 3-terminal one which constraints the kind of circuits that you can build and likewise with the PMOS device.

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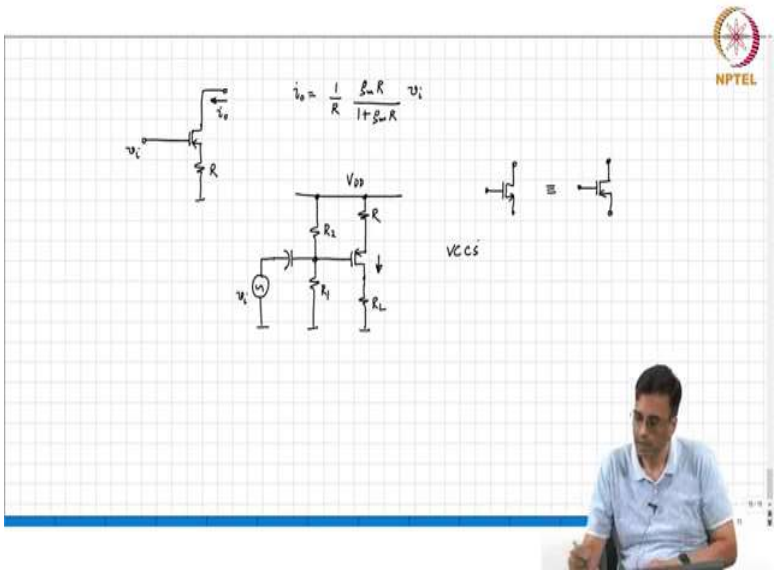

Now, input output, input impedance, output impedance, gain, etcetera are all expressions that we have seen earlier. There is nothing really new. Then is the voltage controlled current source. Again, now I want to dispense with even drawing the g_m. So, this is R, this is v_i, this is i_o. What is i_o in terms of v_i? Incrementally if g_m tends to infinity. If g_m tends to infinity this tends to (1/R) v_i, right? If g_m does not tend to infinity, then this expression is right. Now, if you want to build this with PMOS transistors what will you do?

I mean the incremental circuit nothing is to be done other than. No, no changing drain and source. It is just changing the direction of the arrow in the source, right. Remember the incremental I mean model of the NMOS and the PMOS are exactly the same. So, as far as the incremental circuit is concerned, if you had a device like this in the incremental equivalent ok, it is exactly going to be the same assuming the transistor PMOS transistor is biased properly whether you have this or that is immaterial, ok.

So, now how are you going to bias the device now? Yeah, choose your favourite scheme and again let us say this is V_{DD} this is R_2, this is R_1, this is v_i let us say this is R_L what is the incremental current going in there? Yeah, it is the same thing i_o is (1/R) g_m R/(1 +g_m R). Is that clear? Ok. So, that is the incremental current controlled sorry voltage controlled current source and again the expressions for output impedance input impedance you know gain etcetera etcetera are all the same. There is no point in re-deriving all of that all over again.

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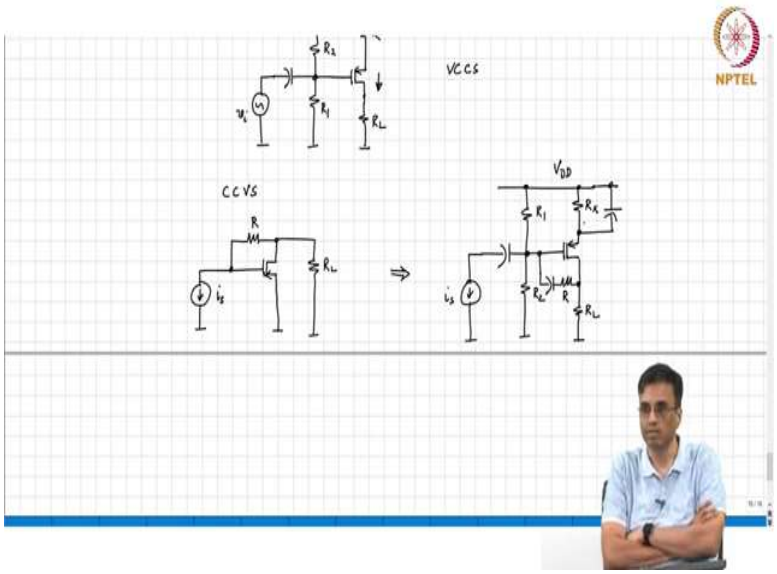

The next one is the current controlled voltage source and again, I am going to dispense with all the discussion. In the NMOS case this is what we had, ok. This is i_s then what happens now? What do we do? In the PMOS case the incremental diagram remains the same. So, all that we need to do is, think of this as a PMOS transistor rather than an NMOS one. You bias up your transistor your favourite way again I am going to pick something. Let us say I pick for a change I put a large resistor in the source, ok. So, this is my bias circuit. So, tell me what all I should do to make this look like the circuit on the left for incremental signals?

Say some resist R_1 R_2. Yeah, what should I do? As the input source, connect the gate and drain. Yeah, this is the large capacitance in series, if you do not want to disturb the operating point, ok. What else? That is R_L, ok. What else? We need the source to be incrementally grounded by the current capacitor, alright. And as you can see this is pretty much, I mean any of these circuits you can take you could have done what we had discussed earlier, namely you take the NMOS circuit you replace V_{DD} with $-V_{DD}$; replace the NMOS transistor with the PMOS transistor.

Add V_{DD} to all nodes and flip the circuit upside down that will give you the same circuit that we have got here, alright. And, so, this is the trans impedance amplifier and as g_m tends to infinity the trans impedance tends to 1/R, the input impedance tends to 0 the output impedance tends to 0, alright.

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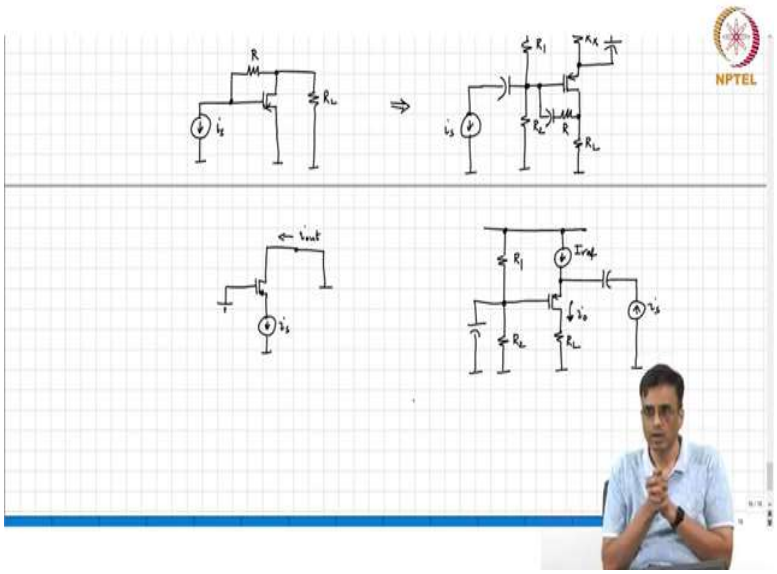

So, the last controlled source is the current controlled current source which was the common gate amplifier, i_{out}, i_s and again same volt, same volt what do we do? Replace i_s ok and again bias the transistor properly for example, like this. So, I_{ref} i_s some R_L here and this incremental current is i_o which is the same as i_s and the gate must be grounded by putting the large capacitor here. So, today we have completed basically we have gone through all that we have done with NMOS transistors we have repeated action replay with PMOS transistors. So, with this you know we are now ready to put we are now in a position now that we understand that PMOS transistors you know how they work it is just a minor change in the mode of operation. But, otherwise fundamentally it is the same set of equations you know similar in fact, the same small signal equivalent everything is pretty much the same.

So, now we should start exploiting the complementary nature of NMOS and PMOS transistors and start to see how we can put these two together to do things that were not possible with a single type of transistor, alright. So, we will start doing that in the next class.