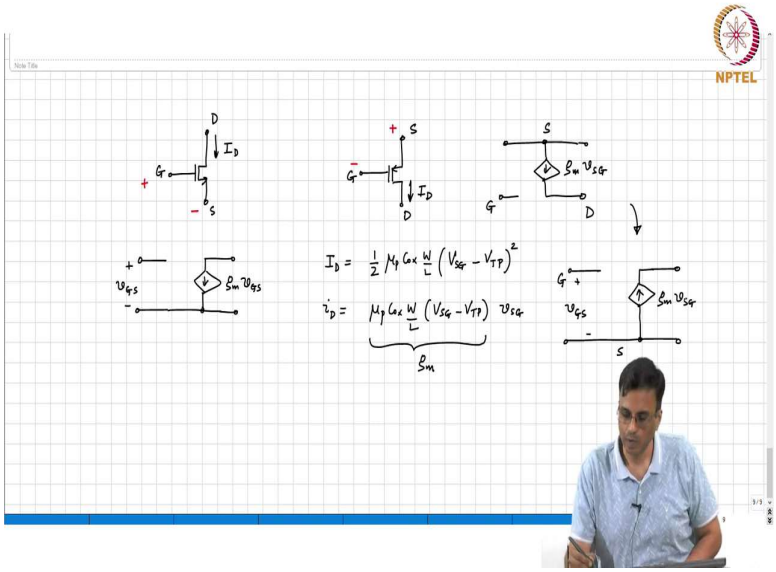
Analog Electronic Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 40
Small-Signal Model and Bias Stabilization

(Refer Slide Time: 00:18)



And so, the first thing we did when we saw the NMOS transistor was draw its, small signal equivalent and that was and this is $g_m V_{GS}$. Now, the question is what do we do with the PMOS? Alright. So, remember the PMOS the drain current is I_D is nothing but in saturation is

$$I_D = \tfrac{1}{2} \mu_P C_{ox} W/L(V_{SG} - V_{TP})^2.$$

Let us assume the transistor is operating in saturation correct. So, what is the change in I_D? So, therefore, i_D is the drain current which is nothing but,

$$i_D = \mu_P C_{ox} W/L(V_{SG} - V_{TP}) V_{SG}$$

Is going out of the drain right. So, the small signal model therefore, will if you want to do it this way will basically look like this. So, this is the source, this is the gate, this is the drain correct? Is this clear people? And what is the value that controlled source?

It is if you call this the incremental g_m like we did in the NMOS case, what is that current source?

Student: $g_m V_{SG}$.

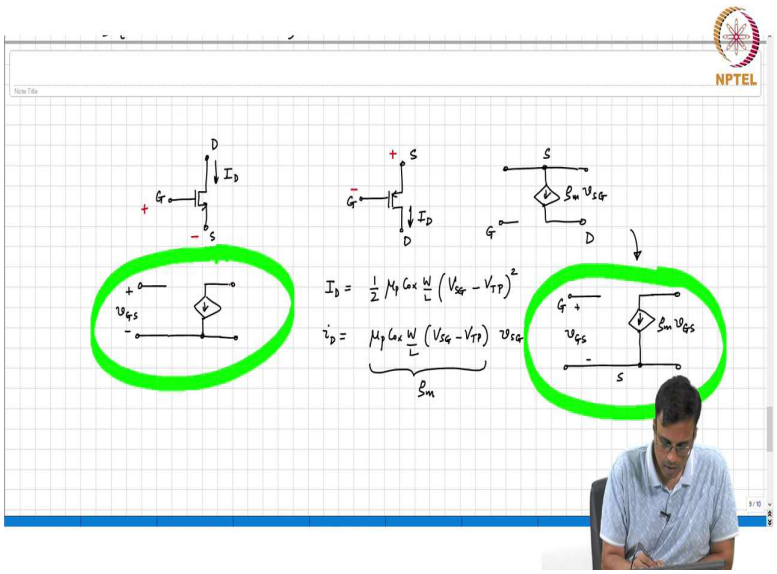
So, now what can you now it is kind of a bit you know strange that the you know remember that in the increment in the absolute circuit the absolute voltage of the source in the PMOS transistor must be will be higher than the drain. But when we for instance when we make a common source amplifier the source is going to be going to be you know at a constant potential right. In the NMOS case that constant potential happen to be ground in the PMOS case, it will be the highest potential which will be V_{DD}. So, in the incremental circuit what happens to the source?

In the incremental circuit the source is grounded again, correct? And again, we end up with this awkward situation where the ground is sitting on top and all the voltages which in the incremental circuit are sitting below ground, right? Physically they will say sitting below ground even though they may be positive with respect to ground in the incremental circuit, right?

To solve the problem what do we do? You flip the whole thing again and therefore, and express the incremental current in terms of V_{GS} again right. And what happens to the current? If I call this V_{GS} what should I do to that current source?

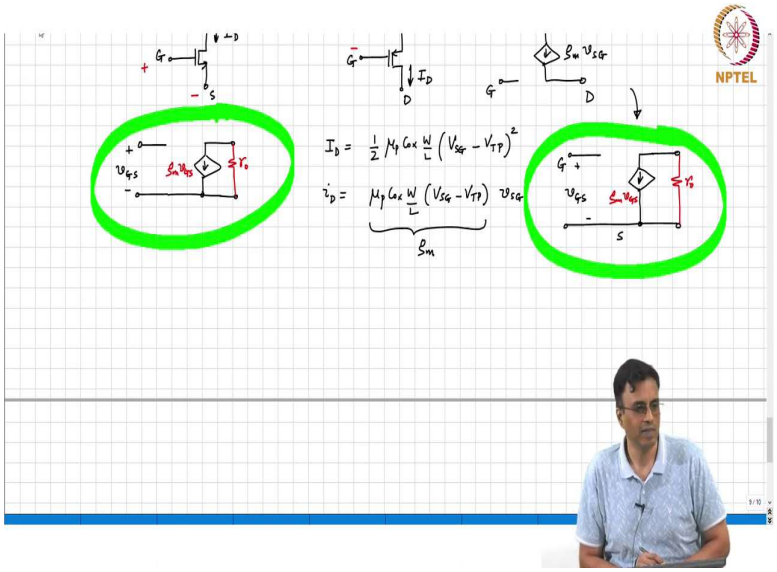
What will this be? When we turn it upside down the current was like this and this was $g_m V_{SG}$. So, now in terms of V_{GS} what will it be?

(Refer Slide Time: 05:22)



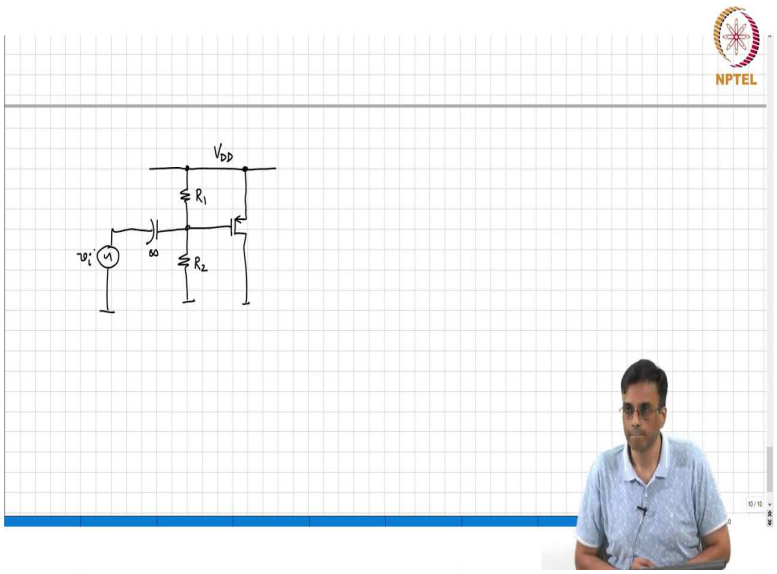
Well, we basically say it is a we keep that call that g_m V_{GS}. Does it make sense people? So, what do we conclude therefore? The incremental model for the NMOS or the PMOS transistors are identical. So, this so that I mean once you draw the once you bias the transistors are properly whether you use an NMOS transistor or I mean or a PMOS transistor the incremental circuit remains the same is that clear? Ok. Now, and of course, you know just like how an NMOS transistors got finite output resistance the PMOS transistor also has got finite output resistance.

(Refer Slide Time: 06:29)



The consequence of that we already saw it was to simply add an output resistance r_o. This is $g_m V_{GS}$ and similarly this is r_o this is $g_m V_{GS}$. Does it make sense? Ok. Now, that we have seen the basic what do you call incremental equivalent circuit; I mean we start making amplifiers like we did in the NMOS case. Let us start with the simplest one that is basically the common source amplifier.

(Refer Slide Time: 07:22)



So, how will we how what is the first bias technique that we use to generate the common source amplifier?

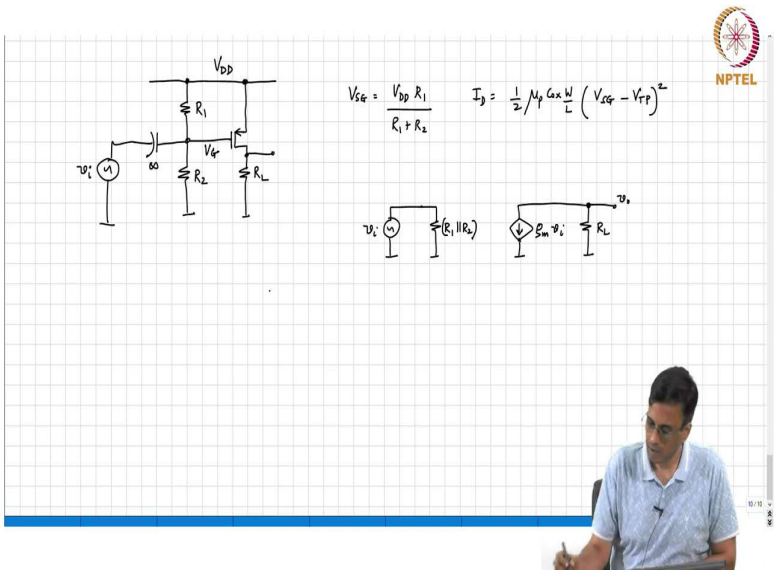
Student: Resistor divider.

So, basically with PMOS circuits often you know the all the sources are connected to the topmost rail right and if you call that V_{DD} and now what is the source gate voltage? What is the source gate voltage? V_{DD} R_1 /(R_1 +R_2). And so, as long as that is greater than V_T you will have some current flowing and therefore, you can have some you will have some trans conductance correct. Now, what comment can you make about now if you want to make a common source amplifier what all should we do?

So, again same volt. That is the input voltage ok. What about the load now?

Student: We can directly put drain.

(Refer Slide Time: 09:19)



We can put in the drain directly. If you are concerned about DC current flowing through the load then you can as usual couple it to the capacitor. And so, the. So, $V_G = V_{DD} R_2 /(R_1 + R_2)$. So, $V_{SG} = V_{DD} R_1 /(R_1 + R_2)$. I_D therefore, is nothing but,

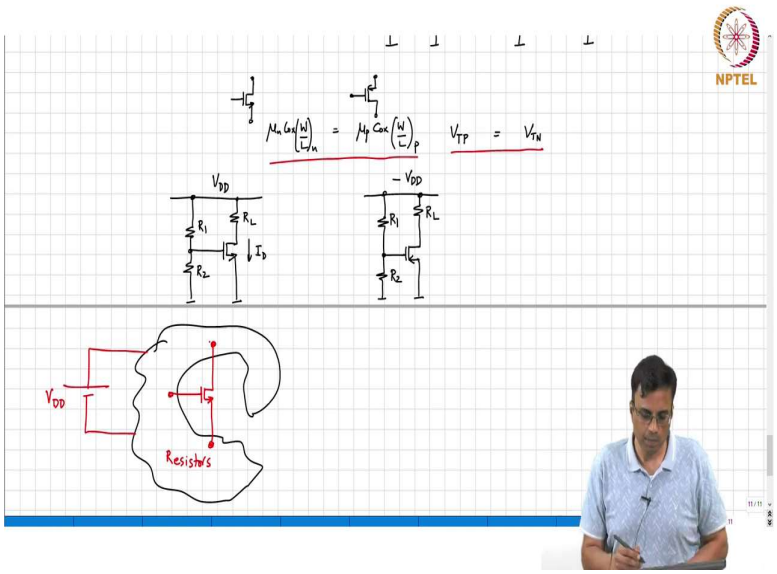
$$I_D = ½ \mu_P C_{ox} W/L(V_{SG} - V_{TP})^2.$$

So, the drain potential the quiescent drain voltage is the quiescent voltage the drain is nothing but $I_D R_L$. And if you want to make the incremental equivalent how does the incremental equivalent look? The capacitor becomes a short that is v_i then you have $R_1 // R_2$ and what is the equivalent? This is $g_m v_i$ which is happens to be V_{GS} in this case and then it is R_L and the output is v_o. Now, what is the incremental gain?

Student: $-g_m R_L$.

This is the same volt common source amplifier that we have looked at. Is it clear? Ok alright.

(Refer Slide Time: 11:32)



So, around let us take look at the let us say I had an NMOS transistor and a PMOS device and let us say for argument sake that $\mu_n C_{ox} W/L$ for the NMOS transistor is the same as $\mu_P C_{ox} W/L$.

Let us also say that V_{TP} is the same as V_{TN} ok. Now, I want to just point out something. So, let us say we have an NMOS circuit something like this ok. This is just an example say R_1 R_2 R_L this is some V_{DD} ok. So, what is the gate source voltage?

Student: V_{DD} R_2 /(R_1 + R_2).

Now, if I want to replace and there is some there is some drain current here which is you know whatever right $(V_G - V_T)2$ ½ μ_n C_{ox} W/L. Now, let us say I wanted to replace this transistor if I wanted to realize the same common source amplifier with a PMOS device. If I wanted to replace the transistor with a PMOS device, alright? What comment can I make about first job of course, is to bias the transistor? So, earlier V_{GS} has to be in the NMOS case V_{GS} has to be positive right? Gate has to be higher than the source. So, in the PMOS case V_{GS} must be?

Student: Negative.

Negative, right. So, if you did not want to change anything as far as the topology is concerned what would you do? You just replace this V_{DD} with?

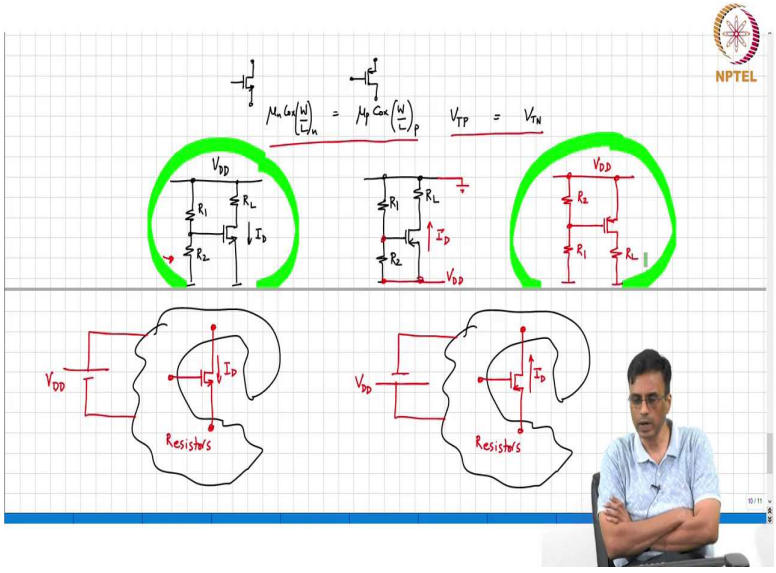
Student: - V_{DD}.

- V_{DD}, correct alright. So, consequently what will happen? All the V_{GS} the quiescent values what have you done? I mean remember that in this case, what you have is a transistor around the transistor you have some you have some network with resistors correct? Ok. This is some you know resistive network, correct? This is what we use for biasing. Correct?

And there is a battery V_{DD} and the operating point is established by this combination of this battery and this this resistive network, correct? Ok. Now, if you want to replace this NMOS transistor with a PMOS one and assuming that the PMOS transistor has the same threshold and the same.

You know μ_n C_{ox} W/L and you know μ_p C_{ox} W/L. What should we do to all the to the quiescent voltages at these nodes? We need to reverse them. So, what is the so, what is the easiest I mean what how do you think we can reverse them? All that we need to do in the PMOS case is to simply take whatever NMOS network we have we flip the direction of the V_{DD} then what can you do? You just simply remove the NMOS and put a PMOS right? Earlier the gate was higher than the source. Now, the source is higher than the gate, but the gate source voltage will remain exactly the same and likewise the direction of the current will be opposite, but the magnitude of the current will be exactly the same. Does it make sense?

(Refer Slide Time: 16:09)



And as an example, you can see here. So, the source gate voltage in this case the gate source voltage was V_{DD} R_2 /(R_1+R_2). Now the source gate voltages V_{DD} R_2/(R_1+R_2). So, earlier the current I_D was flowing downwards, now the current is flowing the same current I_D is flowing upwards alright, but of course, we do not like we do not like negative voltages first right. So, if we do not like negative voltages what do we do?

All the voltages I mean the highest potential is 0 and the lowest potential is negative V_{DD} which we do not like. So, what do we do? Add V_{DD} to all nodes. So, basically then the this node becomes ground. What does the lowest node become?

Student: V_{DD}.

That is V_{DD}. So, nothing changes, correct? Ok. Alright, now what is something else that we do not like the higher potential is below and the lower potential is above. So, we do not like that. So, we?

Student: Flip it.

Yeah, flip it and just redraw the circuit. So, that V_{DD} is on top that is R_L this is V_{DD} what must be the upper resistor in the bias network?

Student: R_2.

R_2 and this is R_1. So, this guy and this guy will have exactly the same operating point same incremental gain same everything provided the transistors are identical except for you know the NMOS being PMOS, that means, that the moment you see a circuit with NMOS transistors right you can convert it into a circuit with PMOS transistors by simply first thing to do is replace every NMOS transistor with a PMOS transistor, replace all positive batteries with negative batteries. Then you do not like negative voltages you add appropriate you know voltage so that the lowest potential becomes 0 and not negative.

Since the directions of the currents are all going you know upside down you turn the circuit upside down and therefore, then you will get a PMOS circuit where which operates between positive supply and ground and where current flows from a you know current of course, always flows from a positive potential to a lower potential, but in the page, it will flow from upwards to downwards, right?

So, so by attending this class you basically doubled the number of circuits you know right because every circuit you knew before can be converted into?

Student: PMOS.

PMOS, right? The only thing is it takes a little while getting used to because you know everything is kind of you know reversed right, but after a little bit of practice you will find that working with PMOS transistors is just as easy or difficult as working with NMOS transistors, right? And as you pointed out it turns out that in a I think you probably know this already from your device classes.

But as you know the mobility of holes at least in older technologies was smaller than the mobility of electrons and therefore, you know ah PMOS transistor that nu P turns out to be smaller maybe by a factor of 2, 3 something like that right, And therefore, inherently if you want to have the same trans conductance with the PMOS device you must increase the size of the device ok. And so, indeed it turns out that you know PMOS transistors are slower than NMOS transistors; however, we still need them and use them because of their complementary property. Does it make sense? Ok.