Analog Electronic Circuits
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Lecture - 39
The PMOS Transistor

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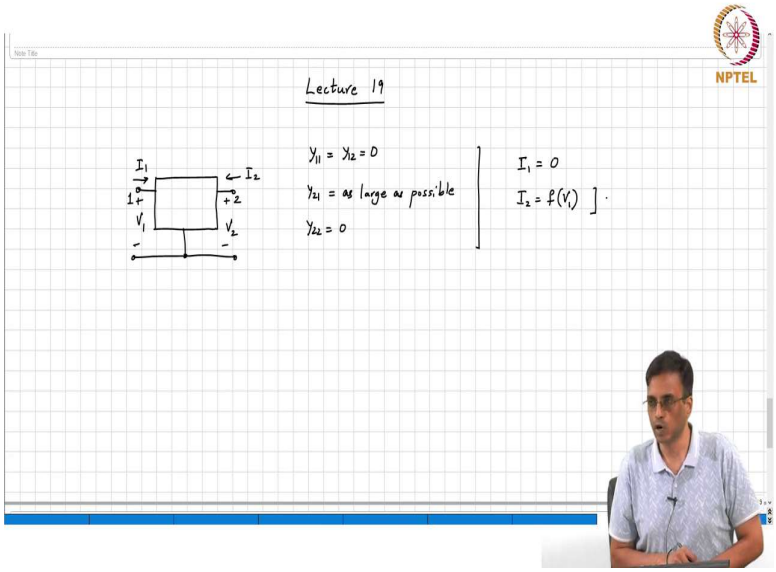

So far in this course, we have seen the NMOS depletion enhancement mode field effect transistor, and how we came up with it was the following: Let me give you a quick reminder. We said we were going to have a passive 3-terminal, 2-port. This is terminal 1, this is terminal 2, and this is the common terminal.

And, we basically said that if the device has to have gain, then it has to be non-linear, and the incremental Y_{11} and the incremental Y_{12} must be 0, and the incremental Y_{21} must be?

Student: Large.

You know as large as possible and incremental Y_{22} must be?

Student: 0.

0, Y_{12} must be 0 to avoid problems with stability. And, a possible set of characteristics that satisfy these constraints is that port 1 current is 0. Remember that port 1 current need not be 0, all that it needs to be is to be a constant, right. If that constant is 0 it is a special case and it

turns out that in practice there are devices which do this and of course, you know I_2 is only a function of V_1, right. So, this is capital V_2, this is I_2 and this is capital I_1 and this is V_1, ok and we also recognize that this is not possible for all the port 2 current cannot be only a function of port 1 voltage for all values of V_2, right. As V_2 becomes sufficiently small we basically end up with the you know the characteristics the output characteristics have to eventually become you know will not be parallel to the x-axis.

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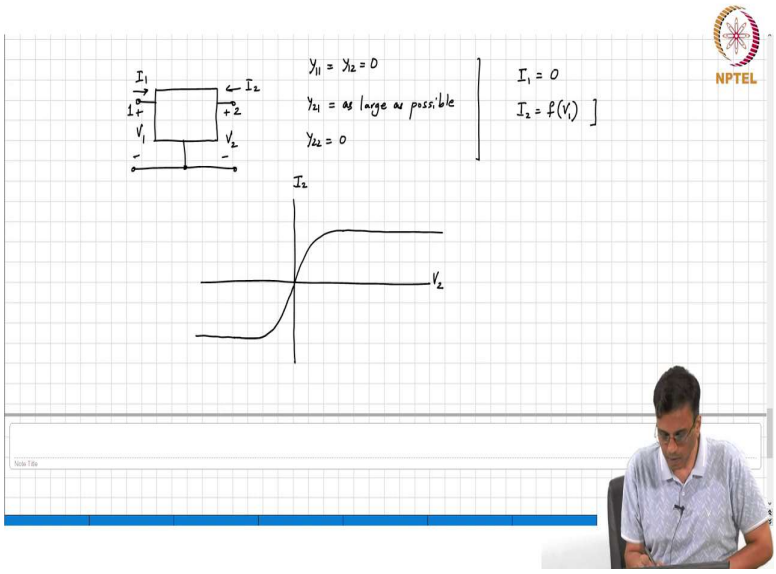

And, so, the characteristics we got assuming that the device is passive is basically we got I_2 versus V_2 if you plot the there is nothing to plot as far as the input characteristics are concerned because I_1 is identically 0. For the output characteristics we saw a family of curves like this which do right and we said that well in our discussion on which eventually led to the NMOS transistor, we said I_2 is positive, V_2 is positive because the characteristic the output characteristic given passivity and the fact that capital I_1 is 0 can only be in the first or the?

Student: Third quadrant.

So, the first quadrant behavior basically led to the NMOS transistor, right. So, it is and because you know you can have something in the third quadrant it is not surprising that you can also find electronic devices which basically have a characteristic which is in the?

Student: Third quadrant.

So, basically you have you know something like this and so, in this case therefore, V_2 is negative and?

Student: I_2 is negative.

I_2 is negative, I_1 is 0, alright and so, therefore, if V_2 is negative and I_2 is negative I_1 is 0 anyway. So, that goes away.

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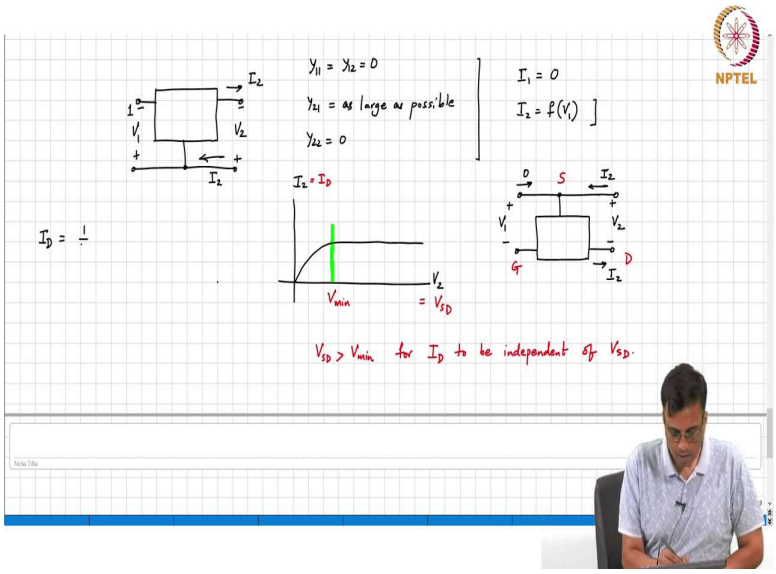

So, it turns out if I_2 is negative we basically change the direction of the arrow and V_2 is negative. So, we basically use right that is as V_2, right so, that this way the V_2 and I_2 can be, I mean if you compare it with NMOS the earlier two port I mean the it is just that V_2 and I_2 are reversed in sign the only I mean and the reason to do that is that otherwise you have to return your head you know 180 degrees.

Now, because we have denoted V_2 and I_2 as shown here. We might as well also call this V_1 ok. So, what comment can you make now? What if you plot if you denote the difference between the common terminal and the terminal on top as V_2, what comment can we make about the characteristics? They all shift to the first quadrant. So, this is just nothing but you know mere what you call notation gimmickry just to make our life easy, right and so, therefore, we are back to square 1. So, the characteristics also look like this now and you know we are often living in a gravitational field where the potential at a point higher is lower than a potential which is physically lower, right?

So, it seems a little bit awkward to say that in this picture in this diagram that we see here it seems a little bit awkward that the higher potential point is physically you know at a lower point whereas, a lower potential point is you know is higher and also seems kind of a little unnerving that current flows against gravity, right. So, gravity and current have nothing to do with each other, right? There is nothing wrong with pushing the current up and then you know having the potential current always flows from a higher potential to a?

Student: Lower potential.

So, there is nothing wrong the lower potential is below and then the higher potential is above I mean the higher potential is below and the lower potential is above and it therefore, I_2 flows from you know down to up right, but this is you know it is kind of a little bit unnerving for us having been used to fluids flowing down and everything flowing down because of the way gravity is, right.

So, rather than I mean the only way to fix this diagram there are only two ways of doing it, right. One way is to stand with your head you know on the floor and then everything will appear natural again because the lower potential will be again lower and the higher potential will be higher on the paper, right. Now, of course, that does not seem like a very practical thing to do. So, what do we do?

Well, you turn the book around right which also seems not quite practical. So, you might as well say well you turn the diagram around, right. So, basically what you do therefore, is you draw the diagram this way, alright and this again now becomes V_2, this is I_2, ok and this is I_1 which is 0 anyway and this is what we call V_1, alright.

And, you know what do you call I mean you know based on our experience with NMOS transistors which terminal will be called the source? What was the source when we talked about NMOS devices where you know what the common terminal was called the source. So, that is still the case, alright and which is the gate and which is the drain? This is the gate and this is the drain, alright. And, again the drain current is independent of the drain source voltage or the source drain voltage remember which now has a higher potential.

The source is at the highest potential the drain is at a potential lower. So, as long as the source drain potential is sufficiently positive so, ok so, if this V_2 is also the potential between the source and the drain. The source must be at a higher potential and this is of course, the drain

current and we can say that the drain current is independent of the source drain voltage as long as the V_{SD} is greater than some V minimum, ok. So, V_{SD} must be greater than V minimum for I_D to be independent of V_{SD}, alright. So, ok and in the NMOS case this statement would be V_{DS}. V_{DS} must be greater than a minimum voltage for I_D to be independent of V_{DS}. And, the equations are also very similar. So, what is the now you know the orientation now which should be straightforward to write the equation.

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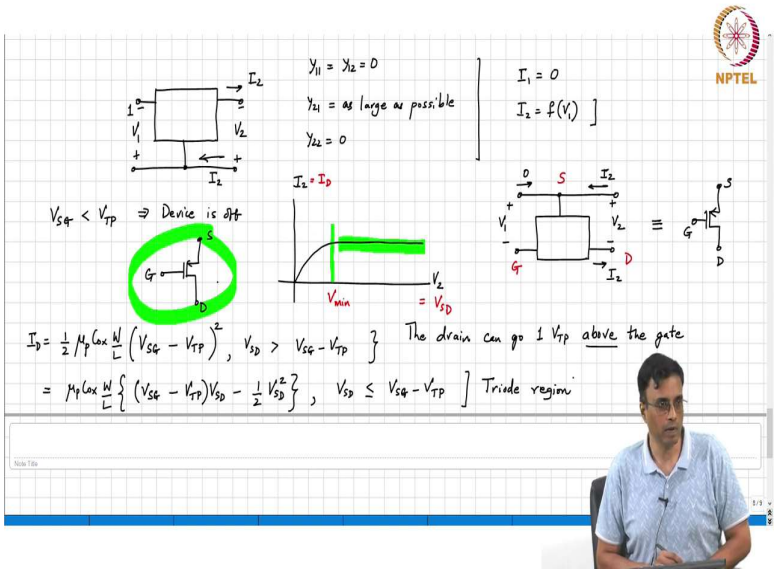

So, I_D turns out to be again first of all if V_{SG} right is less than some threshold quantity called V_T and now, earlier for the now we have two kinds of devices. Those are called the earlier devices called the NMOS transistors and their threshold is V_T. Now, since we have a PMOS transistor I mean this is what is called the PMOS transistor and therefore, to distinguish the thresholds of the two devices you know now you have a new subscript.

So, V_{TP} represents the threshold voltage of a PMOS device whereas, V_{TN} denotes the threshold of an NMOS device. So, if V_{SG} is less than V_{TP} ok the transistor is off, ok alright. And by the way how we draw the symbol is also very similar. For the NMOS transistor what did we do? What was the I mean the gate, the source and drain are very that is straightforward, right – source, gate drain ok. Now, in the NMOS case where was the arrow in which terminal was the arrow put?

Student: Source.

In the source. So, here also we should put in the source now what did the direction of the arrow indicate there?

Student: Direction of current.

So, where does the current flow?

Student: Flows into the source.

Flows into the source. So, basically if we use the same logic then this must be the symbol of the PMOS transistor, correct. So, if V_{GS} is less than V_{TP} the device is off, ok. If V_{SG} is greater than V_{TP}, alright then the current is independent of the drain source voltage or source drain voltage and is only dependent on the source gate voltage. So, V_{SG} - V_{TP} the whole square this is provided V_{SD} is greater than V_{SG} - V_{TP}. V_{TP} here is also a positive quantity. Again corresponding to what is called an enhancement mode PMOS transistor, ok. Now, in NMOS what does this mean? In the NMOS case what did it mean for a transistor to be what is the minimum voltage needed for the transistor to remain in saturation? So, basically V_{DS} had to be greater than V_{GS} minus V_{TN} in the case of an NMOS transistor. In the case of a PMOS transistor?

When do you want the drain potential to be as low as possible or as high as possible in the PMOS case?

Student: Low as possible.

We want the drain potential to be as low as possible, so that V_{SD} becomes very large to maintain the transistor in saturation, ok. So, I mean a lot of people get confused about this V_{SG}, V_{GS} and all this stuff you know which is positive which is negative and all that. The easy way to remember it is basically to recognize one basic fact and that is that current always flows from a higher potential to a lower potential. So, if you start bringing the drain potential closer and closer and closer to the source potential, there is no potential difference right or you bring the potential difference closer and closer to 0 and therefore, current cannot flow, right ok. The more the difference is I mean the easier it is to flow.

So, and if this and in the transistor basically if the source drain potential I mean if the potential between the two terminals drain and source is very large ok and is in the right direction as far as the symbol in the arrow is indicating right. For example, in the PMOS case

the arrow current must flow into the source. So, you conclude that the source potential must be much higher than the drain potential if you want to maintain the transistor in saturation. If you look at an NMOS transistor the current flows out of the source so, the drain potential must be much much larger than the source potential to maintain saturation So, do not get confused between you know if you get confused with regard to the formulas, right always use you know physical intuition, right.

Current always flows from a higher potential to a lower potential right and therefore, in a PMOS transistor the transistor will tend to get into the triode region which is the beginning of where the current flow begins to drop, right. So, the current in the drain was when the drain was at a very low potential there was some current which is constant. As you keep increasing the drain potential the potential between the source and drain starts to become lesser and lesser and therefore, it becomes more and more difficult to maintain current flow right, ok. And, therefore, as the drain potential keeps going higher and higher is when you have a problem in the PMOS case, alright. So, in English therefore, what does this sentence mean? V_{SD} must be greater than V_{SG} - V_{TP}; that means, that the edge of the triode region is defined by the drain potential. This is the easy way to remember it. The drain can go 1 V_{TP} above the gate, right. In the NMOS transistor what was this? The drain can go 1 V_{TN}?

Student: Below the gate.

Below the gate alright, ok. That is my I mean I find it personally much easier to work with that than to sit and do this formula stuff which is basically the same thing, correct. So, in a PMOS transistor the drain can go 1 threshold above the gate before the transistor gets into the triode region, in the NMOS transistor the drain can go 1 threshold below the gate and that will be the it defines the edge of the boundary between the saturation and the triode region, is that clear? Alright and of course, now what happens if the drain indeed goes higher than you know 1 threshold above the gate well the equation the form of the equation is really the same. It is μ_p C_{ox}, the transistor gets into the triode region and in the triode region what is the equation of the NMOS transistor? In the NMOS transistor what was the equation?

$$I_D=\mu_n C_{ox} W/L (V_{GS} - V_{TN}) V_{DS} - V_{DS}^2/2$$

So, now use I mean now tell me what it should be for the PMOS device?

$$I_D=\mu_p C_{ox} W/L (V_{SG} - V_{TP}) V_{SD} - V_{SD}^2/2$$

This is provided $V_{SD} \leq V_{SG} - V_{TP}$.

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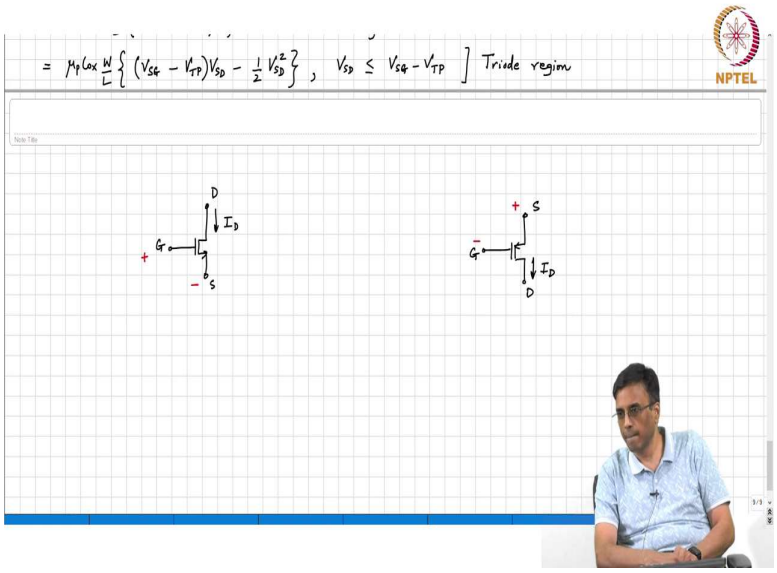

So, this is the triode region alright, ok. So, drain source gate drain, ok. So, the current flows in this direction, the current flows out of the drain right to keep the transistor alive you want the V_{GS} to be greater than a certain amount here you want the V_{SG} to be greater than a certain amount. You want the drain to be if you want to keep the transistor in saturation in the NMOS case, the drain should be very high compared to the source in the PMOS case the drain must be much much lower than the source, right. But otherwise, it is pretty much the same.

So, whatever you can do with an NMOS transistor you can also do with a PMOS transistor, alright. So, the obvious question therefore, is there is what then there is a reasonable question, right. So, I mean you know if I can do with him what I can do with him why do I need two people, right. I mean I just hire one, didn't I? right. So, the question is, you know if the equations are the same it must follow that you can pretty much do what you want if you could do something with NMOS transistors you could also do it with PMOS devices.

So, why are we wasting our time studying PMOS transistors if you know whatever you can do with NMOS you can do with PMOS? Why are we studying these devices? After all I mean you know I mean you must have studied MOS devices in a MOS circuit in your undergraduate or is it bipolar?

Student: Bipolar.

Bipolar also got the same thing. You have NPN, PNP characteristics look similar, equations look similar everything is pretty much the same only some directions of current and you know voltage change. So, why bother? Why are we studying two kinds of devices? More importantly, why are we making them? Right, evidently you know making another kind of device needs more effort, right. So, so, why do we need both of them as complementary behaviors, right? So, basically what and when you say complementary behavior it basically means that you can do something with this guy, you can do the same thing with this guy, but if you put both of them together you can do things which you cannot do with either one of them alone.

So, and you know the classic case in point is the following, right. So, if the potential goes if the drain potential of an NMOS transistor goes down right, the transistor NMOS transistor starts getting into the linear region right whereas, the PMOS transistor is very happy because its source drain voltage is increasing and therefore, it is going deeper and deeper into saturation. Another example of complementary behavior is that the NMOS transistor behaves like if you want to make a current mirror for instance current is being pulled down in an NMOS device, right. What if you want a current source which pushes current that is a PMOS transistor, right.

So, if the PMOS transistor has got a constant source gate voltage, then the transistor pushes current so it can be thought of as a current source whereas an NMOS transistor is a current sink, alright. So, by combining NMOS and PMOS transistors right, even though the individual transistors by themselves can only do a do you know do something which is limited, right.

When you combine these transistors is when you get a whole new range of possibilities that are enabled by complementary behavior, right. One of the biggest advantages you know as he pointed out is in digital logic circuits not because you cannot get logic high and logic low without complementary transistors, right. But the fact that you can make both logic states in such a way that there is no power dissipation is what is key, alright.

We will take a look at that you know going forward you know going forward we will after going through the basics of repeat everything that we saw with NMOS with PMOS just for sake of completeness. We will then see how we can combine NMOS and PMOS transistors

together to do things which are not possible with either kind of devices, right? So, that is why we are studying PMOS devices ok.