Analog Electronic Circuits
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Lecture - 37
Comparison of Current Mirrors, The High-Swing Cascode

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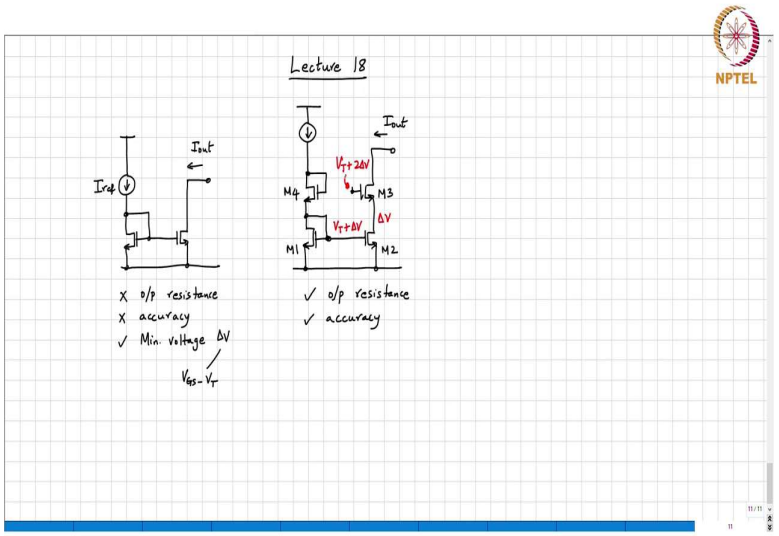

Good morning, everybody and welcome to Analog Electronic Circuits. This is lecture 18. In the last class we were looking at Current Mirrors and this is the Basic Mirror. The output current and what are the problems with this? Yeah, basically output resistance is 4 and accuracy is 4 therefore, accuracy meaning the ratio of I_{out} /I_{ref}, but what is the good point?

The minimum voltage needed is just.

Student: ΔV.

ΔV where ΔV let me remind you is again V_{GS} - V_T, right. So, to fix this problem what did we do? We said the root cause is that this is the bad current source. We want to make it a better current source. So, what do you do? How do you make a bad current source? A better current source you make that the input to a current controlled current source. And the simplest single transistor current controlled current source that you can think of is the common gate amplifier. And so that led us to the cascode current source. And we discussed how this came about yesterday. This is I_{out} and what are the good things about this?

So, the output resistance is larger by a factor of g_mR_o and therefore, also turns out that as we saw yesterday the accuracy is also very good. Why? We discussed this yesterday. Why does this have very good accuracy? Yes, Choudhry.

Student: Means for the gate voltage TΔ. So, the gate voltage will be twice of ΔV+ twice of V. So, the same current, we need a simply similar to the biasing. No hold down the gate of M3, at this I mean in this picture what is the potential of the gate of M3?

Student: 2 V_T+ΔV.

Is that necessary to keep you know M2 in the saturation region?

Student: Yes.

If you want to get high output impedance. M3 and M2 must be in what region of operation? How did we come up with the gate bias of M3? The gate bias of M3 is what? What is the bias voltage at what is the voltage of the gate of M3? What is the meaning of it should be at the edge of overdrive voltage? This sentence does not even make any sense. What is it? No, I do not understand what you are writing man I do not understand. Yes, Abhishek Choudhry. How do you get that?

Student: V_{GS} - V_T is Δs_o.

Why?

Student: same current.

Yeah. So, M3 and M2 are the same size. They are carrying the same current so the gate source voltage of M3 will be V_T+ ΔV. So, what must be the gate voltage of V_G?

Or the gate voltage of M3 must be V_T+2ΔV, right? So, what is therefore, the minimum gate voltage needed to keep M2 in saturation is? I am asking you the same question and I still see you know blank faces. What is the minimum potential needed at the gate of M3 to keep M2 in saturation?

Student: V_T+ 2 ΔV.

So, why don't I just put V? If so, therefore, if I put V_T+2 ΔV here, ok. What comment can you make about the output resistance? Assuming M3 is in saturation.

Student: remains the same.

Remains the same as?

Student: $g_mR_1R_2$.

So, if I connect the gate to V_T+2 ΔV, right? That is enough to keep both M3 and M2 in?

Student: Saturation.

Saturation and the output resistance will be? g_mR_o R_o which is $g_mR_o^2$, alright? Ok.

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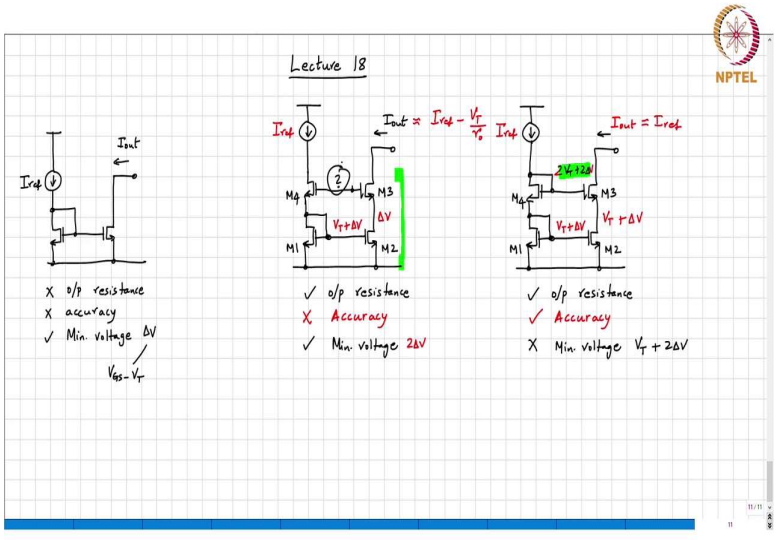

But then why did we connect it to V_T+2 ΔV? Why did we connect it? The gate of course, is I mean only the V_{GS} and the V_{DS} s are Identical, right? So, the gates of course, are identical because they are sorted together.

Student: Yes.

Its V_T+ΔV whereas the drain potential of M2 is ΔV. So, what comment can you make about the approximately? What comment can you make about I_{out}? I know it is less than I_{ref}, right? But how much less is it? Can we estimate it? So, in other words, if this voltage V_G is tied to V_T+2ΔV, what comment can you make about the current I_{out}? Yes, Pavan Kumar.

Student: Sir.

It will be smaller, but smaller by how much?

Student: V_T by half.

How did you get that?

Student: V_{GS}.

So, the difference in drain currents is basically the difference in drain voltage divided by?

Student: R_o.

R_o. So, what is so difficult about that? We did this in the last class.

Student: Yes sir.

Alright? So, what I mean the whole discussion started because this gentleman here said that the accuracy is good if the output resistance is high, but they are two fundamentally different things, right, ok? In this case if we tied this gate to V_T+2 ΔV, right? What comment can we make about the output resistance?

It is $g_m R_o R_o$ which is an order of magnitude better than the basic current mirror. Is this clear to everybody?

Student: Yes sir.

Alright. However, what comment can you make about accuracy? What is I_{out}? $(I_{ref} - V_T)/R_o$ or $g_m R_o^2$?

Student: R.

Why?

Student: R is the current is the M2, ΔV is V_T /R $_o$?

So, basically the accuracy is governed by the ratio of current between the transistors M1 and M2, right? And the V_{DS} difference is V_T and therefore, it is V_T /R $_o$, alright? Ok. So, what comment can you make about accuracy here now, is it good or bad?

Student: Bad.

Bad. So, basically, alright. So, accuracy has got nothing to do with output resistance, right? I mean you can as you can see in this mirror, I mean it is one, it is another matter where we generate V_T+2 ΔV, but what do you call it? What comment can we make about the minimum voltage though? What is the minimum voltage needed to keep to make this behave like a current source? How did you get 2 ΔV? The drain potential can go one threshold below the gate and the gate of M3 is at V_T+2 ΔV. So the minimum drain potential is 2 Δ, right. So, the minimum voltage is not, I mean it is of course, better than, but you had to expect that in order to get this high output resistance, you had to expect to pay something.

Student: Yes sir.

And what you are paying is?

Student: Loss.

Is loss of headroom and that is by only by ΔV. And that makes sense because if you want, if you have, if you stack 2 transistors one above the other, but the remember that the minimum drain source voltage needed to keep a transistor in saturation is the minimum potential needed to keep a transistor in saturation, the minimum drain source potential is what we have a transistor.

Student: Normal is what is needed.

That is all I am asking, like we have done here, what is the minimum voltage needed to keep the stack of both transistors in saturation, it is 2Δ, right? So, you cannot do better than 2 Δ. Is this clear? Ok. Now, what do you call it? So, for the not to, but if you want to fix the accuracy problem, what did we do yesterday? We recognize that the root cause was what is the root cause? What is the root cause for poor accuracy?

Student: Differentiate potential.

Ok. So, what did we do? So, what should the gate be tied to? Gate of M3, how will we fix the problem? If we want to fix the accuracy problem, what will we do? Go step by step, what should we do? What is the root cause of the problem?

The drain of M2 is basically ΔV, but it should be ΔV+V_T. So, what should the gate of M3 be tied to? What should be the potential at the gate of M3? Yes, you, in the last bench? Yeah. If

the source of the M3 is at $V_T+\Delta V$, what should the gate be at? It should be 2 $V_T+2\Delta$, correct? Now, so the minimum voltage is ΔV in this case, 2 ΔV in this case, alright. So, now what comment can you make about accuracy?

Yeah. So, basically I_{out} is simply. No, do you, all of you see why this, you know, just putting an M4 there and forcing current into its drain does not result in a magically a gate voltage? Yes, no.

Student: Yes.

Ok, alright. So, that does not work, ok.

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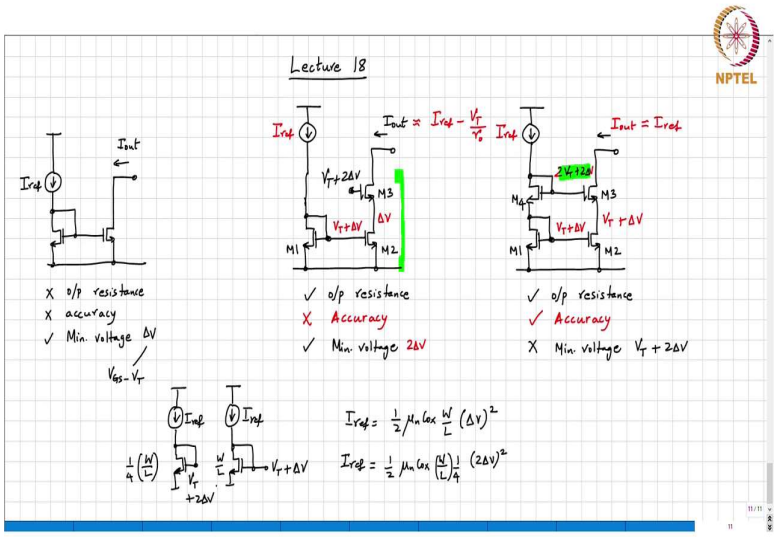

So, what voltage do we need here? We need $V_T+ 2\Delta$. The question is how do we get $V_T+2\Delta$? Alright, if I want to get $V_T+\Delta V$, what will you do?

I mean, if you want to generate a voltage which is $V_T+\Delta V$, what do you do? You will take I_{ref} and connect it into a diode connected transistor, right? So, this is giving me $V_T+\Delta V$, ok? Now, if I want $V_T+2\ \Delta V$, what do you think I should do? Ok, let me lead you to the answer. What does this say? This is if you write the equations, basically its saying I_{ref} is nothing but ½ μ_n C_{ox} W /L ΔV^2. If you are, now if we want to generate ΔV by 2, $V_T+\Delta V$ by 2, what do you think we should do?

Student: I_{ref} / 4.

Yeah, you can either do I_{ref} / 4 or you push, I_{ref} /4 is definitely something you can do. Alternatively, you can basically say you choose a transistor which is?

One fourth the size. And then the overdrive needed to basically support. If you reduce the size of the device by a factor of 4, but still pump in the same current into the diode connected device, what will the gate voltage be?

This is W /L, ok? This is W /L times one fourth. What is this gate potential?

Student: $\Delta V+V_T$.

This is $V_T+ 2\Delta$. Does it make sense?

Student: Yes sir.

Ok. So, now can you tell me how to generate $V_T+2\ \Delta V$? What will we do?

Student: (Refer Time: 19:16).

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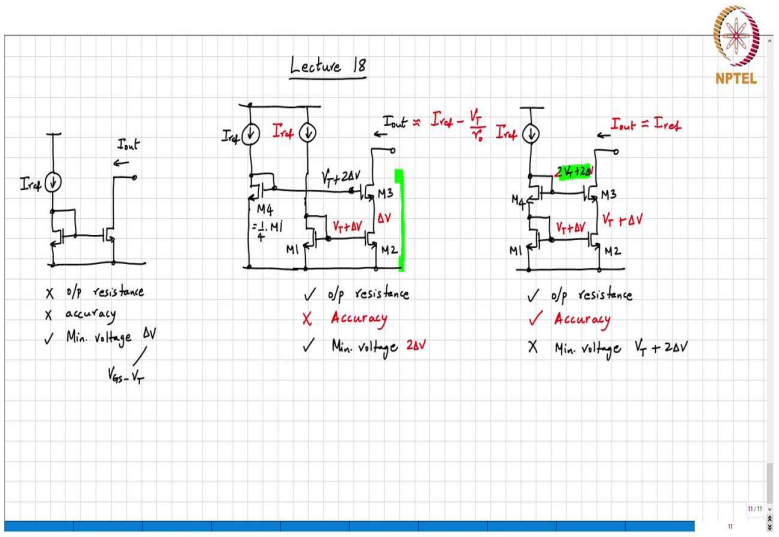

So, basically what you need to do is take. Another current source which is I_{ref} and uses a device which is? This is all this is M4 which is one fourth of?

Student: M1.

M1. In other words, if all these devices are W / L, this is one fourth W /L, ok?

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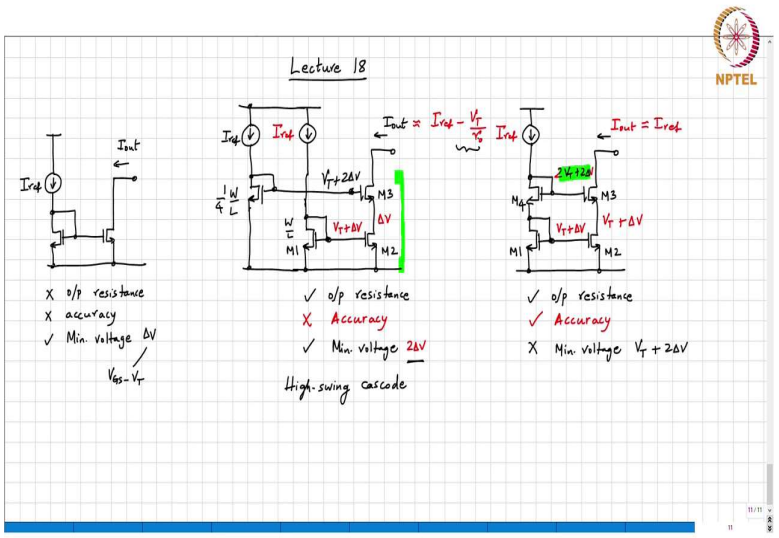

Alright, and you know as we just discussed, the output resistance of this is what is called the high swing cascade. It is called the high swing cascode and, like the regular cascode, it has very high output resistance, but the accuracy is poor because of the drain source potentials of M2 and.

Student: M1.

So, the last thing to do is what would we ideally like to do? We like to have a current mirror where the output resistance is high. The accuracy is good and minimum voltage is I mean what can it be a you know what is the smallest that we can have?

If you want $g_mR_o^2$, the minimum headroom that you need is 2 ΔV, if you want $g_mR_o^2$, you are stacking 2 devices.

Student: Yes.

And the minimum voltage needed to keep each of those devices in saturation is ΔV. So, you cannot presumably get away with the minimum voltage which is smaller than 2Δ, right. So, basically what we need to do therefore, is to make sure that the, I mean what we would ideally like to do is to basically see if we can not only get the high output resistance of $g_mR_o^2$, we also avoid this error in the output current by I mean which is fundamentally due to the different V_{DS} s of the of M1 and M.