

**Analog Electronic Circuits**  
**Prof. Shanthi Pavan**  
**Department of Electrical Engineering**  
**Indian Institute of Technology, Madras**

**Lecture - 23**  
**Robust Biasing with Drain Measurement and Source Feedback**

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Alright, so now that you have the basic idea, let's get back to stabilising the bias of a transistor. As you know, we saw that we were using negative feedback to stabilise the bias current through the transistor. We saw two techniques already right, and the basic principle is the same for all of them: we measure the current in the transistor, compare it with the desired current, and tweak the  $V_{gs}$  in the right direction.

Now, the current in the transistor can be measured in either the drain or the source, and the gate source voltage can be varied by either fixing the source or wiggling the gate.

Student: Fixing the gate.

Fixing the gate wiggled the source, so we saw the first thing that we saw was measure the current in the drain vary  $V_{gs}$  by keeping the source grounded and wiggling the gate potential that led to the current mirror right. That basically the drain in the gate was shorter. The next

thing that we did was we kept the gate voltage fixed, measured the current in the source and varied  $V_{gs}$  by wiggling the source.

Now, you know we will do the other two, alright? And what is the stuff that remains if we keep the gate fixed and measure the current in the drain?

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If  $I_D > I_{ref}$ , means  $V_{GS}$  is too small, must  $V_{GS} \uparrow$   
If  $I_D < I_{ref}$ , means  $V_{GS}$  is too large, must  $V_{GS} \downarrow$

Student: Vary the source.

and vary the source? So, let's say this is some  $V_{DD}$ . I mean, we need to fix the voltage at the gate. We just use a potential divider, but that is not the only way to do it. But I mean, you know, if you had a battery, you could just put that in the gate. So, the bottom line is that the voltage of the gate does not.

Student: Changes.

does not change,, and so what comment can you make? So, we need to compare, so in principle, what will we do now? We need to measure the current in the drain and vary the source voltage. So, in principle, what will we do? We want to measure the current in the drain. So, where will we put our ammeter?

Student: In the drain.

In the drain, this is an ammeter now, and we want to vary the source, which is the variable voltage source. So, what are we going to do? That is  $I_D$ , if  $I_D$  is greater than  $I_{ref}$ . What does it mean? It means that the  $v_{gs}$  is too large, but the gate is fixed, which means  $V_x$ , which is the source voltage. What does it mean that what you should do is the next step? Do not jump. If  $I_D$  is greater than  $I_{ref}$ , it means  $V_{gs}$  is too large, which means that  $V_x$  is?

Student:  $V_x$  is too small.

$V_x$  is too small, therefore. What must you do?

Student: Must increase.

must increase  $V_x$ . On the other hand, if  $I_D$  is less than  $I_{ref}$ , it means  $V_x$  is too large and, therefore, you must reduce  $V_x$ . Yes, clear, So now, therefore, we need to compare two currents:  $I_D$  and  $I_{ref}$ . So, what physical principle will we use?

Student: KCL.

KCL, so where do you recommend that I stick to the current source  $I_{ref}$ .

Student: Drain.

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The slide contains a circuit diagram and handwritten notes. The circuit diagram shows a MOSFET with a drain resistor  $R_D$  connected to a supply voltage  $V_{DD}$ , a gate resistor  $R_G$  connected to a gate voltage  $V_G$ , and a source resistor  $R_S$  connected to a source voltage  $V_x$ . A current source  $I_{ref}$  is connected between the drain and gate nodes. The drain current is labeled  $I_D$  and the source current is labeled  $I_S$ . A node 'y' is marked at the drain. Handwritten notes explain that if  $I_D > I_{ref}$ ,  $V_x$  is too small and must be increased, and if  $I_D < I_{ref}$ ,  $V_x$  is too large and must be decreased. A feedback loop is indicated by  $V_y \downarrow$  leading to  $V_x \uparrow$ , which leads to  $V_y \uparrow$ , which leads to  $V_x \downarrow$ .

The drain, so you want to compare  $I_D$  and  $I_{ref}$  and let that node be y. So, in other words if  $I_D$  is greater than  $I_{ref}$  what will happen to the potential of node y? If  $I_D$  is greater than  $V_y$  it will

decrease right. So, in other words rather than finding the difference between  $I_D$  and  $I_{ref}$  you can just monitor the potential of node y, if node y potential is decreasing. What does it mean?

Student: Greater.

What does it mean?  $I_D$  is greater than  $I_{ref}$  and what should you do?

Then we must increase  $V_x$ , right. So, now in a similar vein if  $I_D$  is less than  $I_{ref}$ , what will happen to  $V_y$ .

$V_y$  will increase and therefore, the bottom line is that if  $V_y$  goes down,  $V_x$  must be increased. and if  $V_y$  goes up  $V_x$  must be decreased, alright.

So basically, therefore we must compare  $V_y$ .

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The slide contains a circuit diagram and handwritten notes. The circuit diagram shows a PMOS transistor with gate voltage  $V_{ref}$  and source node  $y$ , and an NMOS transistor with gate node  $y$  and source node  $x$ . A resistor  $R_1$  is connected between node  $y$  and ground, and a voltage source  $V_x$  is connected between node  $x$  and ground. The drain current of the PMOS is  $I_D$  and the reference current is  $I_{ref}$ . The output voltage is  $V_{out}$ . Handwritten notes explain that if  $I_D > I_{ref}$ ,  $V_x$  is too small, must  $V_x \uparrow$ . If  $I_D < I_{ref}$ ,  $V_x$  is too large, must  $V_x \downarrow$ . A feedback loop is indicated by  $V_y \downarrow \rightarrow V_x \uparrow \downarrow$ .

So,  $V_x$  therefore is a voltage that is controlled by the voltage  $V_y$ , alright and therefore it is a voltage-controlled voltage source between  $y$  and  $x$ . So,  $V_y$  you must compare it against some constant, let us call that,  $V_{ref}$  we only are interested in figuring out whether  $V_y$  is going up or going down. The only circumstance under which the potential of  $V_y$  does not change is when?

Student:  $I_D = I_{ref}$ .

$I_D$  exactly equal to?

Student:  $I_{ref}$ .

$I_{ref}$ , right, so we compare the difference between some fixed voltage.

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NPTEL

$V_{DD}$   
 $R_2$   
 $I_{ref}$   
 $M1$   
 $I_D$   
 $V_{ref}$   
 $R_1$   
 $V_{DD} R_1$   
 $R_1 + R_2$   
 $V_T$   
 $V_{ref} = V_T + \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}}$   
 $V_{ref} \geq \frac{V_{DD} R_1}{R_1 + R_2} - V_T$

$V_y \downarrow$   
 $I_D > I_{ref}$ , means  $V_x$  is too small, must  $V_x \uparrow$   
 $I_D < I_{ref}$ , means  $V_x$  is too large, must  $V_x \downarrow$   
 $V_y \uparrow \rightarrow V_x \downarrow$

And go and vary the source voltage in the right direction now what is the right direction if  $V_y$  goes up  $V_x$  must go down. So, what are the signs of the OP amp?

Student: Negative.

This is negative.

Student: Positive.

And this is positive and so of course, so when the circuit is working, what comment can you make about the potential of the drain of the transistor? Why is the gain of the OP amp infinite? So, it is negative feedback. So, the difference between the minus and plus terminals must be 0 and therefore the potential at the drain is  $V_{ref}$ . Is that clear? So, to ensure that the transistor is in saturation what comment can we make about  $V_{ref}$  or rather the question I guess I am asking is will the transistor M1 remain in saturation for all values of  $V_{ref}$ . So, what are the limits on  $V_{ref}$ ?

So basically we have to ensure that since the drain potential of the transistor is  $V_{ref}$  to ensure that the transistor operates in saturation  $V_D$  must be the drain potential must be can only go as

low as 1 threshold below the gate. So, the gate potential of course, is  $V_{DD} \frac{R_1}{R_1+R_2}$  and so therefore  $V_{ref} \geq V_{DD} \frac{R_1}{R_1+R_2} - V_T$ . And what comment can you make about the potential at the source? How will you find the potential at the source?

Student:  $V_g - \sqrt{y}$ .

Yeah very good. So, basically how did you get that answer?

Student:  $V_{gs}$ .

Correct. So  $V_{gs}$  is known, why is  $V_{gs}$  known? Well the drain current is forced to be equal to  $I_{ref}$ . So,  $V_{gs}$  therefore, is nothing but,

$$V_{GS} = V_T + \sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}}$$

So, the voltage at the source is nothing but,  $V_{DD} \frac{R_1}{R_1+R_2} - V_T - \sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}}$

And so let us imagine for the time being that we had never seen this circuit before and so somebody had erased the signs on the OP amps. How will you figure out the signs on the OP amps? Now we do not know there is no need to panic or we assume some arbitrary signs.

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NPTEL

$V_{DD}$   
 $R_2$   
 $I_{ref}$   
 $M_1$   
 $I_D$   
 $V_{ref}$   
 $R_1$   
 $V_{DD} \frac{R_1}{R_1+R_2}$   
 $V_T$   
 $\sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}}$   
 $V_{GS} = V_T + \sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}}$   
 $V_{ref} \geq \frac{V_{DD} R_1}{R_1+R_2} - V_T$

$V_y \downarrow$   
 $I_D > I_{ref}$ , means  $V_x$  is too small, must  $V_x \uparrow$   
 $I_D < I_{ref}$ , means  $V_x$  is too large, must  $V_x \downarrow$   
 $V_y \uparrow$   
 $V_y \downarrow \rightarrow V_x \uparrow \downarrow$

Let us assume these signs, then what will you do?

Student: Break the loop.

Break the loop somewhere. I do not know I am going to break the loop here and I am going to yank one side up, if that goes up what comment can you make about it? So, the gate voltage is fixed if I increase the potential of the source, what comment can you make about the potential of the drain?

Student: Goes up.

Goes up. Why?

The voltage of the drain is basically you know it is a fight between  $I_{ref}$  and  $I_D$ . If the source goes up  $I_D$  must reduce. So therefore, the current being drawn from node y is smaller than the current that is being pushed into node y. So, net there is an accumulation of charge of that node which causes the node potential to jump up. If that node goes up if the drain goes up what comment we have chosen these arbitrary signs for the OP amp. So, what should be the potential at the output of the OP amp, will go up or go down?

Student: Go up.

Go up, so is this positive feedback or negative feedback.

Student: positive feedback

Positive feedback, so this basically means that the signs of the OP amps were chosen to be that we chose were incorrect.

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$I_D > I_{ref}$ , means  $V_x$  is too small, must  $V_x \uparrow$   
 $I_D < I_{ref}$ , means  $V_x$  is too large, must  $V_x \downarrow$   
 $V_y \downarrow \rightarrow V_x \uparrow$   
 $V_y \uparrow \rightarrow V_x \downarrow$

$$V_{gs} = V_T + \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}}$$

$$V_{ref} \geq \frac{V_{DD} R_1}{R_1 + R_2} - V_T$$

So, it has to be minus and plus. Is that clear folks. So, again this is yet another way of biasing the transistor which looks very different from the previous 2, but the principle is the same. So, now if you want to create a common source amplifier, what do we do?

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Well we bias it up, so the transistors are all ready for action, minus plus, now we want to make it look like a common source amplifier. So, that basically means that we have you want that. So, again it is you know what you call you have to mentally imagine the small signal



equivalent of the circuit on the left and do whatever it takes. So that incremental network looks like the one on the right. So, the easy part first is what are we missing.

Student: Source.

Source and  $R_L$ . So, I guess this now requires no more elaboration. That is  $v_i$ , That is  $R_s$ , alright. So, then we need the load resistance, so what suggestion can you make?

Well, one suggestion is the infinite capacitor  $R_L$ , this is some  $V_{ref}$ . Now source and load are done now. What else needs to be done?

Student: Ground.

How do I ground the source terminal now? The suggestion is you put an infinite capacitor here. Does this work? We know that in reality that infinite capacitor is not going to be infinite after all it's going to be some large value. But remember what kind of control source is the OP amp.

So, a voltage-controlled voltage source So, if you put a capacitor across the output of a voltage source, do you think it makes any difference? You have a voltage control voltage source, which by definition is one whose output does not change regardless of what you load it with.

So therefore, by putting the voltage control voltage source there, I mean the infinitely large capacitor, the output of the OP amp is of no consequence, right? The OP amp will still try to make sure that the drain potential is zero and the gain of the OP amp is infinity. What comment will you be able to make about the absolute potential of the drain?

Will be equal to  $V_{ref}$  irrespective of what else is happening, because the OP amp goes and does whatever it takes to keep that potential equal to  $V_{ref}$ . Therefore, if the potential of the drain is a constant what comment can you make about the incremental voltage at the output, if the voltage of the drain is not changing the output incremental voltage is 0 correct.

So, clearly, adding the infinite capacitor there at the source is not helping. So, what is the root cause of the problem?

Op amp right? So we must have some way of breaking this. I mean the reason why the drain is constant is because of the negative feedback loop created by the OP amp which is going

and wiggling the source in exactly the right way, so as to keep the drain potential constant equal to  $V_{ref}$ . We want that only for the DC picture we do not want it in the incremental network. So, we must therefore, do what to the negative feedback loop in the incremental network.

It must break the negative feedback loop in the incremental network. So, how will you break a loop?

Yeah, so one way of doing it is to simply put a large infinite inductor there or a large resistor there. So, in either case, what happens well for small signals is that this becomes an open circuit. So, the OP amp, even though it creates a negative feedback loop around the transistor for purposes of establishing the operating point, vanishes from the scenario for incremental signals, and of course, this capacitor shorts the source to ground.

So, this is yet another common source amplifier, which looks, as you can see, quite different from the other three common source amplifiers we have seen so far. The first one, of course, was the open-loop biased stabilisation one, where we just applied a gate source voltage, and the second one was the one that used drain feedback to stabilise the bias current.

The third one was one where we put a current source in the source right and then another possibility was we said we the poor man's current source is simply using a larger resistor in the source and increasing the supply voltage. So, that you get the same some similar degree of insensitivity to changes in the threshold voltage right.

And this is the; this is at least the fourth of the fifth circuit that we are seeing correct, and this stabilises again as you can see the bias current. Again, irrespective of what the temperature is and irrespective of what  $V_{DD}$  is, the drain current in the transistor is always going to be equal to  $I$  times  $I_{ref}$ . Now, the last circuit standing is: what is the last combination that is standing?

Yeah, so we basically, you know, the gate potential is not known, so we compare, measure the current in the source, and then vary the gate source voltage by keeping the source voltage constant and, you know, fiddling with the gate potential. So, let's see if we can figure this out.