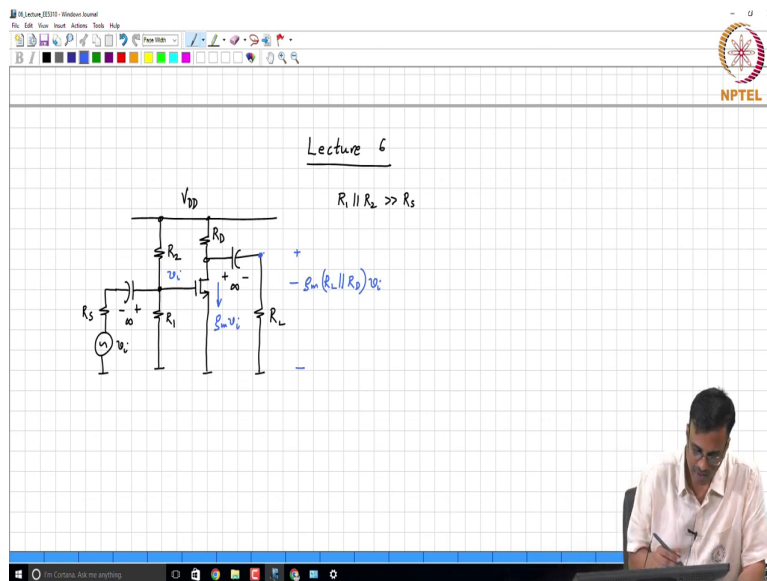


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**Lecture - 11**  
**The Common - source amplifier - part 2**

(Refer Slide Time: 00:18)



Alright. Good morning and welcome to Analog Electronic Circuits. This is lecture 6. In the last class, we looked at building an elementary amplifier using a MOSFET, more specifically an enhancement mode N channel device, right? The assumption is that the transistor is biased such that it is operating in?

Student: Saturation.

Saturation, and we also now know why these capacitors are there, right? And these capacitors are in principle they are infinite capacitors, in practice they cannot be infinite. And, the quiescent gate voltage is  $V_{DD} R_1 / (R_1 + R_2)$ , the quiescent drain voltage is  $V_{DD} - I_D R_D$ . Given the properties of the MOS transistor, we can figure out the drain current in terms of the gate source voltage.

And, the incremental gain in the circuit, if you assume that  $R_1 // R_2$  is chosen to be much larger than  $R_s$ , in that case what comment can we make about the incremental voltage at the gate?

Student:  $v_i$ .

It is simply  $v_i$ . What is the incremental current in the transistor? What is the incremental drain current in the transistor?

Student:  $g_m v_i$ .

$g_m v_i$ . And, what comment can we make about the incremental voltage across the load?

$-g_m R_L // R_D v_i$ . What comment can we make about the total voltage across  $R_L$ ?

Student: Plus, that quiescent value.

Yeah, I mean you know what the quiescent value is?

Student:  $V_{DD} - V$ .

Look, carefully please, what is the quiescent value at this node?

Student: 0.

The quiescent voltage at that node is?

Student: 0.

0. So, what is the total voltage across the load  $R_L$ ?

Student:  $-R_D$ .

It is the same as the incremental quantity, simply because the quiescent voltage is?

Student: 0.

0, is that clear?

Alright, and the consequently the price we pay in order to have a load resistance which is grounded and that does not have DC current passing through it is that the incremental gain is smaller than what we would otherwise get if we had stuck it in the drain and there was DC current flowing through it, right? And, yesterday we saw one way of improving the situation, though not a very practical one is to replace that resistance  $R_D$  with an?

Student: Infinite.

Infinite inductor and just like how an infinite capacitor you know behaves like a voltage source an infinite inductor behaves like a current source, alright. Now, the last point that we were looking at yesterday was that we recognize that this is not the only way in which one can make sure that this voltage at the gate is  $v_i$ . Is there any other way we can think of?

Is there any other way we can think of? There are several ways of.

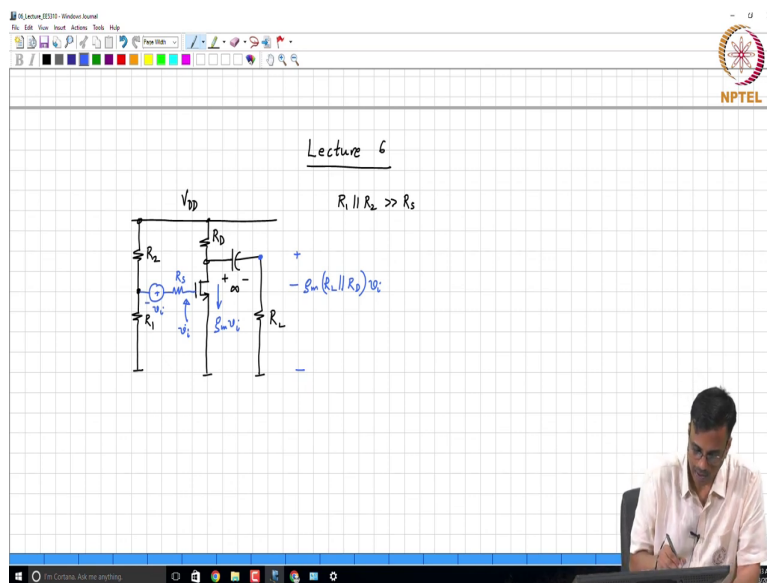
Student: Sir in between.

Pardon.

Student: In between sir. In between that k terminal and between  $R_1$  and  $R_2$ .

Very good, excellent. So, basically another idea the that one of you is suggesting is the following.

(Refer Slide Time: 05:01)



So, this is the incremental source, this is  $R_s$ . What comment can we make about the incremental voltage at the gate now?

Student:  $v_i$ .

It is?

Student:  $v_i$ .

$v_i$ . And, does that depend on  $R_1 // R_2$  being much larger than  $R_s$ ?

Student: No.

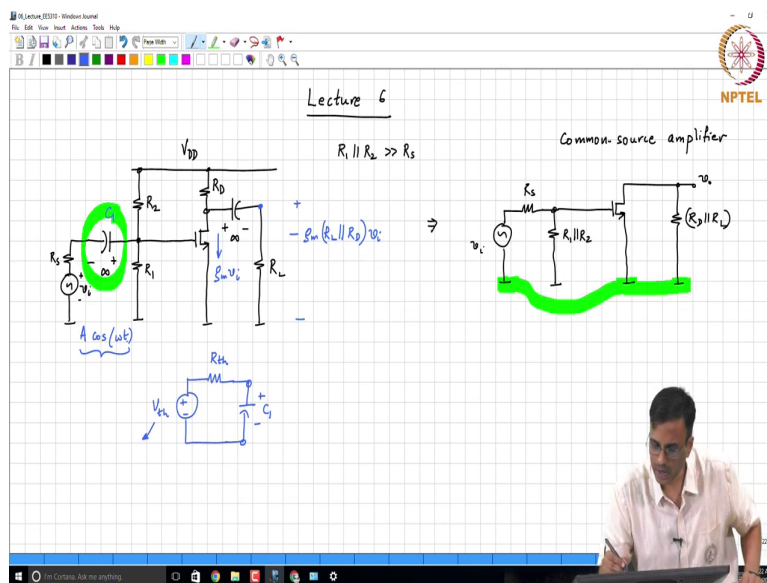
It does not depend on that, right? But what is the you know the disadvantage of the circuit? What might be a problem?

First, the practical problem with this is that this needs a floating source, right? Where both the terminals of the source are available. In practice that is you know it is not very common. Again, in many practical situations one is forced to work with only one terminal of the source being available, the other terminal of the source being inherently?

Student: Grounded.

Grounded, is that clear? Ok.

(Refer Slide Time: 06:19)



So, having seen this, let us get back to our original network, alright. So, the for incremental signals therefore, we see that this is the source  $v_i$ , this is  $R_s$ , this is what is that value of that resistance?

Student:  $R_1 // R_2$ .

Very good,  $R_1 // R_2$  and this refers to the incremental model of the MOS transistor. And, what do we have here?

Student:  $R_D // R_L$ .

$R_D // R_L$  Okay. And, if you observe carefully, you see that the ground of the source, the ground of the load and the source terminal of the?

Student: MOS transistor.

MOS transistor are all the same common terminal, right? So, this is therefore, called the source terminal of the MOS transistor is common to both the input and the?

Student: Output.

Output. So, this is why this is called the?

Student: Common source amplifier.

Common source amplifier, alright. Okay, So, the what is the only element or what are the only components in the circuit that bother us now?

Student:  $R_D // R_L$ .

What is the question?

Student: What is bothering us?

Yeah, what is I mean what when I say what is bothering us, what I mean is what is preventing us from putting the circuit into practice? So, you cannot go to a shop and then say *hi give me an infinite capacitor*. There is no nothing called an?

Student: Infinite.

Infinite capacitor, right? alright. So, now, the only the next thing we can do is say well we cannot put an infinite capacitor, we can only put a?

Student: Large capacitor.

Sufficiently large capacitor. Now, the obvious question, therefore is?

Student: How large?

How large is large? Ok. Now, to figure that out let us focus on one any one of these capacitors. Let us just take this as an example. What comment can we make about the quiescent voltage across that capacitor?

Student: Some  $V_{DD} R_1 / (R_1 + R_2)$ .

Some  $V_{DD} R_1 / (R_1 + R_2)$ , Okay. What comment can we make about the incremental voltage across that capacitor?

Student:  $v_n$ .

What is the incremental voltage across that capacitor? It is?

Student: 0

Incremental voltage?

Student: 0.

Across the capacitor?

Student: 0.

It is a?

Student: Short circuit.

Short circuit. So, basically the ideally the incremental voltage across that if the capacitor was infinite, the incremental voltage across that capacitor must be?

Student: 0.

0, because it behaves like an?

Student: Short circuit.

Like a short circuit for incremental sequence, Okay. Now, if you put in a finite value, however, large it might be. Then what comment can you make about the incremental voltage across that capacitor?

Student: finite.

0 is also finite know.

Yes, do you understand the question?

Student: Did you made some practical or finite capacitor, what will be the increment across capacitor?

Yes, ideally it should be 0. If the capacitor is not infinite, what comment can we make about the incremental voltage across that capacitor?

Student: Small values.

It will be?

Student: Small values.

Small values, small in relation to what?

Student: Change.

Yeah. So, basically if you look, at the world from the two terminals if you are sitting inside the capacitor and looking at the external world as far as the two terminals of the capacitor are concerned, the rest of the world can be replaced for small signals by its?

Student: incremental.

For small signals means incremental. If you have a linear network, right? and you take two terminals and look at the world from those two terminals, what can you replace the rest of this the world by its?

Student: Thevenin equivalent.

Thevenin equivalent. So, basically as far as the capacitor is concerned, there is some Thevenin voltage  $V_{th}$  Okay, and in series with it there is a?

Student:  $R_{th}$ .

There is a Thevenin resistance.

Student:  $R_{th}$ .

$R_{th}$  Okay, and the capacitor let me call this  $C_1$  is connected across, I mean these are the two terminals of the capacitor. And, the rest of the world as far as the capacitor is concerned look like this, correct.

So, if  $v_i = A \cos(\omega t)$ , right? all that we can say is that this  $V_{th}$  will be? What comment can we make about the  $V_{th}$ ? What is the Thevenin voltage dependent on now? Okay. At least in this example can you tell me? It depends on  $v_i$ , right? In this particular case in this particular example as far as  $C_1$  is concerned in the incremental network, what comment can we make about the Thevenin voltage across it?

Student: Equal to  $v_i$ .

It is equal to?

Student:  $v_i$ .

$v_i$ . In general however it will be some.

Student: Fraction of  $v_i$ .

Fraction of  $v_i$ , it will be some number which is proportional to  $v_i$  because it is a linear circuit. The incremental network is a linear network.

(Refer Slide Time: 13:11)

Common-source amplifier

$R_1 || R_2 \gg R_s$

$v_o = -g_m (R_D || R_L) v_i$

What is a "large"  $C_1$ ?

$R_{th} \omega C_1 \gg 1$

$C_1 \gg \frac{1}{\omega R_{th}} \ll R_{th}$

$C_2 \gg \frac{1}{\omega_{min} (R_s + R_1 || R_2)}$

$C_2 \gg \frac{1}{\omega_{min} (R_D + R_L)}$

$v_o/v_i = \frac{-g_m (R_D || R_L)}{1 + j\omega C_1 R_{th}}$

$|v_o/v_i| = \frac{g_m (R_D || R_L)}{\sqrt{1 + (\omega C_1 R_{th})^2}}$

$\omega_c = \frac{1}{R_{th} C_1}$



So, basically what we are looking at is our incremental network is looking like this. This is  $v_i$ , this is  $R_s$ , this is that  $C_1$  Okay,. And, we are looking at the rest of the network from the viewpoint. So, sitting inside that capacitor  $C_1$  and looking at the rest of the network across those two terminals. We established already the that that will be equivalent to its Thevenin equivalent.  $V_{th}$  in this particular example is what?

Student:  $v_i$ .

$v_i$ , what is the Thevenin resistance in this particular example?

Student:  $R_s + R_1 // R_2$ .

$R_s + R_1 // R_2$ . But in general it will be some  $R_{th}$ , correct, Okay. So, now, in this particular example, it is some  $V_{th}$  in this case happens to be  $A \cos(\omega t)$ . So, what comment can we make about the voltage across the incremental voltage across that capacitor  $C_1$ ? And, what is the capacitor reactance?

Student:  $1/j\omega C$ .

$1/j\omega C$ . So, the voltage across the capacitor will also be a sinusoids, right? with an amplitude which is given by? What is the amplitude of the voltage across the capacitor?

$$\frac{A}{\sqrt{1+(R_{th} \omega C_1)^2}} \cos(\omega t + \theta)$$

Right? But, the key point is to note that this amplitude is dependent on two things. One is the frequency of operation and two is the?

Student: Magnitude  $R_2$ .

Value of the capacitor, right? And the frequency of operation, correct? Why does that expression make sense? One is to say well you know it comes out of the math, but what do we know already?

Student:  $C_1$  goes to infinity.

If  $C_1$  goes to infinity, so what?

Student: 0.

What should be 0?

Student: swing.

Yeah. So, if  $C_1$  goes to infinity, we know that the swing across that capacitor must go to?

Student: 0

0, alright, and that is indeed borne out by the math, Okay, alright. So, ideally therefore, the incremental voltage swing across the capacitor must be 0, alright, Okay. In practice, we cannot make  $C_1$  infinite, we can only say  $C_1$  has to be a large capacitance. Now, the question is what is the meaning of large capacitance? Now, you know all the formula, you know what you are looking for. So, what can we say what is a large capacitance?

Student: omega fall.

Very good, right? So, basically remember that the voltage drop across that capacitor  $C_1$  must be a small fraction of the?

Student: Thevenin voltage.

Thevenin voltage.

Student: Yeah.

Alright, now how small constitute? Small is up to you. Someone may say 0.01 is small, another person may say 0.001 is small, right? As long as you are consistent with yourself, you are fine Okay. So, what this basically means that this  $R_{th}\omega C_1 \gg 1$ , Okay. So, basically  $C_1$  must be much much larger than  $1/\omega R_{th}$  or equivalently  $1/\omega C_1$ , yes must be?

Student: Much much smaller than.

Much much smaller than?

Student:  $R_{th}$ .

$R_{th}$ . So, in other words the capacitance must look like a? What is  $1/\omega C_1$ ?

It is the magnitude of the impedance of the capacitor, right? All that this analysis is saying is that well the capacitor must look like a short circuit, right, when compared to?

Student:  $R_{th}$ .

The Thevenin resistance of the circuit looking in from the terminals of the?

Student: Capacitor.

Capacitor, alright, Okay. So, clearly this definition of what a large capacitor constitutes is dependent on.

Student:  $R_{th}$ .

I mean it dependent on  $R_{th}$  that is Okay, but more importantly?

Student: Frequency.

It depends on the frequency of operation, right? So, if you are working with very low frequency circuits; for example, if you are working with audio, you know that the lowest frequency of a human hearing is?

Student: 20 hertz.

About 20 hertz. So, you want to make sure that this when you say your capacitance has to be you know very large, that  $\omega$  that you need to use is  $2\pi$  20 Hz, alright. On the other hand, if you are working with some other amplifier where the lowest frequency of operation was 1 MHz, then clearly the definition of what constitutes a large capacitor will be?

Student: Different.

Very very different in that case, alright. So, the key point to notice is that to understand is that it not only depends on the  $R_{th}$ , okay, it also depends on the lowest frequency of operation that the amplifier is expected to handle alright. So, I mean so,  $C_1$  must be much much greater than  $1/\omega_{min}R_{th}$ . Does that make sense? Now, what comment can we make about  $C_2$  therefore? After all this discussion what comment, what constitutes a large capacitance for  $C_2$ ?

Student:  $1/R_D$ .

Look, carefully, what is the Thevenin resistance looking across  $C_2$ ?

Student:  $R_D + R_L$ .

So,  $C_2$  must therefore, be much much larger than?

$$C_2 \gg \frac{1}{\omega_{\min} (R_D + R_L)}$$

In this case  $R_{th}$  is nothing but? What is  $R_{th}$  here?

$$C_1 \gg \frac{1}{\omega_{\min} (R_s + R_1 // R_2)}$$

So, in general will the limit for  $C_1$  and  $C_2$  be the same or will it be different?

Student: It will be different.

It will be?

Student: Different.

Different. So, basically the notion of what constitutes a large capacitor, even though it is the same circuit correct, different capacitors can have different meanings of what large capacitor constitutes and that is because the  $R_{th}$  looking across a capacitor keeps changing depending on which capacitor you look at. Does it make sense people? Alright, okay. So, with that we have seen all the small signal aspects of the common source amplifier, alright.

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Handwritten notes on a grid background:

Circuit diagram showing a voltage source  $V_{th}$  in series with a capacitor  $C_1$ , connected to a node that branches into a gate terminal (represented by a capacitor  $G$ ) and a load network (represented by a capacitor  $C_2$  in parallel with a resistor  $R_D$  and a load resistor  $R_L$ ). The transfer function is given as  $A(s) = \frac{V_{th}}{1 + j\omega(R_D + R_L)C_2}$ .

Equations derived:

$$G \gg \frac{1}{\omega_{\min} (R_s + R_1 // R_2)}$$

$$C_2 \gg \frac{1}{\omega_{\min} (R_D + R_L)}$$

Additional notes:

$$R_{th} \omega G \gg 1$$

$$G \gg \frac{1}{\omega R_{th}} \equiv \frac{1}{\omega C_1} \ll R_{th}$$

Question: i) What is large signal?

Now, let us take a look at the large signal aspects. So, the first question is?

Student: Large signal.

What is large signal?