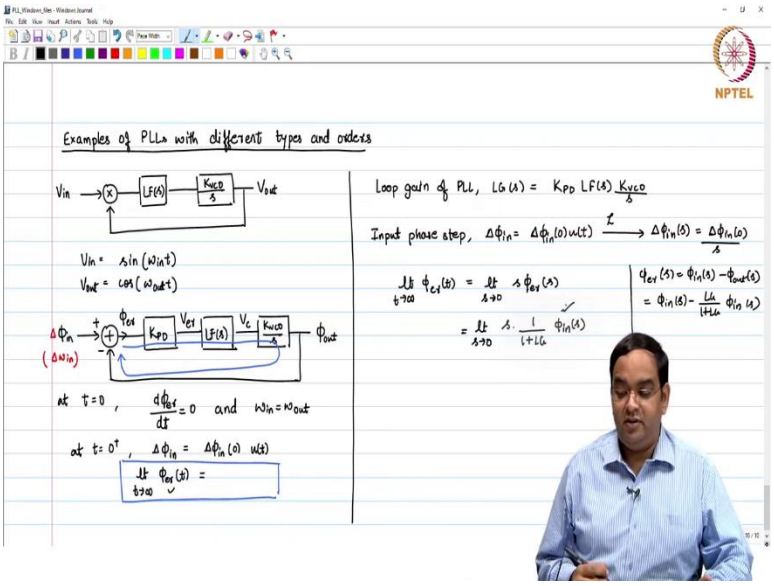
Phase-Locked Loops
Dr. Saurabh Saxena
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture – 9
Small Signal Analysis of Type-I/II/III PLLs for Phase Step, Frequency Step and Frequency Ramp

Hello everyone. In the previous session, we talked about the type and order of PLLs and we told that the loop filter is a block which decides between different PLL types and orders.

(Refer Slide Time: 0:34)



So, today we will look at examples of PLL with different types and orders and the reason to choose different type and order will become clearer as we go through our analysis. So, let me just recall the PLL which we have been using. We had a mixer based phase error detector followed by the loop filter which has a transfer function $LF(s)$ followed by the VCO which has a transfer function $\frac{K_{VCO}}{s}$ and this feeds back. The input and output are sinusoidal voltages. In our case, we will treat them right now as follows:

$$V_{in} = \sin(\omega_{in} t)$$
$$V_{out} = \cos(\omega_{out} t)$$

We drew the small signal model of this particular PLL and the small signal model of the PLL is shown here. You have the phase error detector with input phase and feedback phase. The gain of the phase error detector is K_{PD} followed by loop filter with transfer function $LF(s)$ which is followed by VCO with gain $\frac{K_{VCO}}{s}$. This is the small signal model of the PLL. This is φ_{out}, here you are going to get φ_{er}, output of the phase error detector is voltage, we call this as V_e, output of the loop filter is control voltage which is V_c.

Now, where will this type and order of the PLL matter? It will matter when we apply any change in phase or any change in frequency of the PLL and we want to find out whether this PLL will remain in lock or it will go out of lock or what will happen. So, one standard method of a closed loop feedback system is, let us say you have this closed loop PLL, it is closed loop in nature that is why I am calling it as a closed loop and it is in steady state, that means, at time $t = 0$, the rate of change of phase error is equal to zero, that is how the PLL is in steady state and input and output frequencies are equal. Thus, we have the following:

$$\text{At } t = 0, \frac{d\varphi_{er}}{dt} = 0 \text{ and } \omega_{in} = \omega_{out}$$

So, you have a PLL which is in steady state.

Now, you apply change in input phase or input frequency and if the PLL still remains in lock which means that, at $t = 0^+$, I apply a change in the input phase which is $\Delta\varphi_{in} = \Delta\varphi_{in}(0)u(t)$. This is just one kind of change which is applied to the PLL and then we give it enough time such that all the transients die out and we look at the PLL in steady state which means that after enough time we would like to find out what is the phase error in steady state. Why do we look at the phase error in steady state? Because in steady state or as time $t \to \infty$, the phase error should not change if the PLL is locked.

So, this is the thing which we are looking at, as $t \to \infty$, if the phase error is some fixed value, then the PLL will be considered that it is in lock, if this value tends to infinity, then it is like the phase error increases with respect to time, it is not locked. We would like to find out this particular phase error for different kinds of inputs which will depend on the type of loop filter which we choose.

So, let us begin with an example. We will consider many examples. First, the loop gain of the PLL is given by $LG(s)$. You see that this is the loop and we are considering when you apply a change what comes back, that is the loop gain. This loop gain is given by,

$$LG(s) = K_{PD}\, LF(s) \frac{K_{VCO}}{s}$$

Now, we apply a change at the input which is known as phase step which we will call as input phase step here.

So, we have,

$$\Delta\varphi_{in} = \Delta\varphi_{in}(0)u(t)$$

In frequency domain or in Laplace domain, you have,

$$\Delta\varphi_{in} = \Delta\varphi_{in}(0)u(t) \xrightarrow{L} \Delta\varphi_{in}(s) = \frac{\Delta\varphi_{in}(0)}{s}$$

This is for the step input. So, for this particular case, the error at infinity is given by,

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s\, \varphi_{er}(s)$$

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s\, \frac{1}{1+LG} \varphi_{in}(s)$$

Also, you know from this particular loop that phase error in frequency domain is given by,

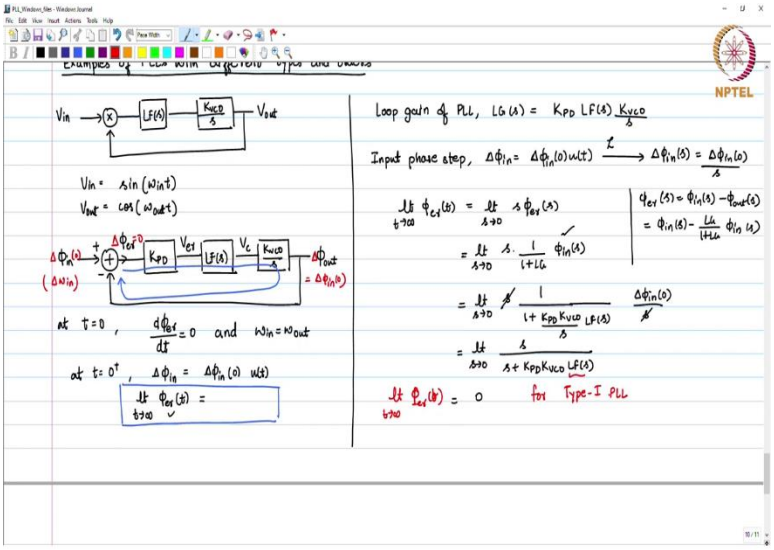
$$\varphi_{er}(s) = \varphi_{in}(s) - \varphi_{out}(s)$$

So, you might be seeing here that I am using $\varphi_{in}(s)$and $\Delta\varphi_{in}(s)$ interchangeably, so that is like the small change which I am applying. So, we have,

$$\varphi_{er}(s) = \varphi_{in}(s) - \frac{LG}{1+LG} \varphi_{in}(s)$$

So, this expression is clear from here.

(Refer Slide Time: 8:22)



Now, we have the following:

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s \frac{1}{1+\frac{K_{PD}\,K_{VCO}}{s} LF(s)} \frac{\Delta\varphi_{in}(0)}{s}$$

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} \frac{s}{s+\ K_{PD}\,K_{VCO}\,LF(s)} \Delta\varphi_{in}(0)$$

After substituting $s = 0$ here, we get,

$$\lim_{t\to\infty} \varphi_{er}(t) = 0$$

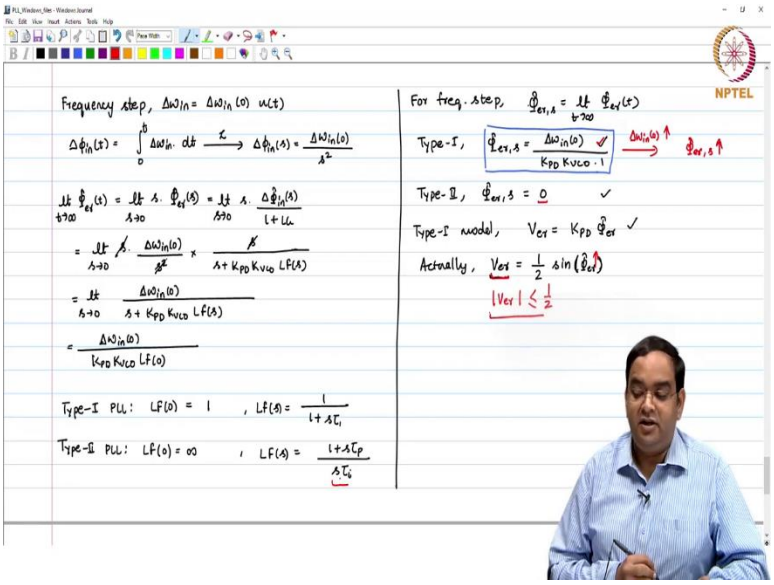
So, you applied a phase step input and you found that the error in steady state is going to be zero. What does it mean? It means that if I apply $\Delta\varphi_{in}(0)$ here, after some time I will see a change in $\Delta\varphi_{out}$ which is same as $\Delta\varphi_{in}(0)$, so that $\Delta\varphi_{er}$ becomes zero. That is what you have.

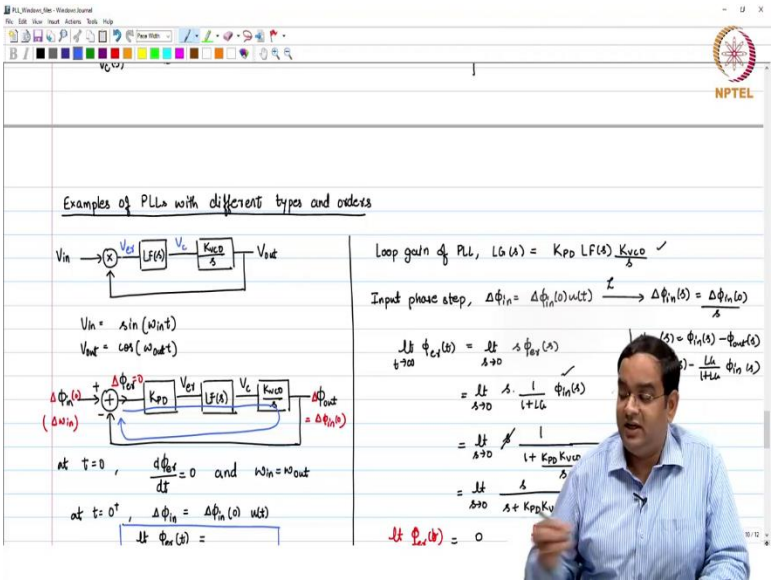
Also, every PLL we know is Type-I PLL. So, here $LF(s)$ you can see, it will only be a problem when $LF(s)$ is $LF(0)$ is equal to zero. Then you have a zero by zero which is not defined, which is not the case also. So, for Type-I PLL, I can write,

$$\lim_{t\to\infty} \varphi_{er}(t) = 0, \text{ for phase input for Type-I PLL}$$

It does not matter what order we have here.

(Refer Slide Time: 10:32)





Now, after this phase step, let us see if I apply another change which is frequency step. When we apply a frequency step to the PLL, so here I am going to apply a frequency step at time instant $t = 0$ which is given by,

$$\Delta\omega_{in} = \Delta\omega_{in}(0)\, u(t)$$

We know that,

$$\Delta\varphi_{in}(t) = \int_0^t \Delta\omega_{in}\, dt$$

Now, in Laplace domain, this frequency step relates to phase ramp as given by,

$$\Delta\varphi_{in}(t) = \int_0^t \Delta\omega_{in}\, dt \xrightarrow{L} \Delta\varphi_{in}(s) = \frac{\Delta\omega_{in}(0)}{s^2}$$

We would like to find out the phase error as $t \to \infty$ for the frequency step. This is given by,

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s\, \varphi_{er}(s) = \lim_{s\to 0} s\, \frac{\Delta\varphi_{in}(s)}{1 + LG}$$

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s\, \frac{\Delta\omega_{in}(0)}{s^2} \times \frac{s}{s + K_{PD}K_{VCO}LF(s)}$$

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} \frac{\Delta\omega_{in}(0)}{s + K_{PD}K_{VCO}LF(s)}$$

$$\lim_{t\to\infty} \varphi_{er}(t) = \frac{\Delta\omega_{in}(0)}{K_{PD}K_{VCO}LF(0)}$$

This is the steady state error in the PLL. So far I have not discussed what is $LF(0)$ but you can see very well here that,

For Type-I PLL: $LF(0) = 1$, where $LF(s) = \frac{1}{1+s\tau_1}$

For the Type-II PLL with two integrators, the loop filter transfer function is given by,

For Type-II PLL: $LF(0) = \infty$, where $LF(s) = \frac{1+s\tau_p}{s\tau_i}$

What is $LF(0)$? $LF(0)$ is actually equal to infinity. If this is the case, then for frequency step, the steady state phase error is given by,

$$\varphi_{er,s} = \lim_{t\to\infty} \varphi_{er}(t)$$

For Type-I PLL, the steady state error is given by,

$$\varphi_{er,s} = \frac{\Delta\omega_{in}(0)}{K_{PD}\, K_{VCO}.1}$$

For Type-II PLL, the steady state error is given by,

$$\varphi_{er,s} = 0$$

For Type-II PLL, what you see is that the steady state phase error is zero because $LF(0)$ goes to infinity. So, this is interesting that for the same PLL, you have input and output frequencies locked and when you apply a simple phase step, you see that in both Type-I and Type-II PLL, the error will be equal to zero, but when you apply frequency step, for Type-I PLL there is a steady state error, but for Type-II PLL, the steady state error is equal to zero. But keep one thing in mind that this particular value, the steady state phase error which you see here does not take into account the large signal or you can say the actual voltage signal at each of these nodes. It is only for small signal modeling.

So, why is this important? Well, we have seen earlier that in the model for Type-I PLL which we are using, the error voltage is given by,

$$\text{Type-I model: } V_{er} = K_{PD}\varphi_{er}$$

But, actually if you remember, the error voltage is given by,

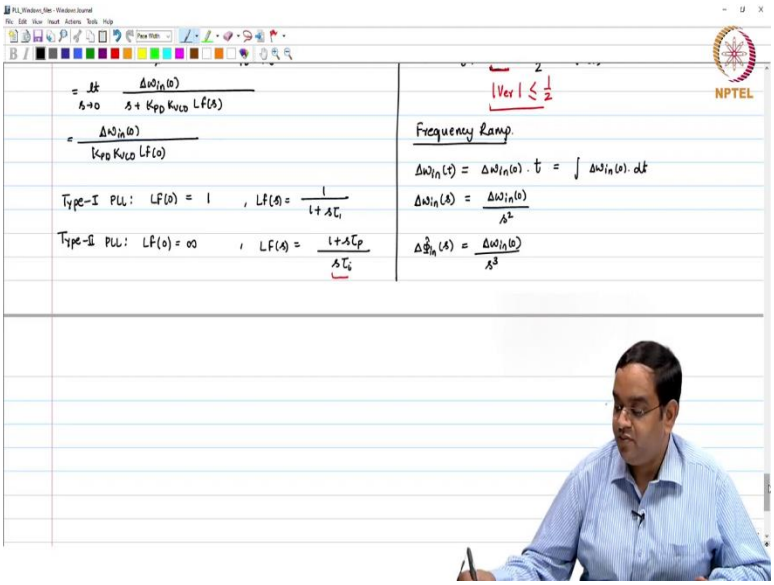
$$\text{Actually: } V_{er} = \frac{1}{2}\sin(\varphi_{er})$$

We have seen this before. I am just repeating it because we are discussing with respect to types and orders.

So, in this model, there is no restriction at all on φ_{er} but if you look at it, no matter what φ_{er} you are going to have, there is a restriction on V_{er}. Here if you see, if $\Delta\omega_{in}(0)$ is large, φ_{er} will also be large. If I increase $\Delta\omega_{in}(0)$, φ_{er} will increase and it appears that the PLL will always remain in lock, whereas actually what you see is even if φ_{er} increases, V_{er} is bounded.

So, if V_{er} does not increase, the control voltage will not increase and you will not be able to get the desired frequency change but for small changes which are limited by your modeling here, $\varphi_{er,s}$ will be valid. In case of Type-II PLL, it does not matter because in steady state you are going to have the phase error of zero. You will acquire all the frequency with the help of the other integrator in the loop.

(Refer Slide Time: 18:22)



Well, this is interesting that for Type-I and Type-II PLL, we are able to get that. Now comes another question. We applied frequency step, now what happens if I apply frequency ramp. So, what do you mean by frequency ramp? It means that $\Delta\omega_{in}(t)$ is increasing at a fixed rate as given below.

$$\Delta\omega_{in}(t) = \Delta\omega_{in}(0).\, t = \int \Delta\omega_{in}(0)\, dt$$

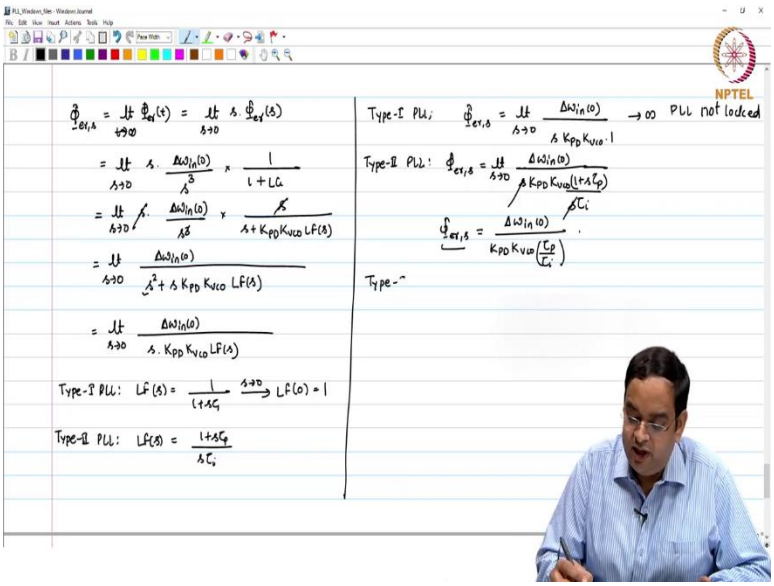
So, for frequency ramp, the transfer function in Laplace domain for the change in the frequency is going to be,

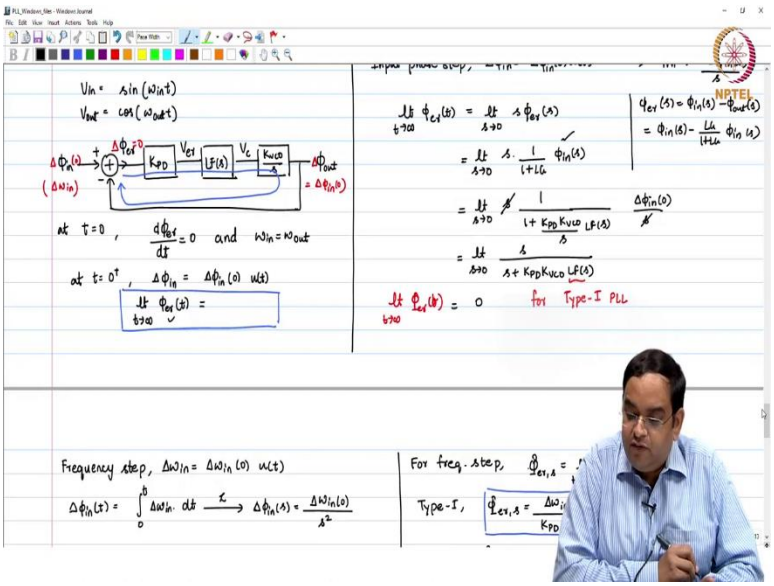
$$\Delta\omega_{in}(s) = \frac{\Delta\omega_{in}(0)}{s^2}$$

For the corresponding change in the frequency, the change in the phase is going to be,

$$\Delta\varphi_{in}(s) = \frac{\Delta\omega_{in}(0)}{s^3}$$

(Refer Slide Time: 19:39)





Now, for the desired frequency change of frequency ramp, the change in phase is given by this. I need to find out whether the PLL will remain in lock which means I need to find out what is the steady state error value. Well, the same principle, nothing changes here, so the steady state phase error is given by,

$$\varphi_{er,s} = \lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s\, \varphi_{er}(s)$$

$$\varphi_{er,s} = \lim_{s\to 0} s\, \frac{\Delta\omega_{in}(0)}{s^3} \times \frac{1}{1+LG}$$

$$\varphi_{er,s} = \lim_{s\to 0} s \frac{\Delta\omega_{in}(0)}{s^3} \times \frac{s}{s + K_{PD}K_{VCO}LF(s)}$$

$$\varphi_{er,s} = \lim_{s\to 0} \frac{\Delta\omega_{in}(0)}{s^2 + s\, K_{PD}K_{VCO}LF(s)}$$

So, I have to substitute $s = 0$, so I will just rewrite it with the remaining terms as follows:

$$\varphi_{er,s} = \lim_{s\to 0} \frac{\Delta\omega_{in}(0)}{s\, K_{PD}K_{VCO}LF(s)}$$

For $LF(s)$, I will not substitute because the evaluation depends on the loop filter. So, for the frequency ramp, what you see is that it depends on what is the value of the loop filter at $s = 0$.

For Type-I PLL: $LF(s) = \frac{1}{1+s\tau_1}$

For Type-II PLL: $LF(s) = \frac{1+s\tau_p}{s\tau_i}$

So, you can substitute $s = 0$ for both the cases. What you are going to see is the following:

For Type-I PLL, as $s \to 0$, $LF(0) = 1$

For Type-I PLL, the steady state phase error is given by,

$$\varphi_{er,s} = \lim_{s\to 0} \frac{\Delta\omega_{in}(0)}{s\, K_{PD}\, K_{VCO}.1} \to \infty$$

So, if you have a Type-I PLL, Type-I, Order-1, that is what we have been using, then when you apply a frequency ramp to the PLL, the steady state phase error goes to infinity which means that the phase error does not settle. The PLL loses lock, it is not locked anymore. For Type-II PLL, the phase error in steady state is given by,

$$\varphi_{er,s} = \lim_{s\to 0} \frac{\Delta\omega_{in}(0)}{s\, K_{PD}\, K_{VCO} \frac{1+s\tau_p}{s\tau_i}}$$

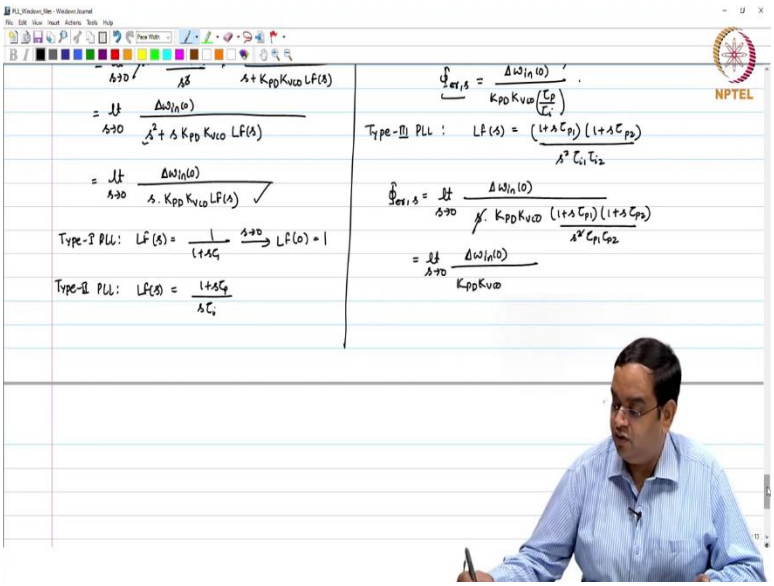
As $s \to 0$, we get,

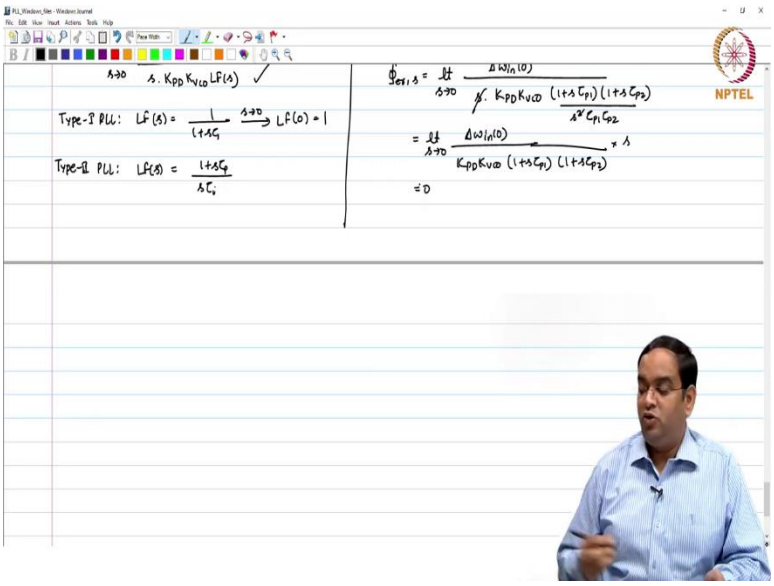
$$\varphi_{er,s} = \frac{\Delta\omega_{in}(0)}{\frac{K_{PD}\, K_{VCO}}{\tau_i}}$$

This is interesting that when you have a frequency ramp or the change in the input frequency is given as a frequency ramp, Type-I PLL will lose lock but Type-II PLL will have a fixed phase error at the output of the phase error detector given by the above equation. So, this will be the fixed value which you have.

So, we can just look at it here. For Type-I PLL, for phase step, you had zero phase error and Type-II PLL also has zero phase error. For frequency step, Type-I PLL has a fixed phase error and Type-II PLL has zero phase error. For frequency ramp, Type-I PLL loses lock as the phase error tends to infinity, whereas Type-II PLL has a fixed steady state phase error. So, looking at this trend, you may be tempted to think that if I want to make this steady state error equal to zero, then Type-III PLL may be a solution, you can increase one order of integrator.

(Refer Slide Time: 26:01)





So, let us just take that example. Let us say for Type-III PLL, we have the loop filter transfer function as given by,

$$LF(s) = \frac{(1 + s\tau_{p1})(1 + s\tau_{p2})}{s^2\tau_{i1}\tau_{i2}}$$

Right now, all these parameters τ are just constant, so do not worry about it. What values they will pick, we will see that during the implementation, if required. So, for this particular loop filter, for frequency ramp, let us calculate the steady state phase error.

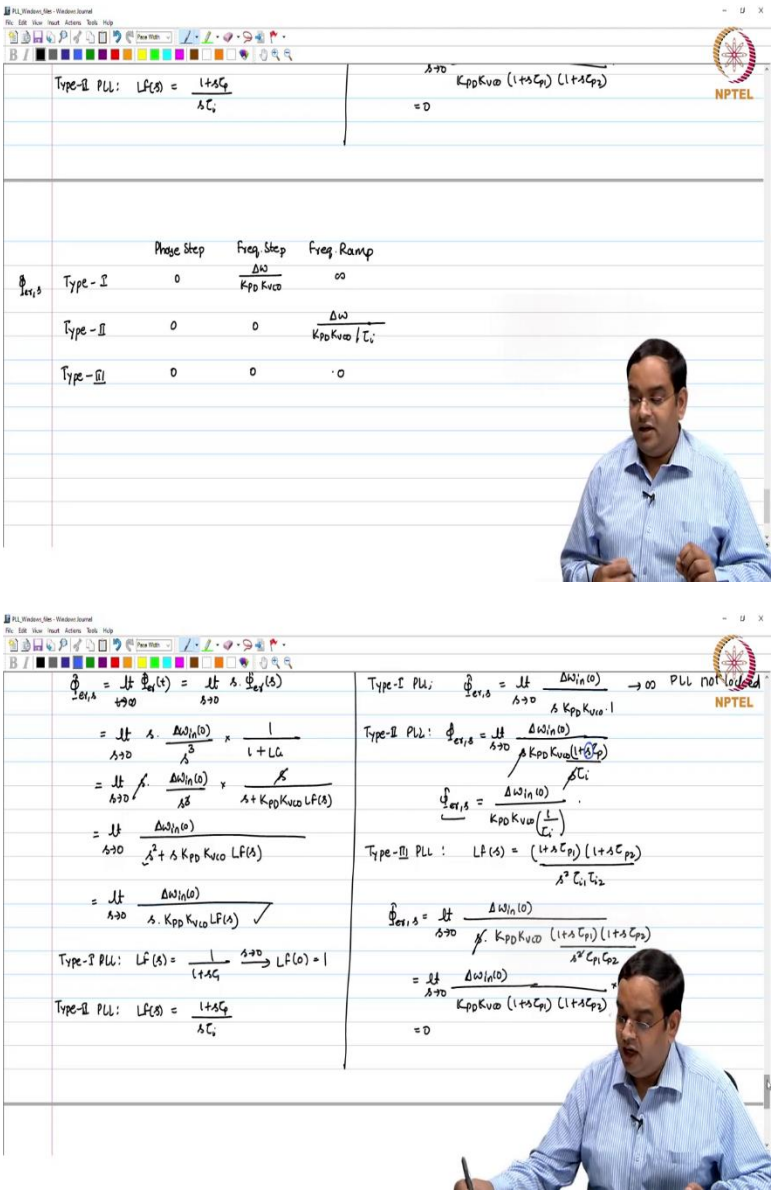
$$\varphi_{er,s} = \lim_{s\to 0} \frac{\Delta\omega_{in}(0)}{s\, K_{PD}\, K_{VCO} \dfrac{(1 + s\tau_{p1})(1 + s\tau_{p2})}{s^2\tau_{i1}\tau_{i2}}}$$

$$\varphi_{er,s} = \lim_{s\to 0} \frac{\Delta\omega_{in}(0)}{K_{PD}\, K_{VCO}(1 + s\tau_{p1})(1 + s\tau_{p2})} \times s$$

$$\varphi_{er,s} = 0$$

So, for Type-III PLL also, what you see is that even in the case of frequency ramp, the error is equal to zero.

(Refer Slide Time: 27:48)



So, I will just summarize it. So what you have is, we are going to write the steady state phase error for Type-I, Type-II and Type-III PLLs when you apply phase step, frequency step and frequency ramp. So, when you have phase step, Type-I, Type-II, Type-III PLL, all will give zero. When you have frequency step, Type-I will give you $\frac{\Delta\omega}{K_{PD}\,K_{VCO}}$. Type-II PLL will give you zero, Type-III will also give you zero.

When you have frequency ramp, Type-I PLL will give you steady state phase error as infinity, that means the PLL is not locked. Type-II PLL is going to give you $\frac{\Delta\omega}{\frac{K_{PD}\,K_{VCO}}{\tau_i}}$.

And for frequency ramp, Type-III PLL will still give you zero. So, based on what you would like to do with the PLL, whether you would like to apply phase step, frequency step or frequency ramp, you can choose the type of the PLL. And type and order of the PLL will depend on what kind of tracking do you want, so based on that you make a choice. Then, you may ask that why I did not have only s^2, why I needed to have $s\tau_{p1}$ and $s\tau_{p2}$. Similarly, for the case of Type-II PLL, why I had $s\tau_p$? Well, all these things are required to stabilize the loop. We will see the stabilization in the upcoming sessions. Thank you.