Phase-Locked Loops
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Lecture – 7
Time Domain versus Small Signal Analysis of a Simple PLL

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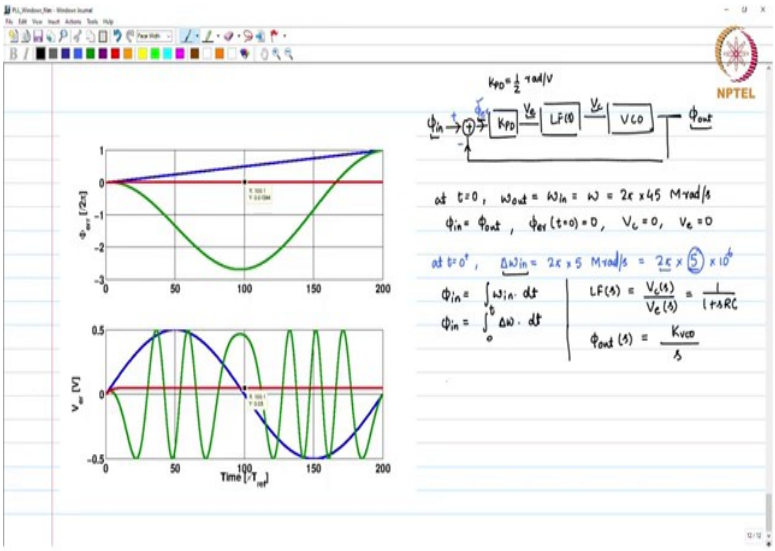

In the previous session, we looked at the operation of a PLL block diagram depicting the simple implementation of the PLL. Today, in this session, we will try to relate the small signal analysis of the PLL with respect to the full simulation of the PLL. So, now consider the previous example which we had. We have this small signal block diagram with our LF (s) and VCO. So now, I have some plots here. I will tell you how we relate these two things. So, assume this is a small signal diagram and that the frequency of the oscillator is the same as the frequency of the input.

So, at t = 0, we have the following:

$$\omega_{out} = \omega_{in} = \omega = 2\pi \times 45 \text{ Mrad/s}$$

There was no frequency error. Even the input phase and the output phase were matched. Thus, we have,

$$\varphi_{in} = \varphi_{out}, \varphi_{er}(t = 0) = 0, V_c = 0, V_e = 0$$

These are all the initial conditions. So, this is like we are talking about a PLL where the input and the output frequencies are same, there is no phase error to begin with, the error voltage and the control voltage are zero.

Now, in this case, we apply a frequency step at $t = 0^+$, you can say. I applied a frequency step at ω_{in}. So, I have the following:

$$\Delta\omega_{in} = 2\pi \times 5 \text{ Mrad/s}$$

You might be worrying that why it is $2\pi \times 5$ always. This is because I just want to give you an explicit number which is easy for calculation where this is 2π, this converts from frequency to radians and this is frequency. So, if you are asked the frequency in Hertz, this is like 5 MHz here. There is 5 MHz frequency error between the input and the output or if you want to convert into radians, it is 10π Mrad. So, just after t equal to 0, we applied a frequency step of 5 MHz or 10π Mrad at the input. Then, what is going to happen? If we assume that this particular system operates in a linear manner, then what are we going to have? This is plus, this is minus, the phase error is going to be with respect to the frequency error. So, as soon as we have the frequency error at the input, you are going to get the phase error.

So, you can analyze this particular thing. When I have a frequency error at the input, how is my input phase related to the input frequency? We know,

$$\varphi_{in} = \int \omega_{in}\, dt$$

So, if I apply a frequency step, effectively I am doing the following:

$$\varphi_{in} = \int_0^t \Delta\omega\, dt$$

That is how the input phase will keep on increasing. As the input phase keeps on increasing, you are going to have error voltage, you are going to have phase error, here you are going to have error voltage and finally control voltage and output phase will change.

So here, now, I will just write the gain of each block we know. Initially the phase error was zero. So, the PLL was locked. $K_{PD} = \frac{1}{2}$ rad/V. When the phase error is equal to zero, we have seen the gain of the phase error detector. The loop filter which we are choosing has transfer function given by,

$$LF(s) = \frac{V_c(s)}{V_e(s)} = \frac{1}{1 + sRC}$$

and $\varphi_{out}(s)$ is given by,

$$\varphi_{out}(s) = \frac{K_{VCO}}{s}$$

These are the transfer functions. So, you can analyze this block using the linear gain model, so, we will do it one by one. So, let us find out, from φ_{in} to φ_{out}, what is the gain in the closed loop.

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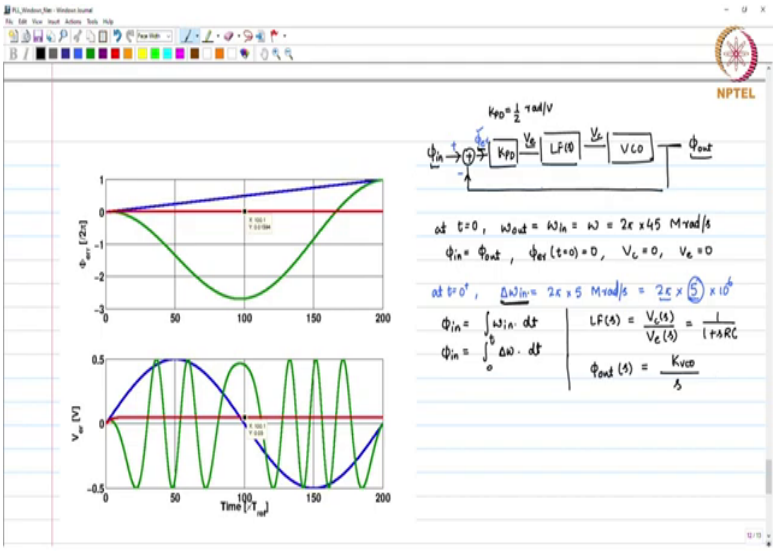

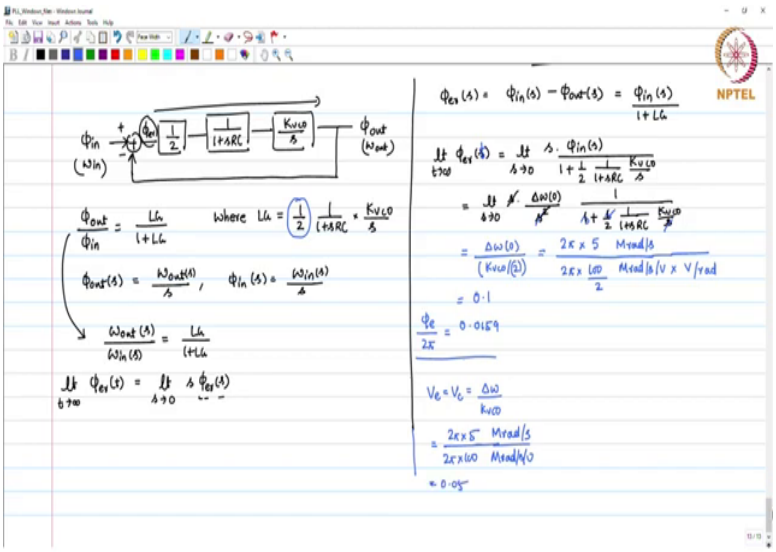

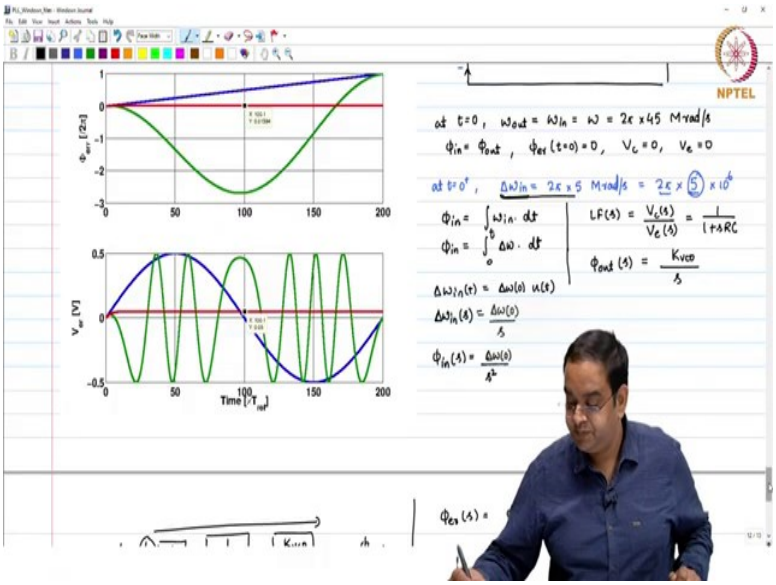

I will draw the loop gain model for this. So, given the PLL which you see in this particular case, the model for this is going to be, I am just writing in terms of gain, so, I have $\frac{1}{2}$, $\frac{1}{1+sRC}$, and $\frac{K_{VCO}}{s}$. This is φ_{in}, this is φ_{out}. One interesting thing you will find out here which is that this particular model or the small signal model is the same for ω_{in} and ω_{out}, it does not change. So, here I will first write between φ_{in} and φ_{out}. So, here I will have the small signal closed loop gain as,

$$\frac{\varphi_{out}}{\varphi_{in}} = \frac{LG}{1+LG}$$

The loop gain is equal to multiplication of all these blocks and is given by,

$$LG = \frac{1}{2}\,\frac{1}{1+sRC}\,\frac{K_{VCO}}{s}$$

We also know,

$$\varphi_{out}(s) = \frac{\omega_{out}(s)}{s}$$

$$\varphi_{in}(s) = \frac{\omega_{in}(s)}{s}$$

So, this gain model is the same as $\frac{\omega_{out}(s)}{\omega_{in}(s)} = \frac{LG}{1+LG}$. It is interesting to realize this.

Now, if we applied a unit step in frequency, where did we apply that? We said $\Delta\omega$ at t=0, you just gave the input frequency step, this input frequency step can be analyzed using this loop

and finally, I can calculate both the terms. So, what we want to know from all this analysis is that if I use the small signal model right now, the final error which I am going to get, when you apply any input, control voltage and error voltage will change, but as time passes by, you give it enough time in steady state when no more voltages or phase values are changing, you have reached the steady state. So, what will be this error value in steady state? So, what we are looking here is, as time t tends to infinity, what is my error value? You can find this error value using the final value theorem as follows:

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s\, \varphi_{er}(s)$$

where,

$$\varphi_{er}(s) = \varphi_{in}(s) - \varphi_{out}(s) = \frac{\varphi_{in}(s)}{1 + LG}$$

So, we got this and we applied a frequency step here to the system. So, I will write it in terms of the frequency transform.

$$\Delta\omega_{in}(t) = \Delta\omega(0)\, u(t)$$

$$\Delta\omega_{in}(s) = \frac{\Delta\omega(0)}{s}$$

This is the frequency change which you applied. So, the phase change which I am adding to my system is given by,

$$\varphi_{in}(s) = \frac{\Delta\omega(0)}{s^2}$$

So,

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s\, \frac{\varphi_{in}(s)}{1 + LG}$$

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s\, \frac{\varphi_{in}(s)}{1 + \frac{1}{2}\,\frac{1}{1+sRC}\,\frac{K_{VCO}}{s}}$$

$$\lim_{t\to\infty} \varphi_{er}(t) = \lim_{s\to 0} s\, \frac{\Delta\omega(0)}{s^2}\,\frac{1}{1 + \frac{1}{2}\,\frac{1}{1+sRC}\,\frac{K_{VCO}}{s}}$$

$$\lim_{t\to\infty} \varphi_{er}(t) = \frac{\Delta\omega(0)}{\frac{K_{VCO}}{2}}$$

So, we applied a frequency error. In response to the frequency error, the phase error changes.

So, let us just calculate. The error which we applied in this case was only 5 Mrad/s.

$$\lim_{t\to\infty} \varphi_{er}(t) = \frac{\Delta\omega(0)}{\frac{K_{VCO}}{2}} = \frac{2\pi \times 5\ \text{Mrad/s}}{2\pi \times \frac{100}{2}\frac{\text{Mrad}}{\text{s}}/\text{V} \times \text{V/rad}} = 0.1$$

$$\frac{\varphi_{er}}{2\pi} = 0.0159$$

So, we did all this math and now if I say that this is the value after doing small signal analysis, I go and simulate my PLL in the same way as we did in the previous session, you see that $\frac{\varphi_{er}}{2\pi} = 0.01594$. This is the thing which I would like to emphasize that in the previous example, when we had the phase error, frequency error to begin with, we went through time domain analysis and we figured out what will be the actual error voltage, control voltage and so on and you understood the different plots which we had.

In this case, we adopted a different approach and the approach was that you start with the small signal model of the PLL, you apply some input, based on the input, you calculate the phase error and you try to match the phase error and frequency error, and the error voltage that you have with the transient simulations. And what you find here is, $\frac{\varphi_{er}}{2\pi} = 0.01594$, this is what we calculated and the error voltage if you look at, this is 0.05. It will be easy for you to recall that,

$$\mathrm{V_e} = \mathrm{V_c} = \frac{\Delta\omega}{K_{VCO}} = \frac{2\pi \times 5\ \text{Mrad/s}}{2\pi \times 100\ \text{Mrad/s/V}} = 0.05\ \text{V}$$

Is it not interesting that you did such complicated time domain simulations, and you found that voltage whereas when we did this small signal analysis, we found the final error voltages and currents?

So, now the question which we have is that whether we should go with the time domain analysis or this small signal model is good to do all kinds of analysis, whether we apply a phase change or frequency change or there are any limitations. So, these are the things which we need to understand and let me tell you the small signal model of the PLL is a simplified model of the PLL. It does not have any limitations so far.

In this particular model, whatever phase error I need, I will get. Whatever voltage I need, I will get. This is because as per this analysis, if we applied a larger frequency error, we would have got a larger error voltage, there is no limitation to it. But, in actual model, there are limitations.

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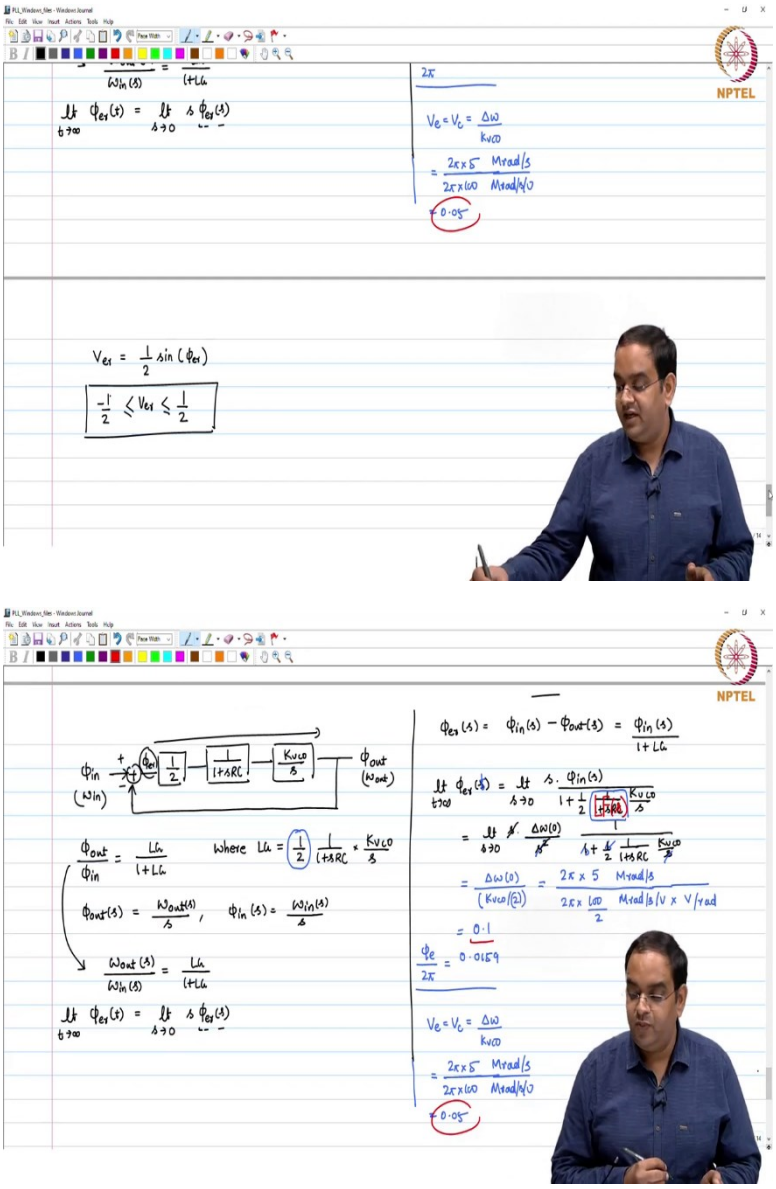

What kind of limitations are those? Well, to begin with, I can tell you that just think about it, you calculated that,

$$V_{er} = \frac{1}{2}\sin(\varphi_{er})$$

So, if this is the case that the error voltage is like this, then you will surely know that,

$$\frac{-1}{2} \leq V_{er} \leq \frac{1}{2}$$

The error voltage is always bounded between $\frac{-1}{2}$ and $\frac{1}{2}$, it cannot go beyond this limit.

If your small signal model somehow tells you that $V_{er} > \frac{1}{2}$ or $V_{er} < \frac{-1}{2}$, that means you should not take that as a value, use it, say that the PLL locks and this is the final error voltage or control

voltage. No, that is not the case. There is a hard limit on the error voltage which you can have in this particular implementation.

How we can overcome that, that we will see in the upcoming sessions. The other important thing here is that if I change the loop filter transfer function, then you know that the final value of the error voltage which I am going to have actually depends on the loop filter DC component because we substituted s as 0 here. So, the loop filter plays a very important role in getting the final value. So, we will look at the loop filter also and how the loop filter restricts our analysis or the final PLL output. Thank you.