Phase-Locked Loops
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Lecture − 63
Analog/Digital Hybrid PLL: Part I

Hello, welcome to this session. In the previous session, we looked at the noise transfer functions for different noise sources in a digital PLL. Also, we summarized that the TDC quantization noise and the power consumption is one of the problems in digital PLLs.

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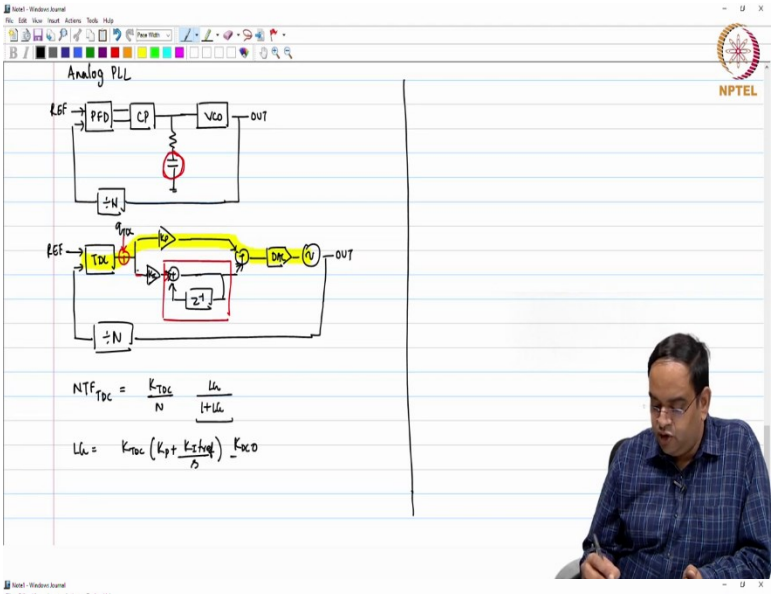

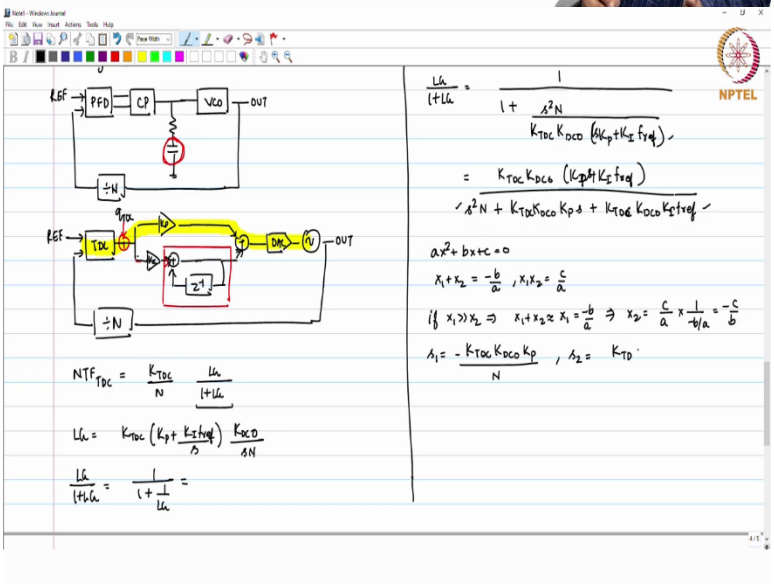

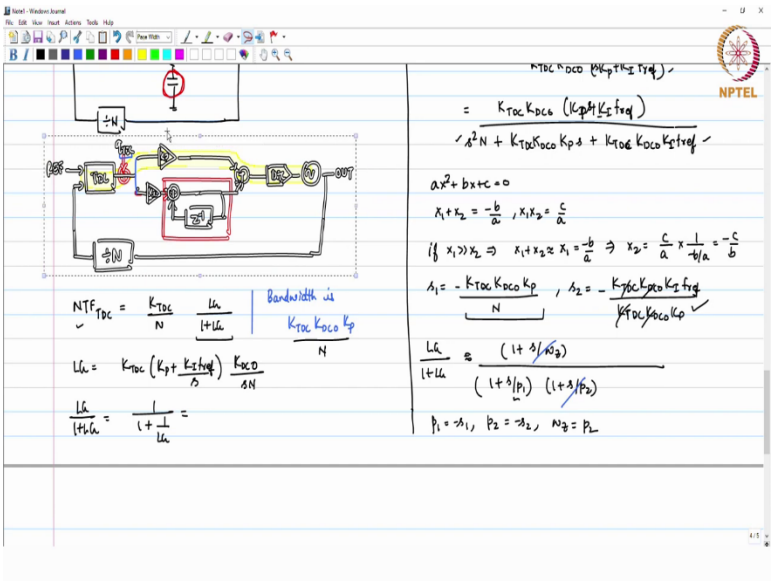

So, now, we would like to do something which helps us to reduce the effect of the quantization noise of the TDC. So, then we recall that in analog PLL, we did not have any quantization noise while measuring the phase error while here it has become a serious challenge. So, let us just compare the two. Analog PLL, when we had PFD, at that time the output of the PFD goes to charge-pump, charge-pump output goes to an analog loop filter like this.

Let us keep only one capacitor and then you had a VCO, this is your feedback signal. So, in contrast to this, the digital PLL is something like this. You have a TDC which gives you quantization error actually. The output of the TDC goes to digital loop filter and I need to just put the digital loop filter in two parts, that is easier to understand and then you have K_I, + here and this with z^{-1} and it is like this.

You have the adder and so on. The output of this goes to your DAC and VCO, this is what we have. Now we will make a distinction between the two by reiterating the exact reason why we went to digital PLL. We went to digital PLL for the fact that this particular loop filter including R and C, this capacitor was taking a lot of area and well, current charge-pump mismatch and resistance and so on things were there. Here you can say that integration part of the capacitor is actually done by this block or very specifically speaking, it is done by this block.

So, if we want to replace the capacitor, if we somehow just replace that particular capacitor part with the integrator, our area problem will be solved. But we have to give the digital bits, that is why we had TDC.

Now, the TDC quantization noise which you are seeing at the output, that is mostly because of your proportional path gain. So, what transfer function did we have for our TDC? It is true that we added quantization noise here. This was our q_{TDC}. So, we have,

$$NTF_{TDC} = \frac{K_{TDC}}{N}\frac{LG}{1+LG}$$

This closed loop transfer function if you are looking at $\frac{LG}{1+LG}$, the bandwidth of this closed loop transfer function is actually the unity gain frequency of your loop gain. It is very close to that. How? Well, you had loop gain as,

$$LG = K_{TDC}\left(K_P + \frac{K_I f_{ref}}{s}\right)\frac{K_{DCO}}{sN}$$

This was your loop gain.

So, we get,

$$\frac{LG}{1+LG} = \frac{1}{1+\frac{1}{LG}}$$

So, I am just trying to give you the bandwidth by handwaving on these expressions. So, we wrote $\frac{LG}{1+LG}$, this closed loop expression as $\frac{1}{1+\frac{1}{LG}}$. So, we get,

$$\frac{LG}{1+LG} = \frac{1}{1+\frac{s^2 N}{K_{TDC}K_{DCO}\left(sK_P + K_I f_{ref}\right)}}$$

This is what we have.

So, if this is the case that we have here, you can just look at it. This will give you a closed loop zero also and we know that we had it earlier. So, we get,

$$\frac{LG}{1+LG} = \frac{K_{TDC}K_{DCO}\left(sK_P + K_I f_{ref}\right)}{s^2 N + K_{TDC}K_{DCO}K_P s + K_{TDC}K_{DCO}K_I f_{ref}}$$

This is what we have. Now, we can have an approximation and the approximation is that the two poles of this denominator, they are quite far away and if the two poles of this denominator which is like $ax^2 + bx + c = 0$. The poles of this quadratic equation are given by,

$$x_1 + x_2 = -\frac{b}{a}$$

$$x_1 x_2 = \frac{c}{a}$$

If I assume that $x_1 \gg x_2$, then I can say that,

$$x_1 + x_2 \approx x_1 = -\frac{b}{a}$$

and this implies that

$$x_2 = \frac{c}{a} \times \frac{1}{-\frac{b}{a}} = -\frac{c}{b}$$

So, the two poles can approximately be found in this manner which means that the two poles here, from this equation if the poles are far away in the closed loop, they will be given by,

$$s_1 = -\frac{K_{TDC} K_{DCO} K_P}{N}$$

$$s_2 = -\frac{K_{TDC} K_{DCO} K_I f_{ref}}{K_{TDC} K_{DCO} K_P}$$

$$s_2 = -\frac{K_I f_{ref}}{K_P}$$

So, the above transfer function which we have that can be written as,

$$\frac{LG}{1 + LG} = \frac{\left(1 + {}^{s}/_{\omega_z}\right)}{\left(1 + {}^{s}/_{p_1}\right)\left(1 + {}^{s}/_{p_2}\right)}$$

where,

$$p_1 = -s_1, p_2 = -s_2, \omega_z = p_2$$

The ω_z value, the zero frequency, you look at the zero frequency that is at $\frac{K_I f_{ref}}{K_P}$, ω_z, $\frac{K_I f_{ref}}{K_P}$ and this is also $\frac{K_I f_{ref}}{K_P}$. So, ω_z is same as p_2.

If that is the case, what you see is in this transfer function that these two, this is approximate, no one is denying that but it works quite well. So, you have p_1 as a pole. What was this earlier? This was the unity gain frequency for the loop gain. So, coming back to our NTF_{TDC}, the bandwidth of this transfer function is same as the unity gain bandwidth which is $K_{TDC}K_{DCO}K_P$.

Why I derived this particular value? The reason is that if you have the quantization noise, the quantization noise goes through this path, the path which is highlighted here in yellow and you have a large gain. You have a large bandwidth, so you have a large gain and when you have a large gain, you actually have a lot of noise at the output.

So, the only way we can reduce the contribution is by reducing the bandwidth. K_{TDC} given the number of bits in the TDC, you cannot do anything. K_{DCO} is also limited to be tuned. K_P is something which you can control. So, you have to reduce the gain. So, what is the minimum gain we can have? The minimum gain which we can have to reduce the contribution of this quantization noise at the output is actually zero. There is nothing else you can, nothing better which you can do more than that.

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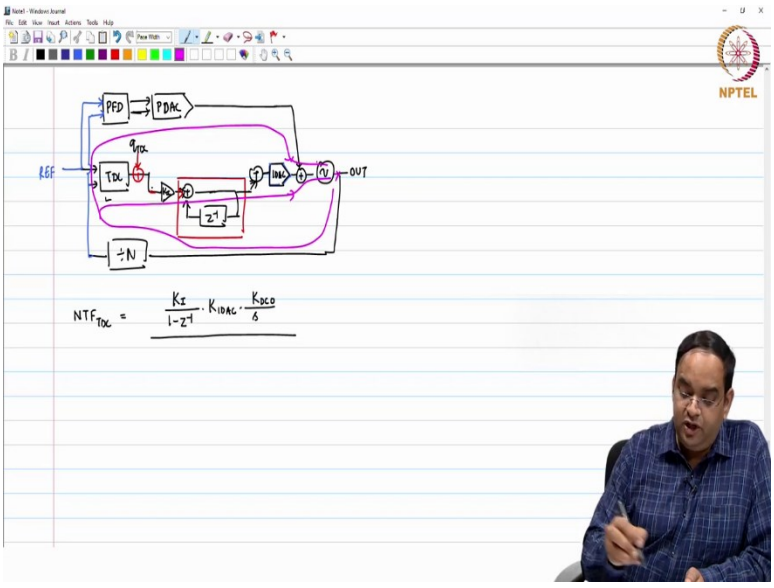

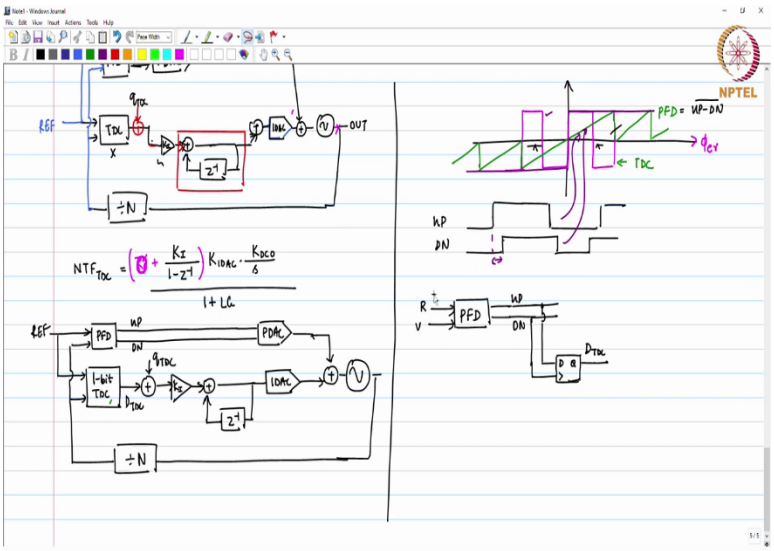
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TDC
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OUT
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PFD = UP - DN
TDC
UP
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R
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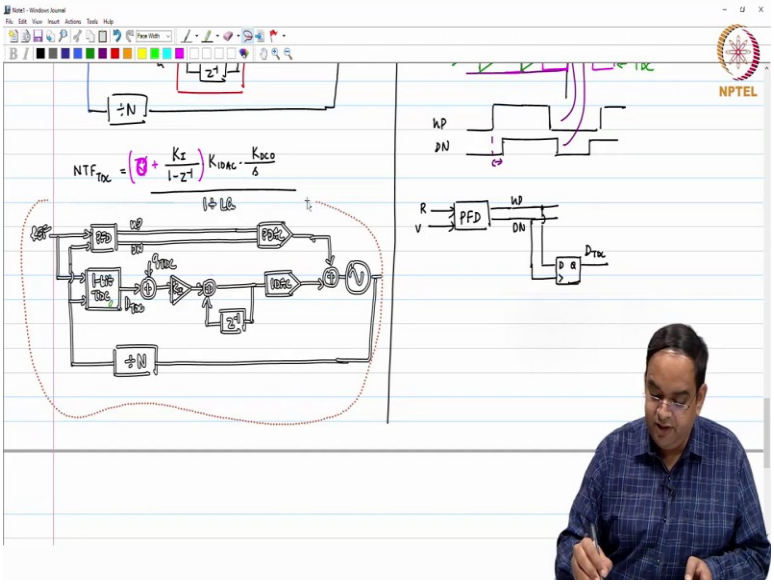
DTDC
1-bit TDC
PDAC
IDAC
DCO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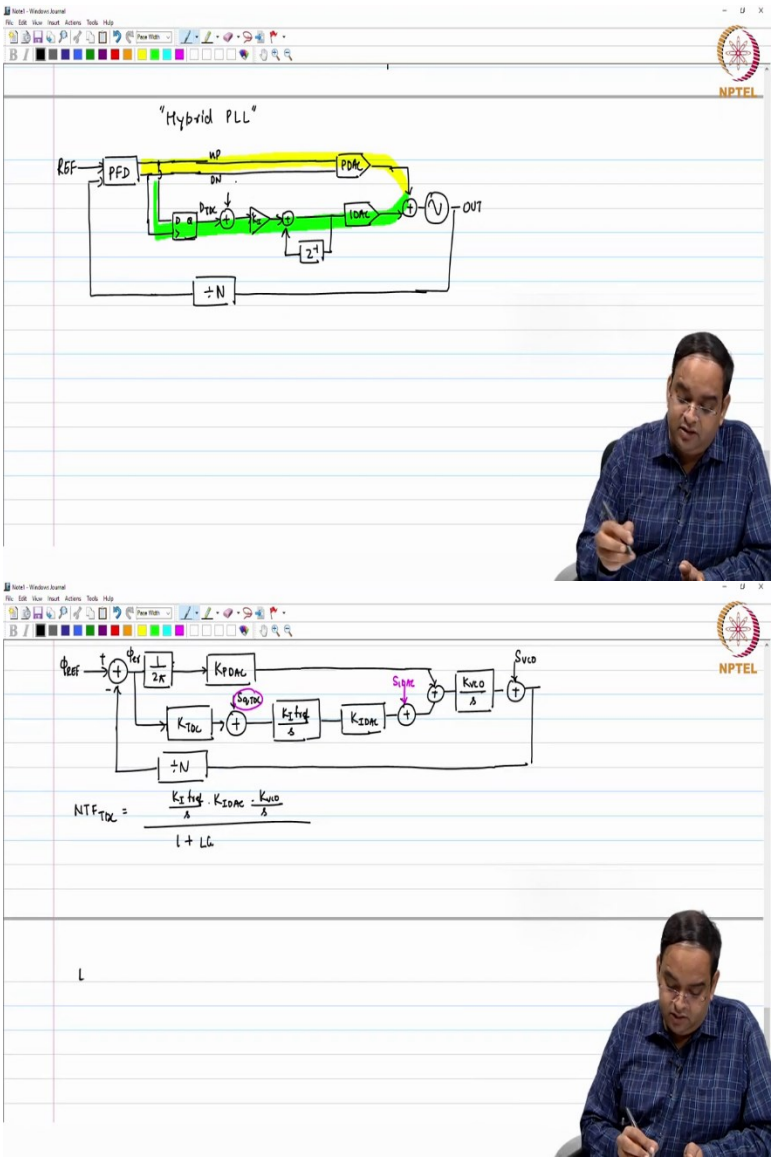

So, if I do that, let us bring this here. So, as I said that the minimum gain which I can have for the quantization noise from the proportional path, that is zero. So, I just removed the path altogether, make it zero. What is the big deal? Well, if I do this, I have two integrators in the path and when I have two integrators in the path, then it will also become a problem, the loop is not stable.

So, then I say no see with the analog PLL, we had proportional path and with respect to that proportional path, there was no quantization error in the phase error detection. So, we will try to do something like that. In measuring the phase error here using the PFD, there was no quantization error.

So, we go and insert this PFD and this reference signal is same, going to both the cases and feedback signal is also going to be same, like this. So, this gives me phase error. Now, this phase error I have to somehow control my VCO. So, you can say you had this DAC output already, the previous one, this is nothing new which you have seen.

This DAC output, you add the proportional path gain somehow. This PFD output has to be converted to some using some DAC because the summation is happening with the DAC voltage or current. PFD gives you UP and DN, we do not know how to do it right now, but we are just assuming if it is possible, they come to a DAC.

I call this DAC as PDAC because it comes in the proportional path and then it gets added up here. The previous DAC is now coming only in the integral path. So, I start calling this as IDAC. Now, you look at this particular PLL, well, it is having analog phase error detector or PFD and then it has DAC which controls the VCO.

In the integral path, it has a TDC and TDC quantization noise appears only in the integral path which is like having a lower gain. How is it having a lower gain? Now look at it. The NTF_{TDC} now has the forward path gain with this part. So, forward path gain is only this which is your $\frac{K_I}{1-z^{-1}} K_{IDAC} \frac{K_{DCO}}{s}$.

This is the forward path gain and the closed loop gain which you are going to see the loop gain, the loop gain is for the whole loop. So, what is the loop gain? I will break the loop near either the phase error detector or at the output. I break the loop here, I go back and see what comes back. Well, it comes through two paths. It comes like this and it also comes like this. It gets added up and then finally after adding up, it appears here. So, loop gain is not only for the integral path, it is for both the paths. So, you are going to see the combined loop gain and what we assume is that we want to keep the same loop gain or the loop gain which helps us to minimize the output jitter. So, we have,

$$NTF_{TDC} = \frac{\frac{K_I}{1-z^{-1}} K_{IDAC} \frac{K_{DCO}}{s}}{1 + LG}$$

So, you have this. Just consider this particular transfer function with the previous one where you had, it is the same thing but initially you had this particular K_P in the numerator also. Previously

it was this, now this has become zero. So, when this becomes zero, your NTF_{TDC} actually your noise contribution at the output of the TDC reduces.

Now, well, this is good. It helps us to reduce the TDC quantization noise contribution to the output. This problem is solved but the other problem that your TDC if you want, still there is some quantization noise and if you want to reduce that quantization noise, then you have to reduce q_{TDC} and there was a power versus quantization noise trade-off.

So, you can say previously the quantization noise contribution to the output was much more. It has reduced but it has not become zero, it is not like your PFD stuff. So, here what one can do is one can try to reduce the power consumption in the TDC, reduce your K_I gain to reduce the contribution to the output.

So, in order to make our PLL more power efficient, what we can do is we can go ahead and use a 1-bit TDC. Whatever TDC you are using, now it seems like you are measuring the phase error in two different forms. One you are using through PFD, other you are using through TDC. If I do that and that too using let us say with our 1-bit TDC or it is just an example, 1-bit, you write it first, it is 1-bit TDC.

So, here we feed the reference to both. One thing which is going to hurt that to measure the same phase error, why do we need two blocks? Well, one, we need a digital input, that is why we need two blocks. So, this goes through your K_I or you can say you have quantization noise with the TDC getting added here.

You go through K_I, then you have the integral path which is like this with z^{-1} coming back here with your IDAC and outputs of this, they go to because PFD gives you UP and DN, I have to somehow convert. I do not know how but we will find it out. PDAC and IDAC, you have an oscillator, they are getting summed up before you feed into the oscillator and then you have VCO. This is your feedback path, $\div N$, here you add q_{TDC}, this is your reference. So, now, the same phase error is measured using PFD and 1-bit TDC and you do add the quantization noise at the output.

Now, if we try to reduce the power consumption in the TDC by using 1-bit, we know that the range of this TDC is very limited. It is like this particular TDC can measure phase error only between

$-\pi$ and π. So, this is what we have. This is a TDC, 1-bit TDC output, so, with respect to phase error at the input.

In contrast to this, so, let me first write our TDC output as D_{TDC} which is still whether it is 1-bit or it is 10-bit, it is the same. The signal name here is the same. So, this is $-\pi$, this is π. Such kind of phase error detector limits your pull-in range because you know for positive phase error, your TDC output is actually becoming negative with an average value of 0 for 0 to 2π. This is going to create a problem.

In contrast to this, you have seen earlier that the PFD output has been something like this. So, your PFD output has been like this which was giving us a proper, this is your PFD output, this is your TDC output. So, now, the question is this 1-bit TDC which helped in reducing the power consumption in the TDC and having TDC only in the integral path helps us to reduce their quantization noise contribution to the output, but now it is limited by the pull-in range for the oscillator for the PLL.

So, what we need to think about is that how I can extend the range of the 1-bit TDC. So, now, if you think about it, the output of your PFD which is UP and DN signal. The average of UP and DN signal is V_{PFD} output. This is nothing but $\overline{UP - DN}$.

If the phase error is positive, in that case $\overline{UP - DN}$ is always going to be positive. If your phase error is negative, $\overline{UP - DN}$ is always negative and these UP and DN signals are independently, they are clock signals, they are not the voltage signals by the way, they are not like analog voltages, they are proper clock signals like this.

So, if I can convert, somehow I can convert this magenta one which is our TDC output for positive and negative phase error, if I can convert like this, that is the best option because then, well, you will have the quantization noise but you will not have a lot of quantization noise because it is a 1-bit but for positive phase error, you will always get positive, for negative phase error, you will always get negative. There will not be any pull-in range issue. So, what we can do is you try to think that this PFD output is always positive and it is actually these two signals are giving you this PFD output and these two signals are clock signals.

If this timing difference is positive, they give positive. So, what we want is if phase error is positive, for TDC we always want only positive, what we can do is we can take these PFD outputs, you have reference and your feedback signal, PFD outputs are UP and DN and these PFD outputs can be used to clock the 1-bit TDC.

So, here, just this is what you have. I will just take these signals UP and DN and these signals go to 1-bit TDC which is nothing but like a D flip-flop. So, this is clock, this is D, this is Q, you get an output and now this output I call as D_{TDC}. So, you look at it, if here my UP comes first, that is at D, my DN comes later which is here.

So, DN is going to sample the UP, if the phase error was positive, I will get D_{TDC} as 1. If my phase error would have been negative, something like this, then I would get 0. So, you get 1-bit output at D_{TDC} while having the range which is the same as your PFD. It is infinite range. So, now, we can include this particular block in our PLL.

So, previously, we had this as the PLL where we tried to reduce the contribution of the quantization noise of the TDC. Now, we have moved a step further and we are removing this TDC from here because you still have to, you are having trouble with the pull-in range.

We get this, so, now you have these UP and DN signals, they go here, D_{TDC} output is this, this is your feedback signal and this is your reference, this is output. Now this particular PLL is called as a hybrid PLL because it has analog and digital both.

So, what you see is in the proportional path, to highlight it, I will do that. In the proportional path, your phase error directly comes through PDAC and the summing voltage in the integral path, what you see is you get the phase error digitized to 1-bit, goes to the integral path and comes here. So, now, this particular PLL has unlimited pull-in range. It is not limited by any sort of TDC issues.

Now, well, we are done with this hybrid PLL block diagram. Now, let us look at the quantization noise and other stuff, the noise sources which we have now. So, I will just write $S_{q_{TDC}}$. So, for your small signal block diagram, I have to measure my phase error between the reference and the feedback, this is +, this is -, this is my phase error, PFD block we have seen, it is $\frac{1}{2\pi}$, that is the gain. Then you have PDAC.

So, right now, you get this whatever the phase error you get, it goes to PDAC, PDAC has gain, let us call that as K_{PDAC}, goes here. The output of the PFD, it comes, the phase error, whatever phase error you have, that phase error goes through the TDC. It has the TDC gain, K_{TDC}, then you add the TDC quantization noise $S_{q_{TDC}}$. It goes through the integrator which is $\frac{K_I}{1-z^{-1}}$.

So, I will write here $\frac{K_I f_{ref}}{s}$. Then it has the DAC gain which is K_{IDAC}. These two add up here. When you have the DAC gain, you can actually have the DAC quantization noise $S_{q_{DAC}}$ and this $S_{q_{DAC}}$ actually adds here and then you have $\frac{K_{VCO}}{s}$, this comes back in the feedback. This is the small signal block diagram of the hybrid PLL. Well, there is the phase noise of the VCO which I will add, S_{VCO}.

So, now, you see that the TDC quantization noise is not present in the proportional path at all. So, with the given noise sources, we can find the noise transfer function for both of these and as I told earlier, the NTF or the noise transfer function for the TDC, this is quite important. The DAC quantization noise, well, whatever you have let us just write that S_{IDAC}, this quantization noise will come, and this is going to be band pass filtered here.

So, when we are looking at different contributions, we need to just write our NTF, what we are going to have is NTF_{TDC}. And we wrote that earlier, so, we have,

$$NTF_{TDC} = \frac{\frac{K_I f_{ref}}{s} \times K_{IDAC} \times \frac{K_{VCO}}{s}}{1 + LG}$$

and in this case, the loop gain is going to be, is a little complicated.

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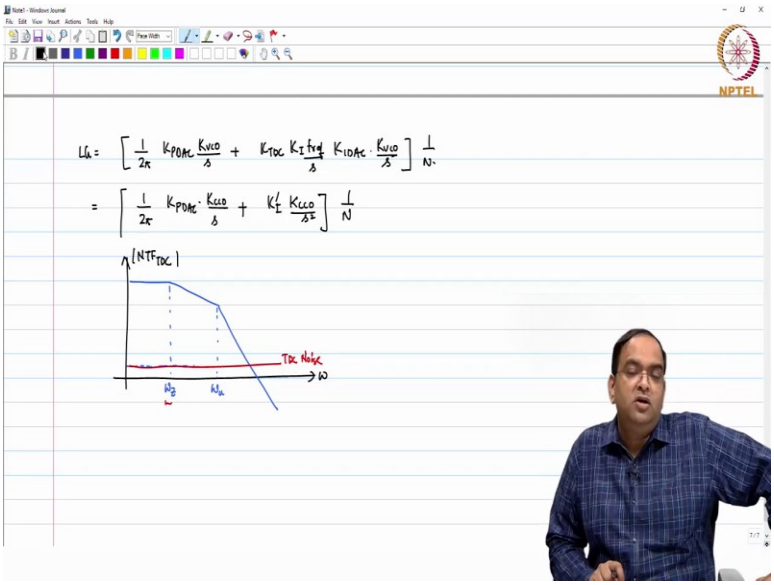

So, I am going to break the loop here. The loop gain is going to be,

$$LG = \left[\frac{1}{2\pi} K_{PDAC} \frac{K_{VCO}}{s} + K_{TDC} K_I \frac{f_{ref}}{s} K_{IDAC} \frac{K_{VCO}}{s}\right] \frac{1}{N}$$

So, what I see here is now, it is quite common to, when you are implementing in this manner, your control of the oscillator is not the voltage control because it is easy to sum up the current.

So, we may use a current controlled oscillator. As I told earlier, you can have a voltage controlled oscillator or you can have a current controlled oscillator. Using a current controlled oscillator will be easy here. So, I am just writing it in a different way that you have,

$$LG = \left[\frac{1}{2\pi} K_{PDAC} \frac{K_{CCO}}{s} + K_I{}' f_{ref} \frac{K_{CCO}}{s^2}\right] \frac{1}{N}$$

Here, $K_{TDC} K_I K_{IDAC} = K_I{}'$. If you plug in all these values in your NTF_{TDC}, what you are going to find that this NTF_{TDC} with respect to ω, the NTF_{TDC} with respect to ω, this is going to be low pass transfer function and this particular low pass transfer function has two zeros, two poles like this.

And the first pole will appear at your zero frequency ω_z and the second pole will appear at the unity gain frequency for the loop gain. So, this is what you get and then the TDC quantization noise which you have, that quantization noise is actually flat. So, it is getting filtered by TDC, this is TDC noise, it is going to get filtered by your low pass transfer function here which is where the

pole frequency is, the dominant pole is coming is actually the zero frequency. Previously, we have seen that the dominant pole while filtering TDC's quantization noise when you have the TDC quantization noise going through proportional and integral path was the unity gain bandwidth.

Now that has reduced to the zero frequency for the same PLL. So, TDC noise gets more filtered. So, in this way, we can design now choosing all these parameters, we can get the same PLL performance as we were getting for the analog. Now, how to control the oscillator and other things, these are the things which we need to look at. We will see in the next session. Thank you.