## **Phase-Locked Loops Dr. Saurabh Saxena Department of Electrical Engineering Indian Institute of Technology, Madras**

## **Lecture − 6 Time Domain Analysis of a Simple PLL**

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Previously, we have seen the simple implementation of the PLL circuit. So, just to recollect, that simple implementation was with the help of a mixer, a simple low pass RC filter followed by an oscillator. This is what we saw earlier and at the end of the last session, we actually found the small signal block diagram for this simple implementation. In this session, we would like to see that how these two blocks are related with the help of an example. So, this is  $V_{in}$ , this is Vout, you have R and C here, this is V<sup>e</sup> and this is the control voltage of the oscillator. And we have seen the relationship between  $V_e$ ,  $V_{in}$ ,  $V_c$ , and all other variables.

The corresponding small signal block diagram which we drew in the last session was this. You have phase error detector which takes input  $\varphi_{in}$ , this is positive, this is negative, and it goes through a block whose gain is  $K_{PD}$  followed by the loop filter which is modelled using R and C here with transfer function  $LF(s)$  which is followed by the VCO whose transfer function is Kvco  $\frac{1}{s}$ , and the output of this is fed back, this is  $\varphi_{out}$ .

Now, one is the actual implementation of the PLL, the other one is small signal model of the PLL or you can say the linear gain model of the PLL, as you see on the left. Now, to understand that how these things work, we will take an example.

Example:

$$
V_{in} = 1.\sin(\omega_{in}t)
$$

We will consider the phase offset as 0 and the amplitude as 1, just to simplify our calculation.

$$
V_{out} = 1.\cos(\omega_{out}t)
$$

At  $t=0$ ,

$$
\omega_{in} = \omega
$$

$$
\omega_{out} = \omega - \Delta\omega(0) = \omega_{fr}
$$

This is the frequency of the oscillator at time  $t = 0$ . You can also call this as the free running frequency of the oscillator. So, as you see, at time instant  $t = 0$ , the input and the output are not frequency matched.

$$
K_{VCO} = 2\pi \times 100 \times 10^6
$$
 rad/sec  

$$
K_{VCO} = 2\pi \times 100
$$
 Mrad/sec

These are just the ways in which we write. So, initially there is frequency error between the input and the output frequencies. So, if I write at any given time that what is the frequency error, that will be  $\omega_{in} - \omega_{out}$ .

Now, to understand this particular block, we will do part by part. First, let us see, if we only focus on the phase error detector part. So, when we only focus on the phase error detector part, it means that we are looking at the phase error detector in open loop. So, you have  $V_{in}$ , and you have V<sub>out</sub>. If this is in open loop, in the PLL it is not in open loop, but to understand that how this closed loop works, we will go part by part.

So, here, as per our discussion in the previous session, the error voltage is given by,

$$
V_e = \frac{1}{2} \left[ \sin\left( (2\omega - \Delta\omega)t \right) + \sin(\Delta\omega(0)t) \right]
$$

The phase error between the input and the output is given by,

$$
\varphi_{er} = \int \omega \, dt - \int (\omega - \Delta \omega(0)) \, dt
$$

So, if you treat the mixer in open loop and you have a frequency error between the input and the output signals, you are going to get the error voltage given here, where one component is at  $2\omega - \Delta\omega$  and the other component is  $\Delta\omega(0)$ . The phase error is given by.

$$
\varphi_{er}=\Delta\omega(0)\;t
$$

The phase error would linearly increase with respect to time. When I have frequency error between the input and the output signal, phase error appears to be linear,  $\Delta\omega(0)$  t.

So, if I am not controlling this in the loop, then  $V_e$  will be sinusoidal in nature and the phase error will be linear in nature. Now, the control voltage which we have here, this control voltage is the filtered version of the error voltage. In this particular application, let us say I have this RC filter here and for the RC filter this is  $V_e$  and this is  $V_c$ , just treat this as standalone. If I feed this particular  $V_e$  to my system and  $\Delta\omega(0)$  happens to be much lesser than the filter bandwidth, and  $2\omega - \Delta\omega(0)$  is much greater than the filter bandwidth, thus, we have,

$$
\Delta \omega(0) \ll \frac{1}{RC}
$$

$$
2\omega - \Delta \omega(0) \gg \frac{1}{RC}
$$

Then, what are you going to see at the output of the filter?

$$
V_c(t) = \frac{1}{2}\sin(\Delta\omega(0) t)
$$

So, the error voltage has both the frequencies,  $2\omega - \Delta\omega$  and  $\Delta\omega(0)$  but the control voltage has only one frequency standalone.

Now, if this is the control voltage and you have an oscillator which is shown in this block, VCO, this is  $V_c$  and we know what is  $V_{out}$ , but the way the frequency is controlled at any given time is given by,

$$
\omega_{out}(t) = \omega_{fr} + K_{VCO} V_c
$$

$$
\omega_{out} = \omega - \Delta\omega(0) + \frac{K_{VCO}}{2}\sin(\Delta\omega(0)t)
$$

So, what you see here is that the output frequency will change if I feed in the control voltage as given here. In response to this output frequency, the output phase is given by,

$$
\varphi_{out}(t) = \int \omega_{out} dt
$$

$$
\varphi_{out}(t) = \left(\omega - \Delta\omega(0)\right)t + \frac{K_{VCO}}{2}\int \sin(\Delta\omega(0)t) dt
$$

You will get the output phase like this. So, what we are doing here is, we are breaking this particular PLL into different parts and we look at each part in an open loop. Later, we are going to close the loop and see what happens in the closed loop. This is important to understand what is happening at each node. So, we have seen with the phase error detector, we have seen with the loop filter and then we have seen with the output phase.

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So, given this output phase, the phase error at any given time is given by,

$$
\varphi_{er}(t) = \varphi_{in}(t) - \varphi_{out}(t)
$$

$$
\varphi_{er}(t) = \omega t - (\omega - \Delta \omega(0))t - \frac{K_{VCO}}{2} \int \sin(\Delta \omega(0)t) dt
$$

You may ask a question that how this will remain at  $\Delta\omega(0)$  all the time. Well, it will not remain at  $\Delta\omega(0)$  all the time, this is just in the beginning when the loop is open. As you close the loop, the argument of this will keep on changing. But, we are just trying to understand what happens in each case. So, the phase error is given by,

$$
\varphi_{er}(t) = \Delta\omega(0) t - \frac{K_{VCO}}{2} \int \sin(\Delta\omega(0)t) dt
$$

So, you see that the phase error in response to the phase accumulated by the VCO has two terms, one is linear and the other is an integral of the sin wave which will be periodic in nature. Now, I told each of these things in open loop, and when I close the loop, I will see some kind of response which I am going to show you here. So, what I do here is I plot  $\frac{\varphi_{er}}{2\pi}$ . So, let me just write it. I plot here phase error at any given time divided by  $2\pi$  for different cases and I also plot  $V_e$  and other voltages. So, let us see, one by one.

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So, in this case, the phase error increases linearly with time which is  $\Delta\omega(0)$  t. So, the curve which you see is the blue one. When I highlight, this is the curve which is increasing linearly with time. And I am plotting  $\frac{\varphi_{er}}{2\pi}$ , so, what you see is that the output value is 1 in place of being  $2\pi$  or  $3\pi$  or so on.

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The next one is the error voltage which you see here as  $\frac{1}{2}$  $\frac{1}{2}$ sin( $\Delta\omega(0)$  t). So, I plot that in the bottom figure and you see that this error voltage is actually sinusoidal in nature. I am removing the component  $\frac{1}{2}$  $\frac{1}{2}$  sin((2 $\omega - \Delta \omega$ )t) because I know that this component is going to be filtered off by the loop filter. So, that is the blue component. Then, in response to that control voltage, I change the frequency and when I change the frequency, I get the phase error which is shown here. This particular phase error in response to the change in the control voltage as per the phase error, you get a new phase error which is shown here. It has a linear term and a sinusoidal term. So, then I again plotted this phase error term and what you see is something like this, it is periodic in nature. So, I will just do it like this. This is periodic in nature. So, you have a linear component and you have this component. All these things were in open loop and in response to this phase error now, you are going to have the error voltage given by,

$$
V_e(t) = \frac{1}{2}\sin(\varphi_{er}t)
$$

So, in response to the phase error which is periodic in nature as shown here, I again plotted the error voltage which is shown by the green curve. So, all the things which I am plotting with respect to time, they are like treating different blocks of the PLL in parts. When I close this loop, think about it, when you have a frequency error, you get voltage error, this voltage error changes the control voltage which is going to change the  $\omega_{out}$  which again changes the error and it is in negative feedback. So, finally, it will try to reach the case where  $\omega_{out} = \omega_{in}$  and that is going to happen when,

$$
\omega_{out} = \omega_{in} = \omega - \Delta\omega(0) + K_{VCO}V_c = \omega
$$

$$
V_c = \frac{\Delta\omega(0)}{K_{VCO}}
$$

When you reach this control voltage, you will compensate for the frequency error initially. What was this control voltage? This particular control voltage was given by,

$$
V_c = \frac{1}{2}\sin(\varphi_{er})
$$

$$
\varphi_{er} = \sin^{-1}\left(\frac{2 \Delta \omega(0)}{K_{VCO}}\right)
$$

So, you see that two things settle here in closed loop. The one thing which settles here is, you see that it comes from here and it settles at some value and for error voltage also, you see that this settles in some time. So, this is the closed loop. The red curves which you are seeing are

from closed loop simulations. So, what you can find from here is that once you reach the control voltage which compensates for the frequency error, at the same time, you will also have certain phase error which is non-zero in this particular stage.



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To verify, simply you can think about it that initially, the example which I chose here was such that  $\omega = 2\pi \times 50$  Mrad/s, and  $\Delta\omega(0) = 2\pi \times 40$  Mrad/s. The initial analysis is for any value but for the example which I plotted here,  $\Delta\omega(0) = 2\pi \times 40$  Mrad/s.

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So, based on the frequency error, the control voltage is given by,

$$
V_c = \frac{\Delta \omega(0)}{K_{VCO}} = \frac{2\pi \times 40 \text{ Mrad/s}}{2\pi \times 100 \frac{\text{Mrad}}{\text{s}}/V} = 0.4 \text{ V}
$$

Here,  $K_{VCO} = 2\pi \times 100$  Mrad/s/V. So, you see this voltage is 0.4 Volts and the error voltage settles to this voltage of 0.4 Volts. Now, this particular phase error happens to be sine inverse, you can calculate with respect to this value, and you will find that  $\frac{\varphi_{er}}{2\pi} = 0.1476$ . So, what we understand from this particular analysis is that given the frequency error, how the PLL locks, how the waveforms at different parts of this PLL block diagram will look here.