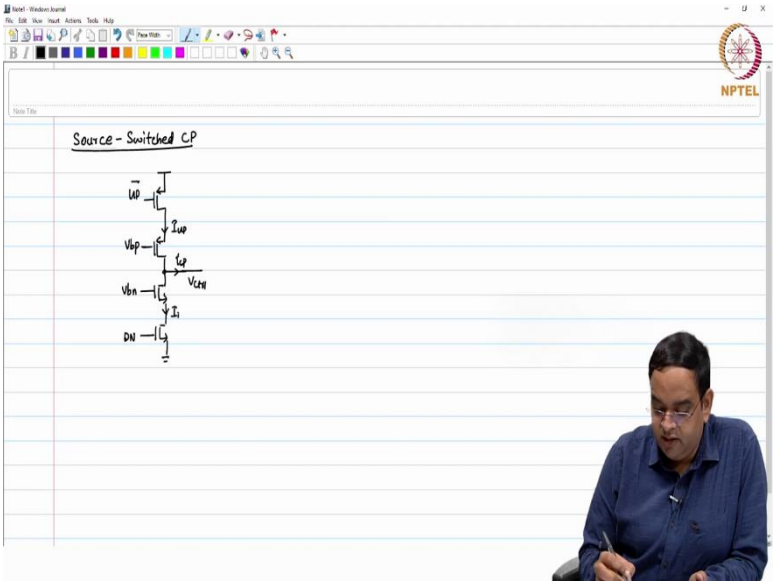
**Phase-Locked Loops**
**Dr. Saurabh Saxena**
**Department of Electrical Engineering**
**Indian Institute of Technology Madras**

**Lecture – 56**
**Circuit-level Design of Charge Pump: Part VI**

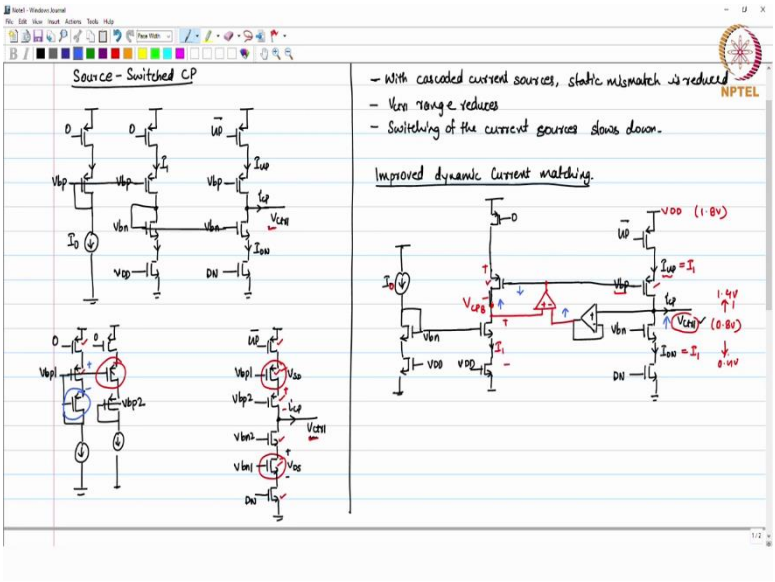
(Refer Slide Time: 0:16)




Hello everyone. Welcome to this session. In the previous session, we discussed the charge-pump design. And now, we also discussed the reasons for mismatch in the current output for the charge-pump and then because of this mismatch, how it will lead to the spur at the output of the oscillator. So, in this session, we will look at how to address these mismatches. So, we are going to talk about the methods to address these mismatches in source-switched charge-pump which is quite commonly used.

So, previously, you had seen that there is a current mismatch between the charge-pump and between the $UP$ and $DN$ current sources. So, this is what we used earlier with, this is $\overline{UP}$, this is $DN$ and you have this as $V_{bp}$, it was generated using a replica biasing scheme and because of the channel length modulation, you will see that this particular current source has mismatch, voltage is this and this is $i_{cp}$. The current which is flowing here is $I_{UP}$ and the current which flows here is $I_{DN}$.

(Refer Slide Time: 1:45)




The way we get these voltages was something like this. So, I will just copy it, this is what we had earlier, this was 0 and this particular thing was $VDD$ and then you can have this. So, we can remove this and have a current source, an external current source like this, this is connected here, this and this is done in this manner. This is connected here.

So, this is how we actually designed our bias for the charge-pump. This is current $I_0$, the current in this branch will be $I_1$. Depending on the matching between the second branch and the first branch, you are going to see current $I_1 = I_0$ or with some mismatch and then when you have the actual charge-pump, you have a control voltage.

So, because of this control voltage, you will see a mismatch between the current $i_{cp}$ and $I_0$. Now, in order to increase the matching or reduce this mismatch, what we can do is we can have a cascoded current source that will have lesser susceptibility towards your $V_{ctrl}$. So, what I can do is the following. So, I have $V_{ctrl}$, your up MOSFET and then I have a cascoded PMOS current source like this. Similarly, cascoded NMOS current source and these two cascode voltages are going to be generated using replica biasing scheme.

So, this is still $\overline{UP}$ and this is $DN$, the output of the charge-pump is this, going to a loop filter with a control voltage $V_{ctrl}$. This is $V_{bp1}$ and $V_{bp2}$. Similarly, you have $V_{bn1}$ and $V_{bn2}$. These four voltages are generated using the replica bias scheme. Now, whether you are going to use some kind of diode connection or amplifiers, that depends, but the thing is that in this particular case, your actual current source if you look at it, you have the current source here, this particular current source.

Assuming that the top MOSFET and bottom MOSFET, they offer only a very low amount of resistance and they are operating in the linear region. Both these MOSFETs, all these four MOSFETs are operating in saturation region. So, the susceptibility of the current or the variation in the current due to $V_{ctrl}$ is going to be minimum because you will maintain same $V_{DS}$ when it operates in the bias case as compared to the charge-pump.

So, if I just take this branch and start generating these bias voltages. So, let us say, I have it here. So, all this goes away and for example, I am going to generate the bias voltage. This is going to be 0 and you will keep this. So, one of the methods can be you can do this and then this particular, this is passed on, this is 0. You can have the same current $I_0$ here and generate these $V_{bp1}$ and $V_{bp2}$. The size of this particular MOSFET will be chosen independently such that you get the desired $V_{SD}$ across this PMOS transistor.

So, in this way you can generate now. If this is the main current source, what you will see is in the regular operation, the $V_{SD}$ of the main current source remains roughly the same even when $V_{ctrl}$ varies. So, $V_{SD}$ for the cascode transistor will vary but not the actual current source. So, the current will roughly remain the same. Similarly, you can generate the bias voltage for NMOS also. So, this way it helps in reducing the static mismatch. So, with cascoded current sources, static mismatch is reduced but this has a problem that your $V_{ctrl}$ range reduces.

And by the way, when you have the cascoded PMOS, both these PMOS should operate in saturation region. That is the reason that $V_{ctrl}$ range reduces. In the presence of cascode, your actual parasitics will also increase. So, the switching of the current sources slows down, there is a trade-off. It is not that it comes on its own with no trade-off. Now, the other thing is that $V_{ctrl}$ varies all the time and this particular method has the problem of your speed and your range for $V_{ctrl}$.

So, there is another method which helps in reducing the current mismatch and let us look at that architecture with some improved current matching. When $V_{ctrl}$ varies, even in the presence of varying $V_{ctrl}$, we can get proper matching. So, the basic idea is the following that you take this actual charge-pump, source-switched charge-pump here. Now, one thing is that your $V_{ctrl}$ voltage varies all the time. So, with respect to $V_{ctrl}$, if $V_{ctrl}$ varies, we have to decide the other bias voltage or the current source accordingly.

So, here what we can do is, we can have the same, we can have the current bias generation for NMOS like this, where this is $VDD$ and you force in the current source, get this $V_{bn}$. Now, this

$V_{bn}$ is passed to another NMOS transistor. So, you have this current. If this current is $I_0$, you are forcing that this current be also equal to $I_0$ ideally and then the PMOS current which earlier you were deciding with a diode connection, now that PMOS current you are going to decide based on the control voltage.

So, this PMOS current, which is finally going to be surely connected to $V_{bp}$, this is going to be decided based on the $V_{ctrl}$ voltage. So, the method to do that is that you tap this $V_{ctrl}$ voltage, buffer it and in the current biasing branch itself, you try to force this voltage also as $V_{ctrl}$. So, if I call this voltage as $V_{CPB}$, where $CPB$ stands for charge-pump biasing. Then this $V_{CPB}$ biasing should be equal to $V_{ctrl}$ in the regular operation.

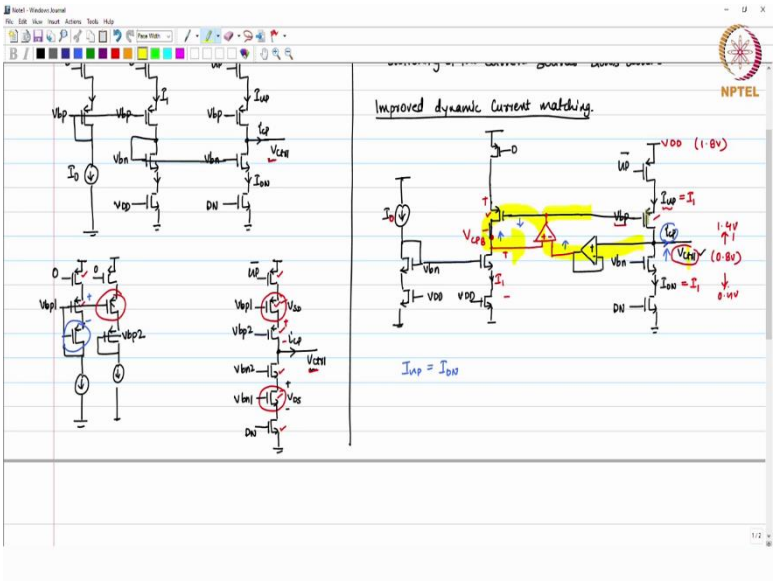
So, what will happen is if I want to force it, what I need to do is I need to compare this voltage whatever your buffered $V_{ctrl}$ voltage with our, buffered $V_{ctrl}$ voltage. So, I will take this $V_{ctrl}$, buffered $V_{ctrl}$ voltage connected here and then I choose the $V_{CPB}$ bias voltage. So, here what is going to happen is just think about it that you may bias your charge-pump with $V_{ctrl}$ if this is $VDD$ for example 1.8 V, you bias your loop filter at 0.8 V for example.

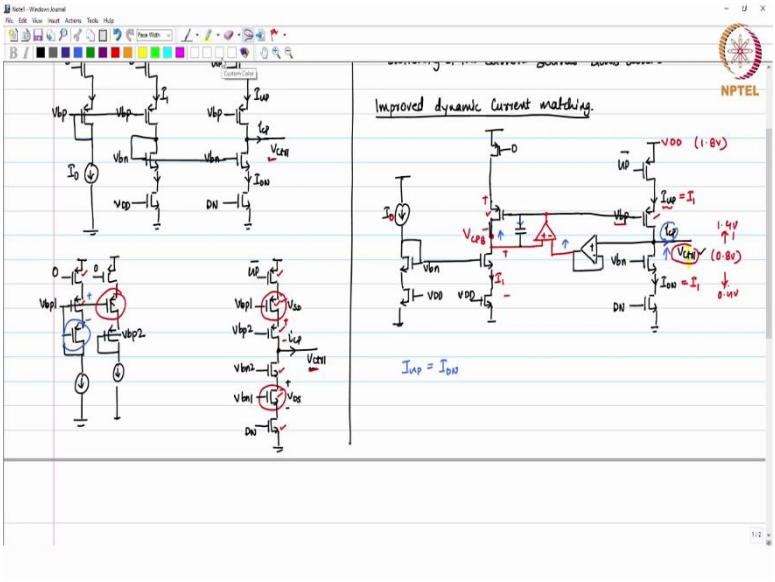
Then what it is going to do is this biasing is going to do, it is going to find the $V_{bp}$ voltage in such a way that $V_{CPB}$ is also equal to 0.8 V. So, in the regular operation of the charge-pump, you will have, it will not be like that you are having a different $V_{DS}$ voltage because of which you have a current mismatch. So, let us say, if this is $I_0$ here and this current happens to be $I_1$, there may be some mismatch between $I_0$ and $I_1$, whatever that mismatch is, that is fine.

Now, I am choosing the bias voltage of the PMOS in such a way that the $V_{SD}$ of the PMOS in the regular operation is close to $VDD - V_{ctrl}$ and $V_{DS}$ of NMOS is also equal to $V_{ctrl}$. So, your $I_{UP} = I_1$ and $I_{DN} = I_1$. Then the rest is the mismatch between these two transistors but whatever you will have because of different $V_{ctrl}$, this 0.8 V, you can go up to let us say 1.4 V and you go up to 0.4 V at the bottom. If you have even this variation, you will change the bias voltage here.

So, in this way, you can suppress your dynamic mismatch between the top and bottom current sources to a great extent. Now, you see here that you want to look at the feedback loop. So, if $V_{ctrl}$ voltage is higher, if $V_{ctrl}$ voltage increases, this voltage increases, if this voltage increases based on the amplifier here, this voltage drops. If this voltage drops, then $V_{CPB}$ increases. It will become equal to this only.

(Refer Slide Time: 14:23)




Now, in this case, what you see is during the regular operation of the charge-pump, you will have some current which is flowing into the loop filter. What we want is that there is a matching between $I_{UP}$ and $I_{DN}$. So, there should be minimum mismatch between $I_{UP}$ and $I_{DN}$ because of the $V_{ctrl}$ voltage, so it will try to do that.

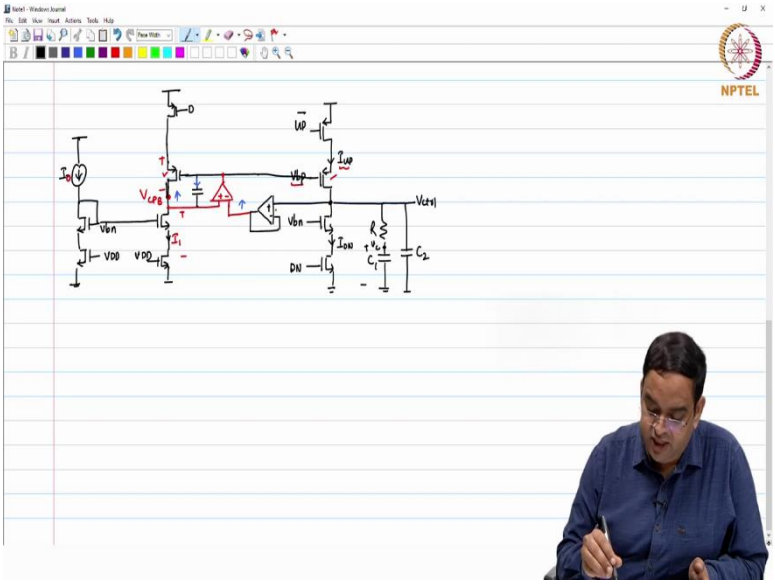
But whatever happens whenever you are adding any current to $V_{ctrl}$, we have seen that in the presence of the loop filter, your $i_{cp}$ will create a jump in the control voltage. And when it creates a jump in the control voltage, you can say that this particular, you see any change in the control voltage, this particular loop gets activated and well, it is changing $V_{bp}$ here.

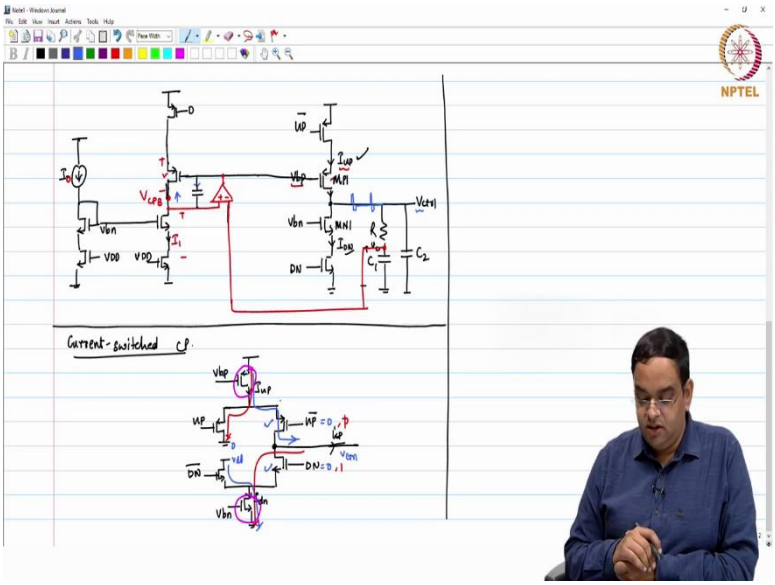
So, it seems like for example, if $V_{ctrl}$ voltage increases in steady state, every reference cycle you have some current which is added to the loop filter. So, if $V_{ctrl}$ voltage increases, what this particular loop is doing is if this voltage increases, it is trying to, this particular loop also acts and it responds to local disturbance. What we want here is that during the regular operation of the PLL, $V_{ctrl}$ voltage changes for the desired output frequency.

So, for different output frequencies, whatever your control voltage is, with respect to that control voltage, I should bias my $I_{UP}$ and $I_{DN}$ in such a way that there is minimum mismatch, but the charge-pump, this control loop starts acting on every reference cycle which is something which is not needed and it can create problems also if it is not stabilized properly.

So, what we need to do is, we need to stabilize this loop, this particular loop with the help of Miller capacitor here in general and the bandwidth of this loop can be quite less. Even then what you are going to see there will be some disturbances which will come.

(Refer Slide Time: 16:56)






For, in order to minimize the disturbances on which the loop acts, in place of directly taking the $V_{ctrl}$ from there, so, ideally, we know that this particular current is actually going to the loop filter with R and $C_1$ and $C_2$. So, your $V_{ctrl}$ voltage and your $V_c$ voltage, the voltage across the $C_1$ capacitor, the DC value of these two voltages is the same and it will change only when you require the frequency of the oscillator to vary. So, that is the only thing.

So, what we can do is, in place of having the reference coming from $V_{ctrl}$, we can remove this and we can actually take the reference from here. So, the regular disturbances at your $V_{ctrl}$ that you every time you have a reference clock, you may have some kind of current, these regular disturbances are actually suppressed as $V_{c1}$ node.

So, this particular loop will not be acting on the so frequent disturbances. And this helps in minimizing the ripple on the $V_{ctrl}$ also or this helps in minimizing the disturbances because of the PLL and because of this loop itself. So, in this way, we can minimize the dynamic mismatch between your $I_{UP}$ and $I_{DN}$. This is the way which we can use. Now, even after doing all these things, what happens is, well, this works pretty good.

But what will happen is that if you look at it, these two transistors which are MP1 and MN1, these two transistors, they go into cut-off and then they go to saturation. So, whenever you have a current source which is in cut-off and then during the transient, it goes into saturation, there is some lag, time lag and even it is not only the simple time lag, the current changes from zero to the final value non-linearly.

So, that is one problem and the switching speed is also a problem that your current source turns off and then it goes to saturation. So, how fast you can switch, the speed is going to be limited.

So, you may not be able to operate this particular charge-pump at a higher speed. So, what we can do is in place of switching the current sources in this manner, what we can do is we can keep a fixed current and we can switch the current at the output as desired.

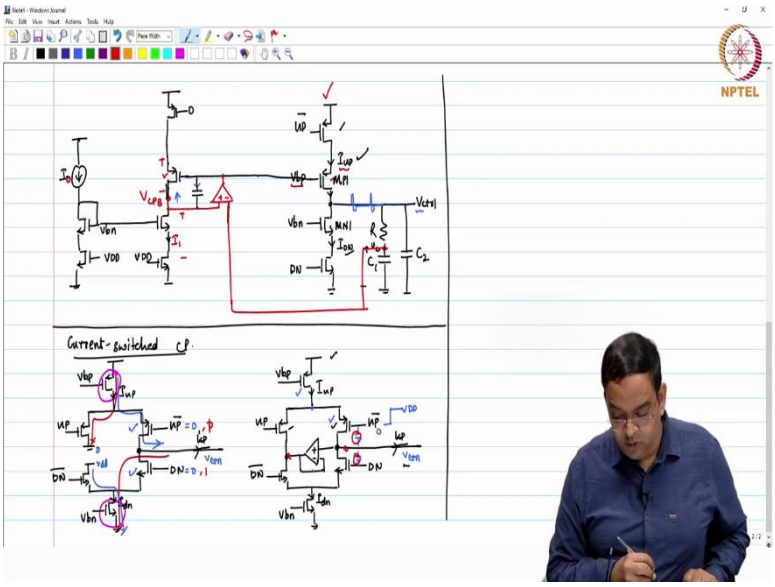
So, normally, we call that as a current-switched charge-pump. So, here what do we do? We have a fixed current value which we generate using the bias voltage which we generate using some replica biasing scheme and then this current is fixed always, it will be there and you switch it to the output depending on your PFD outputs and this current at the bottom also, the current is fixed. So, I generate $V_{bp}$ and $V_{bn}$ in such a way that these two current sources are same.

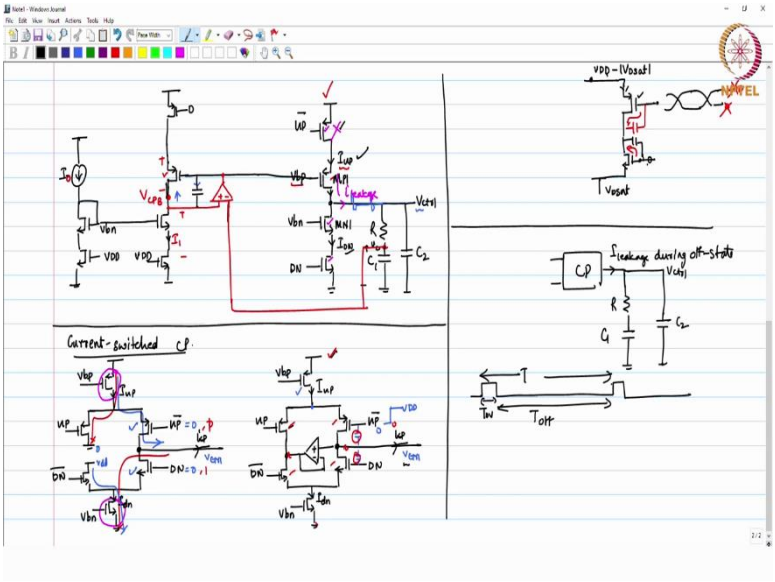
So, this I can call $I_{UP}$ which is coming and $I_{DN}$. If these are current sources, then I should have $I_{UP} = I_{DN}$ when I am going to generate $V_{bp}$ and $V_{bn}$. Then you have the other two switches which actually divert the current when the current is not in use. So, if this is $\overline{UP}$, you have $UP$ signal here and for the NMOS case on the other side, this is $\overline{DN}$ and this is $DN$, this output is fed to the loop filter.

So, now, you see when $\overline{UP} = 0$, $\overline{UP} = 0$ that is like $UP = 1$ and $DN = 0$, in that particular case, all the $UP$ current flows through this switch and goes to the output and the NMOS current because $DN = 0$, NMOS current takes this path. On the other hand, when you have $DN = 1$ and $\overline{UP} = 1$, at that time, the current, $DN$ current flows like this and your $UP$ current gets diverted and it goes here.

So, you see that these two MOSFETs, the current source is not switched off at any given time. It is just switched from one direction or you can say one MOSFET to the other. So, this is quite fast because your current source is not getting switched from off-state to on-state. This particular design has a problem that the switches which are operating, these two switches are actually having a $V_{ctrl}$ at the output whereas when you divert the current to the other direction, one is ground, the other is $VDD$. So, because of this, the exact current mirroring will not happen or you will see additional current flowing in the charge-pump output.

(Refer Slide Time: 23:09)




So, to minimize that, what we can do is, so, what we would like to do is the similar thing which we did earlier that we, first, in place of having a different voltage for these switches, we can keep the same voltage as it exists in the charge-pump output. So, to do that, we are going to connect it like this and then what you can do is you can have a buffer using an amplifier and it connects it here. So, whatever your $V_{ctrl}$ is you will have a similar $V_{ctrl}$ here. Any mismatch during the current transition will be supplied by the opamp here.

So, in this way, you have current sources which are not switched from off-state to on-state. The current is actually steered from one direction to the other direction and the other thing is that the switches which are steering the current from one direction to the other direction, those switches are also operating with same source to drain voltage, source to drain or drain to source

voltage. Now, here also you will see that some kind of, if there is any ripple here, this ripple is also going to change the or it will create a ripple at this node. You can get rid of it if you take the reference in the manner as I have taken here.

So, this is one of the fastest methods to switch the current in the charge-pump. Now, one important thing is that all this source-switched charge-pump, this particular charge-pump is consuming only during the time when $UP$ and $DN$ pulses are high. And we know that in steady state, the charge-pump is turned on only during the overlap period when you have $UP$ and $DN$ pulses both high.

So, the current is consumed in the charge-pump, source-switched charge-pump only when you have the phase error or only during the overlap time which is much lesser than the reference clock period. But what happens here is in this kind of charge-pump, you are consuming the current always. So, if you are trying to minimize the power consumption in the PLL and charge-pump current has a significant role to play or significant value is there for the charge-pump current, then using the source-switched charge-pump is less power-hungry design as compared to the current-switched charge-pump.

So, that is one reason why you directly do not go for the current-switched charge-pump unless the speed is a problem or the variation in the small mismatch in the current is a problem. So, that is what we do. And now current-switched charge-pump, if you start giving big pulses like 0 and $VDD$. So, when you have 0 and $VDD$, similar things will happen if you recall this is like a drain-switched charge-pump.

Because you want to keep the current constant, this transistor is always on, you are switching at the drain. So, you get a good amount of clock feed through coming in. Now, this clock feed through is surely a problem. So, we can minimize this clock feed through by not switching these transistors, the switches which you are seeing here highlighted or checked with red, by not switching these switches with full scale signals like 0 to $VDD$, we can limit the signal which are used for these switches.

So, if you think about it, I will just draw the PMOS as a switch. So, this voltage will surely be something in an ideal case it will surely be $VDD - |V_{Dsat}|$ of PMOS transistor. Now, in order to switch this transistor, the current, if I want to steer the current, I do not need this voltage to go to 0 and one time it is going to 0 and the other time it is going to $VDD$. By the way I never

want this voltage to go to $VDD$ because this particular transistor turns off even before the gate voltage goes to $VDD$.

So, I can limit the swing for this transistor between some values depending on our design and if these two switching values, they are not 0 and $VDD$, then the clock feed through which is coming through the capacitor, that will be minimized and a similar thing will happen for NMOS also. To turn off the NMOS, you do not need this particular voltage to go to 0. So, your lower swing is limited. On the higher side also, how much swing you need, it depends on the switch size.

So, based on the limited swing here, you can minimize the clock feed through through this transistor also. So, as I told earlier that the drain-switched charge-pump is also used but quite often in this manner. And if we recall regarding this clock feed through problem, we have to address it by not using full swing for switching the current. So, no matter whichever charge-pump you use, what happens is that you have this loop filter, by the way, whatever charge-pump you are using.

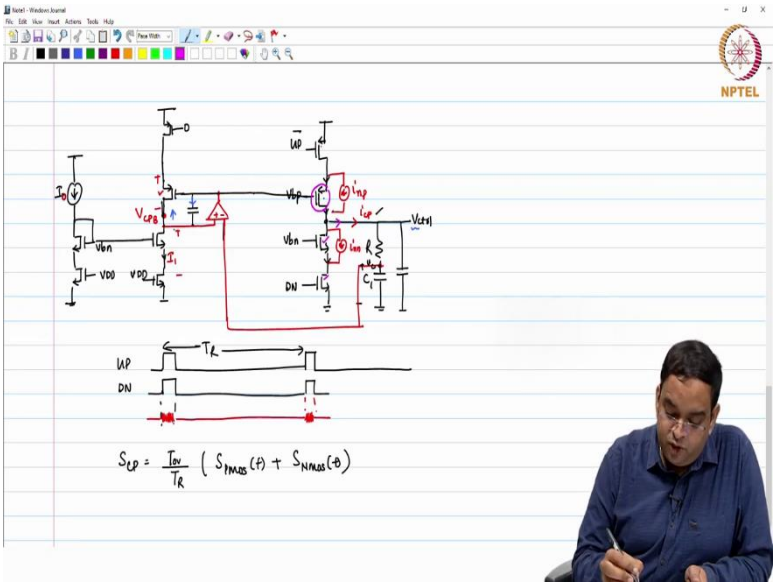
Now, you know the charge-pump consists of your MOS transistors and even when the MOS transistors are off, during the off-state also, there will be some leakage current, some leakage current I call that as $I_{leakage}$ during off-state. So, what happens is whether it is draining the charge or it is pushing the charge in the loop filter, it depends on the sub-threshold current.

For example, if you take this particular charge-pump, so, this switch is off, this one, there is some sub-threshold current which is, both these switches will be, both this switch and the current source will be having. Similarly, you have a sub-threshold current for this. Whatever the error in the sub-threshold current between the top and the bottom branch, that will flow as $I_{leakage}$ and if you have a leakage current during long in steady state, we know charge-pump is active only for a small amount of time. So, most of the time, the charge-pump is off.

So, it is like your $UP$ and $DN$ pulses will be, this is still a magnified version. During all this time, the charge-pump is off. This is your whole time period, this is only $T_{ov}$. So, during the off-state, you have leakage current. Because of that leakage current, your control voltage changes and if your control voltage changes in steady state, your PLL feedback loop will get into action and try to fix it by creating an offset at the input of the PFD.

So, that is what is going to happen. Then, the last thing about this charge-pump is as you see that the charge-pump gets active only during the time when you have $UP$ and $DN$ pulses both as high, so, in that case, the noise from this charge-pump.

(Refer Slide Time: 31:58)



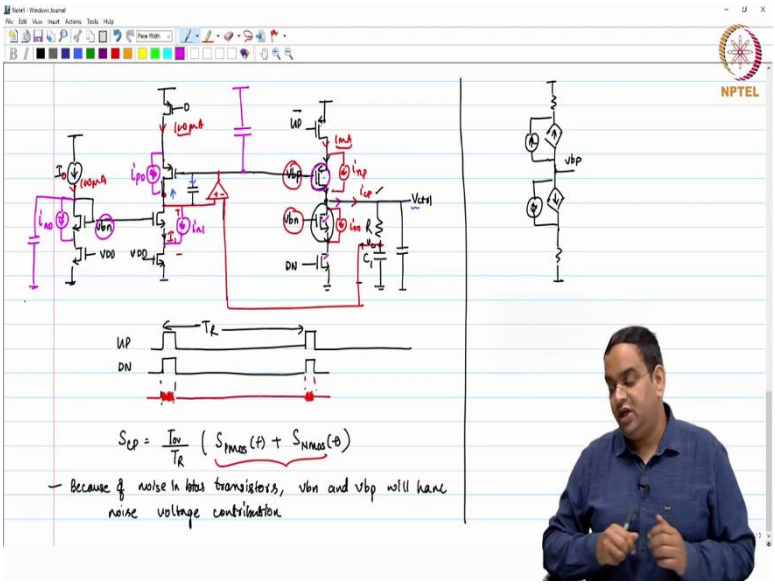

So, I will just let us draw this. So, this is the charge-pump which I have. So, we know that our $UP$ and $DN$ pulses in steady state, they will have some overlap region. During the overlap region, these two current sources are active or you can say both the branches are active. Now, when both the branches are active, then the noise current, whatever the noise current you have, the difference in the noise current is going to flow and come at the output. We have seen this earlier, now this is just with the transistors.

So, thinking or assuming that the current sources are going to dominate the noise, I call this as $i_{np}$ and this is $i_{nn}$. So, the noise current is going to be present only during the time when both the switches are on and the difference of the noise current is going to flow but these two currents are not correlated. So, what you will see is that the charge-pump noise spectral density is given by,

$$S_{CP} = \frac{T_{ov}}{T_R}\left(S_{PMOS}(f) + S_{NMOS}(f)\right)$$

I am just writing $R$ as a subscript to denote that $T_R$ is the reference clock period, $S_{PMOS}(f)$ is the noise spectral density for the PMOS current source and this is NMOS, this is what we have seen earlier. So, that is how the noise will come from the charge-pump. An important part here is the following that it is not only the noise contributed by this transistor.

(Refer Slide Time: 34:10)




So, whatever noise you have because of this transistor and this particular transistor, these two noise sources are going to change the $V_{bp}$ voltage here. Similarly, the noise of this current source is going to change $V_{bn}$ here. So, I will call this as $i_{n0}$, this as $i_{n1}$ and this as $i_{p0}$. So, because of $i_{n0}$, because of noise in the bias transistors, $V_{bn}$ and $V_{bp}$, here I am assuming the amplifier is ideal, but you can think because of the amplifier noise also, $V_{bn}$ and $V_{bp}$ will have noise. Why does it happen? Because when you have a noise voltage here, it will change the $V_{bn}$ voltage, it is going to change, similarly, you will change from $i_{p0}$ and $i_{n1}$, it is going to change.

How to find how much contribution? Well, that is easy. Let us say you consider the first bias branch. So, first switch I am modelling as a resistance though it also has a noise. Then I have the current source. So, you draw the small signal model and after drawing the small signal model, you can very well find the voltage and noise contributions. So, with the help of the small signal model, you can find what is this $V_{bp}$ voltage. Now if $V_{bp}$ voltage is noisy, then based on the $g_m$ of this transistor and the $g_m$ of the NMOS transistor, that noise also gets amplified at the charge-pump output.

So, the idea is that this noise which you are seeing in the parenthesis, this noise is not only due to the transistors which are present in the final charge-pump, but the noise is also due to the bias branches which are contributing noise at these bias voltages. It is quite important to note that it is not rejected.

So, you cannot say that you have simulated the noise only for this branch because this is the main charge-pump and if it contributes some noise, I will take that and I will discard the bias. The reason why this is very important is that quite often what we do is if we want a current of 1 mA, we do not like to burn 1 mA current in the bias branch. We may burn only let us say 100 μA here and 100 μA here.

So, from the power consumption point of view, the bias is consuming much lesser power than the actual charge-pump required. What happens in the actual charge-pump current requirement? This charge-pump current is dictated by, if you remember the loop gain analysis and the noise analysis, so, this is the number which you will get from your analysis, bias you will just add to support the actual circuit, charge-pump circuit. If you have less current here, your $V_{bp}$ and $V_{bn}$ are going to be noisy and when they are noisy, you will have the final output noise also quite large.

So, the scaling cannot be skewed by a lot of margin. You can have 1:6, 1:8, do not think that you can have 1:1000 scaling and everything will work fine, it does not. The other thing which you can do is that you have a noise at this $V_{bp}$, you can add a capacitor at this node to filter out the noise at $V_{bp}$. Similarly, you can add a decoupling capacitor at $V_{bn}$ to filter out the noise at $V_{bn}$.

So, these two things are utilized to reduce the noise contribution from the bias but there is also a limit to how much capacitor you can add and how much is the noise contribution coming from the bias circuit. These are all design dependent. You will understand or learn more when you are going to design on your own. Thank you.