Phase-Locked Loops
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Lecture – 54
Circuit-Level Design of Charge Pump: Part IV

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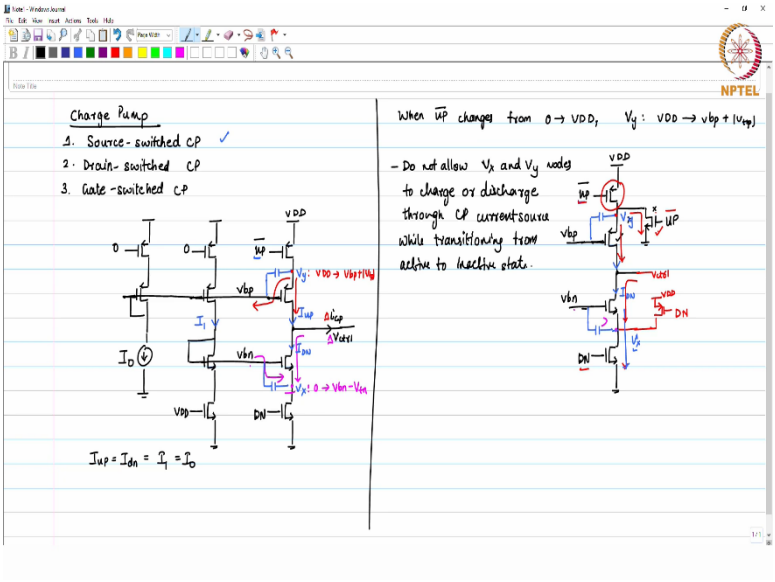

Hello everyone. Welcome to this session. In the previous session, we discussed different topologies for charge-pump, we will continue our discussion on that. So, we saw three different kinds of charge-pump, one is source-switched where we switch the current source at its source. Then we saw drain-switched charge-pump and after that we saw gate-switched charge-pump.

Now, based on our requirement, we may choose between source-switched or gate-switched charge-pump. Drain-switched charge-pump inherently has a lot of clock feed through. So, we would not like to use that. Gate-switched and source-switched are the two main options which we have but among all these three options, source-switched is quite commonly used unless we are going for the differential or some other charge-pump. We will see that.

So, in the source-switched charge-pump, let us go a little bit in detail. So, we have our switch like this and then we have a current source with NMOS and PMOS current source and we bias our current source and other things in such a way that it carries the desired amount of current. So, I will just make that also here. So, this is what you have and then a copy of this is here.

So, to get the desired bias current, what we are going to do is we will pass the desired current through this which is I_0. This generates the V_{bp} voltage which is passed to the PMOS here and

this is 0. This remains 0, then this is generated here with a diode connection and this is VDD and this voltage is passed like this. So, this is V_{bp} and this is V_{bn}.

Here you use $\overline{UP}$ and DN signals and this is what you have. Now, the current which you are going to see in these branches is let us say I_1, so I_1 in this branch because this is always conducting and I will call this as I_{UP} and this one as I_{DN}. So, this is the current source which you will have if it operates. This is i_{cp}.

Now, it depends on, so, ideally what we think is that $I_{UP} = I_{DN} = I_1 = I_0$, this is in the ideal case. And by the way, this voltage node is called as control voltage. So, this is the case. So, what happens is that you have a capacitor connecting like this and we saw that in the previous session that you have this capacitor here.

So, what happens is that during the off state, these voltage nodes, we call this as V_x and V_y, these voltage nodes should ideally as soon as this switch is turned, this particular switch turns off, then what should happen is that the current from the upside should be equal to 0. And similarly, the current from the downside should also be equal to 0 but this V_y voltage makes a transition.

So, when $\overline{UP}$ changes from 0 to VDD, during that time, this is VDD in this case, during that time, your V_y signal changes from close to VDD to $V_{bp} + |V_{tp}|$. Whenever your $\overline{UP}$ signal actually goes from 0 to VDD, you make a transition here from VDD to $V_{bp} + |V_{tp}|$. So, during this process, you have a current which is actually pumped to the loop filter. You have this current which whatever this node discharges from one potential to the other. So, this current has to go somewhere.

You can say that this current sees two paths, one path is this, the other path is this because of the C_{gs} capacitor. So, you have some Δi_{cp} current going into the loop filter which creates a change in the V_{ctrl} voltage which is not desired. A similar thing is going to happen that this V_x potential goes from roughly 0 to $V_{bn} - V_{tn}$.

So, when this voltage changes from 0 to $V_{bn} - V_{tn}$, you can think that you have to draw the current from the V_{ctrl} node and charge this particular node to $V_{bn} - V_{tn}$. So, there is a discharge path which is, or charging path which happens either from here or from here and it happens from both the places which actually changes the control voltage or this is unwanted current which you have.

So, if you do not minimize it, it will create disturbance in the control voltage and we have seen at least at system-level that if you have a change in the control voltage, this is going to modulate the frequency of the VCO and thereby it is going to add to the reference spur. So, what we can do is the following.

In place of leaving this circuit as such, what we can do is, let me just redraw this. We cannot remove the cap whatever cap we are having, that cap will anyways be there, this is V_{bp} and V_{bn}. The thing which we can do is, this node potential, we do not want this node potential to discharge through the current source.

So, what we can do here is, at this node, we provide a separate discharge path and this is working with UP signal. When $UP = 0$, that time this is turned off. When $UP = 1$, at that particular time, so, just look at it, so this MOSFET is active when UP signal is 1. When $UP = 1$, so this is actually working on $\overline{UP}$ itself. When UP signal is 1, at that time your PMOS is active and NMOS is turned off.

When $UP = 0$, that time NMOS turns off and it discharges this V_x node to ground. It minimizes the current coming from the current source, this PMOS and changing the control voltage. Similarly, on the V_y node, we can add PMOS transistor like this which is connected to VDD and this is working with DN.

So, when $DN = 1$, at that particular time, PMOS is off and you have a current path like this. The current path is shown here but when you go from $DN = 1$ to $DN = 0$, previously your V_y node was getting, this is by the way V_y, I have been using, this is V_x. Your V_x node was earlier going to $V_{bn} - V_{tn}$. But now what happens is this particular node, V_x node is charged to VDD or higher potential such that the current which is drained from the V_{ctrl} node, that current is minimized or reduced to 0.

There are options to choose MOSFETs, both these MOSFETs with high V_t or something to make sure that this particular voltage does not go all the way to ground, it can go to some potential. So, those things can be done. The basic idea is do not allow V_x and V_y nodes to charge or discharge through charge-pump current source while transitioning from active to inactive state. You keep this in mind, so whatever helps you to do that, you can do that. This is one of the options. Now, well, after doing all this, we have a good charge-pump. So, let us see are there any problems with this or this is good to be used in the PLL.

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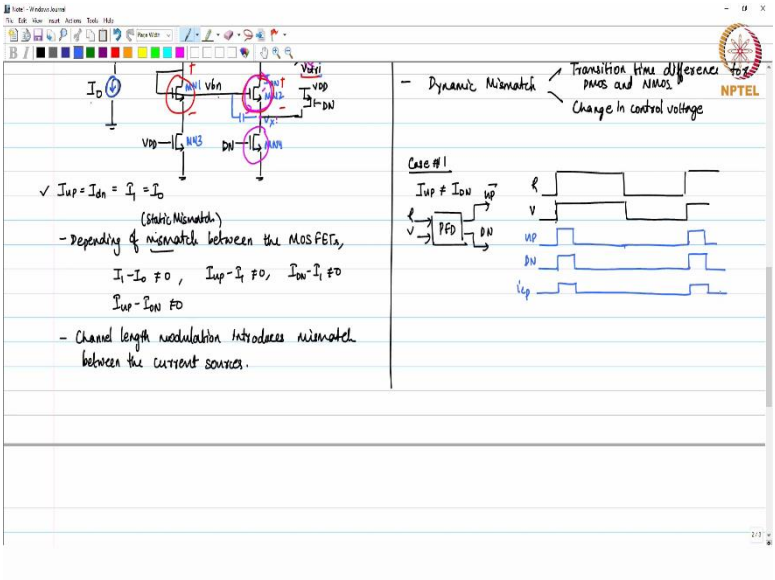

So, now, we can add the transistor which we were having here like either NMOS going to ground working with $\overline{UP}$ and this one pulled up to VDD so that you turned off the main transistor, this is connected to DN. Now, as I said that it is our assumption that $I_{UP} = I_{DN} = I_1 = I_0$. This is the current which you control from outside. So, you have a control on this. Depending on this, your current should change at the output.

Now, what happens is that if you just take these two transistors, the current sources, let us call them as MP1 and this is MP2. Based on the mismatch between these two transistors, MP1 and MP2, your current I_1 is going to vary from I_0. So, I will write this MP1, MP2, MP3. Similarly, this is MN1, this is MN2, and you will have all other transistors, I will just name it, MP4, MP5, MP6. This is MN3 and MN4.

So, depending on the mismatch between the MOSFETs, you will have the variation between I_1, I_0 and then I_{UP} and I_{DN}. So, you can say,

$$I_1 - I_0 \neq 0$$

Similarly, we have,

$$I_{UP} - I_1 \neq 0$$

$$I_{DN} - I_1 \neq 0$$

$$I_{UP} - I_{DN} \neq 0$$

Ideally, we know that all these current sources, they have to be same, but these current sources are not same all the time.

Now, if these current sources are not same all the time, what are the effects? That is one thing which we need to understand. The other thing which we need to know is that is there some way that we can fix that. The other thing is that this is only depending on the mismatch between the MOSFETs which you will have and this particular mismatch is called as static mismatch. Why is it static mismatch? Because when you design this circuit, whatever mismatch you have, that mismatch will remain, that mismatch will always be there. It will not change during the operation of the charge-pump. So, this is one mismatch which you will see. The other mismatch which you are going to see is V_{ctrl}. So, the current which you are going to see coming from I_{UP} or I_{DN}, that also depends on V_{ctrl}. So, you can say you have channel length modulation for the current sources whichever current sources you see. Based on the channel length modulation, you will again have the mismatch.

So, I will write that channel length modulation introduces mismatch between the current sources and why it will be there during the regular operation? The V_{ctrl} node which you are having, this V_{ctrl} voltage is decided by the PLL feedback loop, this is the control voltage of the oscillator. So, V_{ctrl} can vary. If V_{ctrl} varies, then you see that the V_{SD} of the PMOS here is different from the V_{DS} of the NMOS here.

So, if your drain to source potential for NMOS or source to drain potential for your PMOS differ, then they cannot have the same current. So, this is another mismatch which you will see between these current sources. The other one is that when you are making a transition, when your UP pulse, if you look at it, this I_{UP} and I_{DN}.

So, when my $\overline{UP}$ signal makes a transition from 1 to 0 like this or high to low like this, your I_{UP} current, this particular current will go from 0 to 1 in some time and when you make it, when you make your $\overline{UP}$ signal to go from low to high, then your I_{UP} current will go from high to 0 something like this.

So, even when this current which is the current when you say when it has reached steady state, this current maybe same for both UP and DN pulses. So, you can look at I_{DN} and I_{DN} current depending on your DN signal, I_{DN} current maybe like this. So, you may have this current same as this current but during the transition which you see, this current is not the same as the current here.

And these things will happen because in this case, you see that the PMOS, one transition is happening I_{UP} current is coming because of the PMOS which will not respond exactly in the same manner as your NMOS is going to respond. So, these two PMOS, they will respond differently as compared to NMOS. So, you will see the difference in the current.

In steady state, well, when it settles, then during the settling process, the current is same. Why does it not respond in the same way? Because PMOS mobility is different, the parasitic capacitors are different, how much time it will take for this node, $\overline{UP}$ node to go from 1 to 0 and then how much time it is going to take V_y to go from some 0 voltage to VDD and then get this current source activated. These timings are going to be different from your timings for the NMOS. So, there is going to be a mismatch here. That is another mismatch which you will see in these current sources.

Another one, so, this is a kind of a, you can say a dynamic mismatch in the current sources. So, you have dynamic mismatch and one dynamic mismatch is because of transition time difference for PMOS and NMOS. That is one thing. Another thing is that when your control voltage is changing.

So, one thing is that in steady state, if the control voltage remains fixed, then you do not have any, then the current source will always remain fixed, but every reference clock or depending on the feedback required, control voltage may have a ripple or let us say this ripple is not because of the charge-pump. The ripple is because of the other things in the PLL. Also, the control voltage may need to vary across the frequency range which you need for your PLL.

So, if your oscillator goes from x frequency to 2x frequency, control voltage may vary by 2x. So, if control voltage changes, in that case also, your output current will change. So, because of the change in the control voltage, this control voltage is the control voltage of the oscillator, change in the control voltage during the regular PLL operation, you will have the difference between I_{UP} and I_{DN}.

So, there are multiple reasons for which you may see a mismatch between the UP and DN current sources from your external current source which you are using for biasing the charge-pump and this mismatch creates additional voltage ripples on the control voltage which in turn creates the reference spur.

So, let us just understand that how this kind of ripples are going to create and what is going to happen in the PLL. Once we know that what problems it causes, we will try later to address

and minimize this mismatch. Now, to begin with, let us take case one where, for any particular reason, you have a mismatch between UP and DN currents. So, two cases we will study here that when you have UP and DN mismatch current. So, $I_{UP} \neq I_{DN}$ whether it is coming from your MOSFET mismatches or it is coming because of the channel length modulation, this mismatch exists.

So, when this mismatch exists, what will happen is by the way you are having your PFD which gives you signal $\overline{UP}$ and DN to control the charge-pump. This is what you will have. You have the signals R and V. V is the feedback signal, R is the reference signal. So, ideally in steady state, you should have R and V aligned. But now, if I do that, let us say R and V signals are aligned like this in a Type-II Order-3 PLL. If this happens, then we know that our UP and DN signals, they will have a certain overlap period in this manner. This will happen when you have the phases aligned. You will have UP and DN but because your $I_{UP} - I_{DN} \neq 0$, so your charge-pump current will be, you will see a current i_{cp} with whatever difference you have $I_{UP} - I_{DN}$ current like this.

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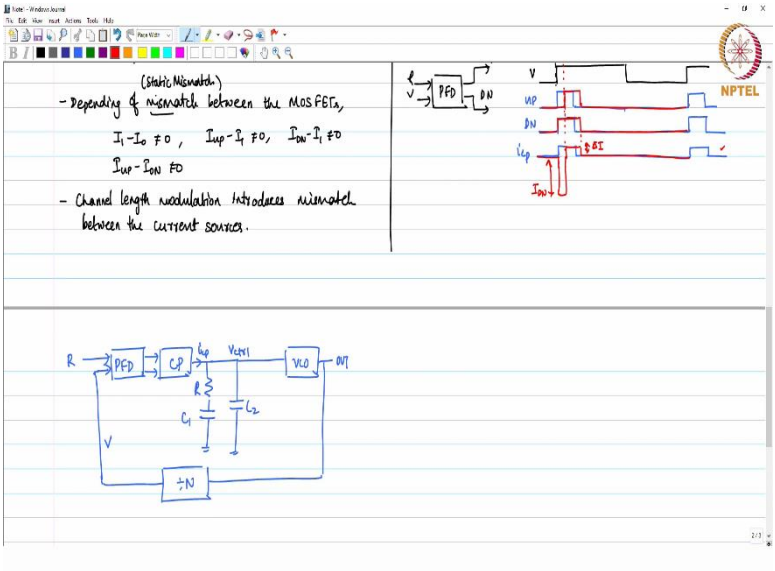

So, if someone has forgotten the PLL block, I will just draw that. So, we are having PFD followed by charge-pump, you are using source-switched charge-pump. Then we have loop filter R C_1 and the other one is C_2 and then you have VCO with a divider in the feedback and this goes, comes back here, this is R and this is V, by the way. Here this is your output of the PLL. So, we are talking about this i_{cp} and this control voltage. So, this will happen if there is a difference between I_{UP} and I_{DN} and that difference I am calling as ΔI.

If you are going to add this current to the PLL, then the control, because you are adding, this i_{cp} waveform here has non-zero DC value which means you are adding a DC current to the capacitor. So, voltage will always keep on increasing and if this happens, then you are going to saturate but because you are operating the PLL in a feedback loop, this does not happen. So, what happens is that the PLL itself will actually create an offset in such a way that the average current which goes into the capacitor, that is 0. So, how does it do that? So, this is what you see that $I_{UP} > I_{DN}$. So, during the overlap period, this will happen. So, what I need to do is in order to compensate for this current, I have to add a negative current which means that I have to create a negative phase offset.

So, the PLL itself is going to do the following. It will create an offset like this in feedback because that is what the PLL will control. Now, when you have an offset like this, so, your DN signal will go high here but UP signal goes high like this. This will happen your UP signal goes like this and the overlap period is now you have a negative phase error and this is your overlap period and this is going to repeat.

So, with respect to our original case, what will happen is during this time when you have a negative phase offset, you will have a negative current which is I_{DN}. When you have DN signal as active, you will have I_{DN} current and then for the overlap period, you will have this value. So, this T_{os} is created by the PLL loop and it is done in such a way that this current which you are seeing as I_{DN} and this is the ΔI current such that these two things are going to give an average current to the loop filter which is 0 so that in steady state, you do not have any change in the frequency.

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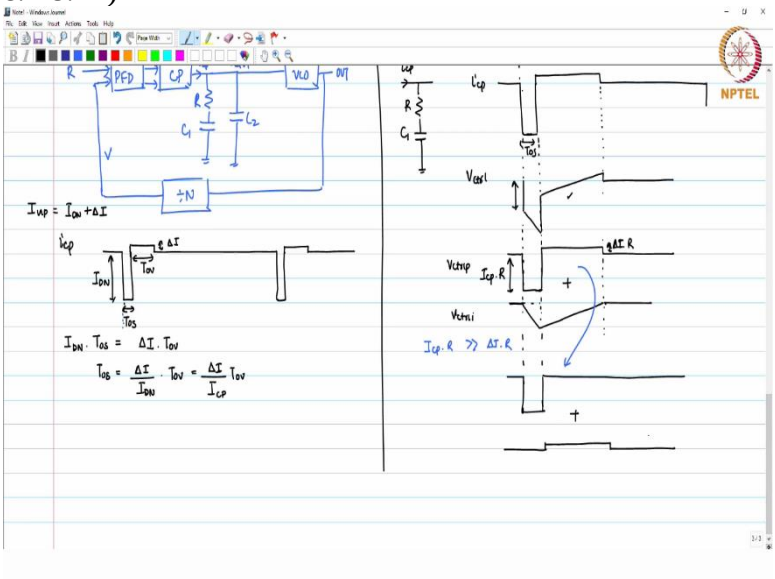

So, now, with respect to this current, if you think about it, I_{CP} R I have, so I will just now magnify this let us say here. In the presence of the mismatch between your currents, I am going to have a current like this from 0 to I_{DN} value and then the overlap period like this and this is the thing which is going to repeat every reference clock period. It is going to repeat, this value is I_{DN}, so if I write it let us say $I_{UP} > I_{DN}$.

So, we have,

$$I_{UP} = I_{DN} + \Delta I$$

This is what I have. So, here this value is I_{DN}, this value is ΔI. This offset is T_{os}, this region, and this is T_{ov}. So, in steady state, what you are going to see is the following:

$$I_{DN}\, T_{os} = \Delta I\, T_{ov}$$

So, T_{os} value which you are going to have is given by,

$$T_{os} = \frac{\Delta I}{I_{DN}}\, T_{ov}$$

So, I am just writing I_{DN} as I_{CP} now. So, we get,

$$T_{os} = \frac{\Delta I}{I_{CP}}\, T_{ov}$$

So, this is what you are going to see. It will create an offset value which is given in this manner. Now, in response to this steady state disturbance in the current source, you are going to have a change in the control voltage. And how will the control voltage react now? So, if you had only this loop filter, a part of the loop filter I am drawing R and C because going with both of them becomes a little difficult to visualize.

So, if this is my loop filter and I have i_{cp} the way I have shown you like this, I will again draw here with maybe an enlarged value. This is I_{CP} and then I have a large portion which is T_{ov}. Now, this is repeating. So, this is your total time period T. This is my T_{os}. So, in response to this i_{cp}, I am going to have V_{ctrl} voltage. i_{cp} is negative, so your V_{ctrl} voltage will take a jump and then it will integrate in the negative direction.

This is I_{DN} R jump you are going to have and then it will be a reverse jump like this and then what you are going to have is with respect to this. So, there is going to be this jump and then

you are going to integrate in the opposite direction and then again you are going to, this is what you may have in general.

If you only look at, this is what will happen if you have this loop filter. So, if you want to look at it, you look at it in two parts. One, the V_{ctrl} which you are going to have is only $I_{CP}\ R$ jumps which you see. So, one is like this, $I_{CP} = -I_{DN}\ R$ and then you have this is the jump and then, so, I can write this is as simple $I_{CP}\ R$ and this value is $\Delta I\ R$. So, this is the control voltage jump. The other part which you are seeing is nothing but the integrator part of it. So, that integrator part of it, what is it doing? It is doing something like this ideally.

So, absolutely if you look at it, your V_{ctrl} which you have here, this V_{ctrl} is sum of these two. So, the total charge what I am saying is you start with V_{ctrl} as 0, you go negative, but at the end you again you have V_{ctrl} as 0. Without this offset, what you may have here is only with the blue one, you may have V_{ctrl} going always in one direction and remaining there, but now what you see is that V_{ctrl} decreases and then it gets back to 0. So, in the presence of the second capacitor, things change a little bit. You do not have a sharp jump here, you have a slower jump, still you will see that effect.

So, let us look at first only with the simple loop filter R and C_1. So, now, this particular jump which you are seeing, this $I_{CP}\ R$ normally you will have $I_{CP}\ R \gg \Delta I\ R$ and why I am writing like this because I am going to decompose this particular part as two of the pulses. One which is this which is a large pulse like this every clock period and the other one I am going to write it like this, in this manner. So, this is only let us call this as V_{ctrlp} and this as V_{ctrli}. So, I am decomposing V_{ctrlp} as sum of these two waveforms.

What happens is that one of the waveforms which you see is having a much larger magnitude as compared to the other one. So, this creates a larger reference spur as compared to this part. So, we can analyze the one which is dominant and the one which is dominant is $I_{CP}\ R$.

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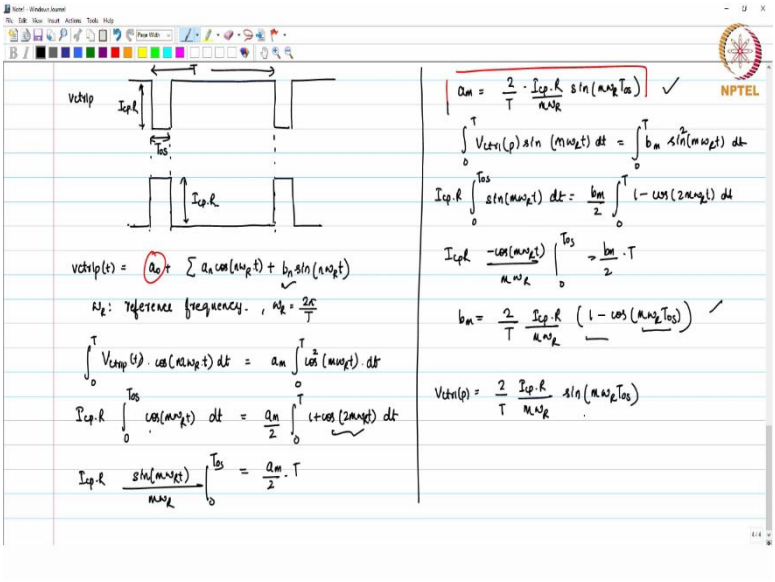

So, let me just redraw V_{ctrl} voltage, V_{ctrlp} for example and what you have here is, it is like this. This is repeated at every you can see in this manner, this is your time period T and for how much time? This is for T_{os}, jump $I_{CP}\ R$. You can have a negative jump, you can have a positive jump. So, I can very well say if your $I_{UP} < I_{DN}$, then you may see such kind of jump. So, there is nothing like you can have only one kind of jump. You can have both positive and negative.

So, now, this is a periodic disturbance in the control voltage. For this periodic disturbance in the control voltage, you need to find out that how it is going to change the frequency or it is going to cause any disturbance at the output. So, the standard procedure is that you write this $V_{ctrlp}(t)$ as a Fourier series. So, I will write as,

$$V_{ctrlp}(t) = a_0 + \sum a_n \cos(n\omega_R t) + b_n \sin(n\omega_R t)$$

Here it is happening at reference frequency. So, you will see that you are going to get a lot of components here. So, if I go and find the Fourier series component for this, I will get the fundamental. So, ω_R here is the reference frequency and I am just writing it for the positive one, not to get confused with the negative sign during our calculation. So, this is let us say this is $I_{CP}\ R$ also here.

So, when I go ahead and do this, what I will find is that you have here both the sine and cosine components, you can compute the values for both and to compute the values, it is an easy way. What you are going to do is $V_{ctrlp}(t)$, integrate this. If I want cosine, I am going to multiply with $\cos(m\omega_R t)$, integrate over one period. So, we get,

$$\int_0^T V_{ctrlp}(t)\cos(m\omega_R t)\,dt = a_m \int_0^T \cos^2(m\omega_R t)\,dt$$

You are going to integrate over one period such that $\omega_R = \frac{2\pi}{T}$.

So, to calculate this, we know that the $V_{ctrlp}(t)$ is actually non-zero only during the time 0 to T_{os}. So, we get,

$$I_{CP}\,R \int_0^{T_{os}} \cos(m\omega_R t)\,dt = \frac{a_m}{2}\int_0^T 1 + \cos(2m\omega_R t)dt$$

This integration over the time period is going to give us 0. So, what we are going to get here is,

$$I_{CP}\,R\,\frac{\sin(m\omega_R t)}{m\omega_R}\Big|_0^{T_{os}} = \frac{a_m}{2}T$$

So, this is going to give us that,

$$a_m = \frac{2}{T}\frac{I_{CP}\,R}{m\omega_R}\sin(m\omega_R\,T_{os})$$

So, this is what we get.

To find b_m, I will just do the integration with respect to sine. So, we get,

$$\int_0^T V_{ctrlp}(t)\sin(m\omega_R t)\,dt = b_m \int_0^T \sin^2(m\omega_R t)\,dt$$

$$I_{CP}\,R \int_0^{T_{os}} \sin(m\omega_R t)\,dt = \frac{b_m}{2}\int_0^T 1 - \cos(2m\omega_R t)dt$$

$$I_{CP}\,R\,\frac{-\cos(m\omega_R t)}{m\omega_R}\Big|_0^{T_{os}} = \frac{b_m}{2}T$$

$$b_m = \frac{2}{T}\frac{I_{CP}\,R}{m\omega_R}\left(1 - \cos(m\omega_R\,T_{os})\right)$$

So, you see these two components. The thing is that your T_{os} is quite small and when T_{os} is going to be quite small, this cosine of the small value is like equal to cos(0) which is equal to 1. So, b_m component will be more or less equal to 0. So, we will focus on this component only.

So, when we focus on this particular component and the dc component we know here that the dc component is going to be cancelled by the other offset component. So, in this case, we can write,

$$V_{ctrlp}(t) = \frac{2}{T}\frac{I_{CP}\,R}{m\omega_R}\sin(m\omega_R\,T_{os})\cos(m\omega_R t)$$

So, when we have this as a control voltage where we focus right now only on the fundamental amplitude.

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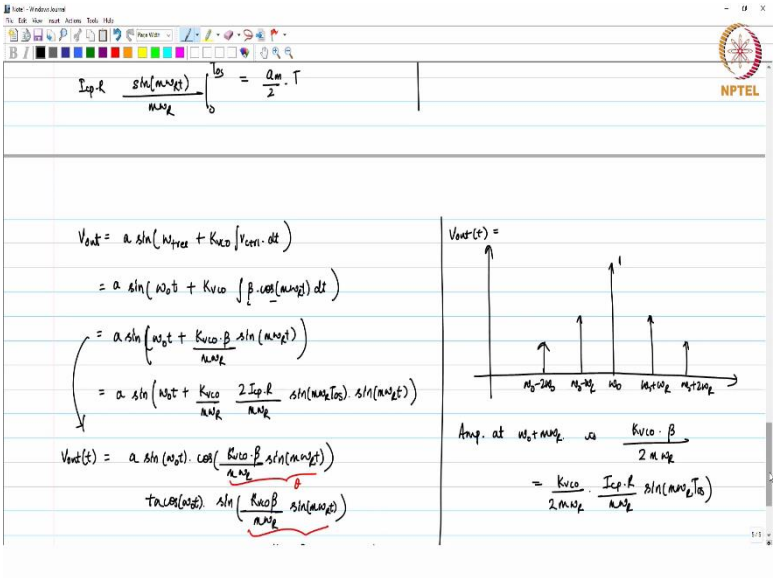

So, when that is the case, the V_{out} of the oscillator is given by,

$$V_{out} = a\sin\left(\omega_{free} + K_{VCO}\int V_{ctrl}\,.\,dt\right)$$

This is what we have which I will just write it as,

$$V_{out} = a\sin\left(\omega_0 t + K_{VCO}\int \beta\cos(m\omega_R t)\,dt\right)$$

$$V_{out} = a\sin\left(\omega_0 t + \frac{K_{VCO}\beta}{m\omega_R}\sin(m\omega_R t)\right)$$

So, you get this particular voltage at the output.

Now, if you look at it, we get,

$$V_{out} = a\sin\left(\omega_0 t + \frac{K_{VCO}}{m\omega_R}\frac{2I_{CP}R}{m\omega_R}\sin(m\omega_R T_{os})\sin(m\omega_R t)\right)$$

This is the expression which you have, absolute expression. But we are going to do a simplification here. So, we have,

$$V_{out}(t) = a\sin(\omega_0 t)\cos\left(\frac{K_{VCO}\beta}{m\omega_R}\sin(m\omega_R t)\right) + a\cos(\omega_0 t)\sin\left(\frac{K_{VCO}\beta}{m\omega_R}\sin(m\omega_R t)\right)$$

So, now, we will make an assumption that this value or whatever the argument of this is quite small. We know β is normally quite small and then you have another factor of $m\omega_R$ in the denominator. So, this whole, $\frac{K_{VCO}\beta}{m\omega_R}\sin(m\omega_R t)$, let us call this as θ. So, we have, $\frac{K_{VCO}\beta}{m\omega_R}\sin(m\omega_R t) = \theta$. If θ is quite small, then $\cos(\theta) = 1$ and $\sin(\theta) = \theta$. So, I will substitute that. So, we get,

$$V_{out} = a\sin(\omega_0 t) + a\cos(\omega_0 t)\left(\frac{K_{VCO}\beta}{m\omega_R}\sin(m\omega_R t)\right)$$

$$V_{out} = a\sin(\omega_0 t) + \frac{K_{VCO}\beta}{m\omega_R}\frac{a}{2}\left[\sin\big((\omega_0 + m\omega_R)t\big) - \sin\big((\omega_0 - m\omega_R)t\big)\right]$$

This is what you are going to see in the output spectrum. If $m = 1$, then I can write, I will just simplify this. So, further, you are going to see reference spur. You are going to see spurs at reference and its harmonics at all the places. So, $V_{out}(t)$ has the frequency ω_0 plus it also sees the magnitude $\frac{K_{VCO}\beta}{m\omega_R}\frac{a}{2}$ at $(\omega_0 + m\omega_R)$ and $(\omega_0 - m\omega_R)$. So, I will just plot this, that is better.

So, spectrum of V_{out} whatever value it has here, if this value happens to be 1, then you will see it is flanked by values at ω_R and so this is ω_0, you will see $(\omega_0 + \omega_R)$, $(\omega_0 + 2\omega_R)$ and this is $(\omega_0 - \omega_R)$, this is $(\omega_0 - 2\omega_R)$ and this amplitude is going to be at your m^{th} harmonic. So, amplitude at $(\omega_0 + m\omega_R)$ is given by,

$$\frac{K_{VCO}\beta}{m\omega_R}\frac{a}{2} = \frac{a\,K_{VCO}}{2m\omega_R}\frac{I_{CP}\,R}{m\omega_R}\sin(m\omega_R T_{os})$$

So, depending on your T_{os} value, you are going to see the spur. So, this is how I have worked out for one particular case when you have a current mismatch because of UP and DN. You can do the same thing for any mismatch whether it is UP and DN mismatch or it is a mismatch

because of the control voltage. The same logic will apply and you can always work this out. Thank you.