Phase-Locked Loops
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Lecture – 52
Circuit-level Design of Charge Pump: Part II

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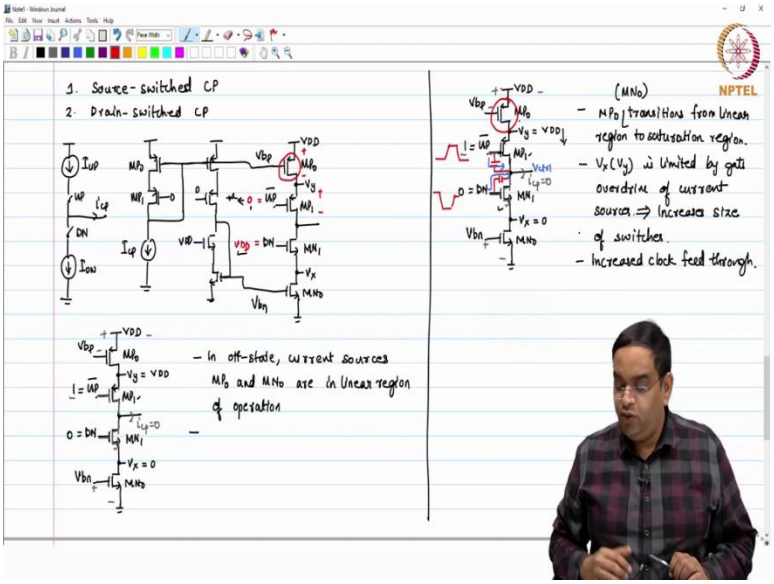

Hello, welcome to this session. Previously, we have looked at source-switched charge-pump which makes us feel that if there is source-switched charge-pump, then there should be something known as drain-switched charge-pump and gate-switched charge-pump also. So, let us look at them also one by one whether they are good or they offer something better. If they do offer better, then we should use them.

So, this is like in place of putting the switch at the top, I am going to have current at the top. So, I use these two switches, this is an ideal model of our charge-pump now, UP and DN and you have i_{cp} here, this is I_{UP} and this is I_{DN}. Typically, both these values of I_{UP} and I_{DN} are same. So, the charge-pump which we are going to implement now has a PMOS current source with a PMOS switch and then you have NMOS switch and NMOS current source.

So, if these are current sources, we know that they have to be biased. This is a switch, so, it is triggered at $\overline{UP}$. This is with DN and here this is VDD. These are MN_0, MN_1, MP_0 and MP_1. So,

for the current source, I will again use the replica based method to decide my current source bias voltage. I can try this, if this works, then fine.

So, I will have this as a 0 which is switch size, example, let us say, MP_1 itself and I am going to do the diode connection here and have an external current source of value whatever I want, I_{CP}. So, I do this and then once I generate the bias voltage which I get here, I will pass that current to another branch keeping the same replicas here and then this is connected to the switch, so, connected to VDD and then you have NMOS for which I want the bias voltage.

I do the diode connection here and this voltage is passed as V_{bp} and this particular voltage is passed as V_{bn}. Let us bring the charge-pump a little closer. So, this goes to VDD, goes here. So, this is our V_{bp} and this is our V_{bn}, these two things are V_x and V_y. So, in this case, what is going to happen when either of these UP or DN switches are on, let us look at that. So, let us start with the case when UP and DN both are off.

So, in that case, V_{bn}, so, V_{bp} and V_{bn} are always present. When $\overline{UP} = 1$ and $DN = 0$, at that particular time, this PMOS is off and this NMOS is also off. They do not conduct any current, $i_{cp} = 0$. When $i_{cp} = 0$, what is the value of, this is 1 by the way. You have $V_{SG} - V_{tp} > 0$ for PMOS and $V_{GS} - V_{tn} > 0$ for NMOS.

So, when these two things are there, in this case, what happens is that V_y potential will be pulled to VDD because there is no current going through this transistor MP_1. So, the only way is you do not supply any current, so, V_y gets pulled to VDD such that $V_{SD} = 0$ for PMOS and similarly V_x potential gets to 0.

So, in off state, your current sources MP_0 and MN_0 are in linear region of operation and when any of these MOSFETs turns on whether your MP_1 turns on or your MN_1 turns on, what is it going to do? If MP_1 turns on, then, so, let us say if your MP_1 turns on, then what is going to happen is that first this V_y potential drops from VDD to a low value such that your MP_0 goes from linear region of operation to saturation region.

So, MP_0 switches or transitions from linear region to saturation region. So, the current source is not active as soon as your MP_1 transitions. So, there is some transition delay when the current

source will become fully active and it will start giving the current as we want. So, there is some kind of current variation. Well, that will anyways be there, but there is a delay associated with this transition of the current source from linear region to saturation region and a similar thing will happen with MN_0.

So, this is one of the problems you can say as compared to the source-switched charge-pump because there the current source always remains in saturation. So, there is no transition delay going from linear region of operation to saturation region. Here, first your V_y node has to drop from VDD. Similarly, V_x node has to get charged to the desired potential, then only it will work like a current source which we want.

Now, the other thing which we have here is that the switches which you are having, now, if I keep both the switches like in this case, your $\overline{UP}$ signal at max is 0 and this signal is at max is VDD. Now, to keep the current source in saturation region, you need a certain voltage and for the switches, you would like to keep a minimum voltage between the switches.

So, if that is the case, across the switches, minimum voltage. So, if that is the case, then what happens is that your V_y voltage is actually limited by the gate overdrive of the PMOS transistor. So, you can say V_x and V_y is limited by the gate overdrive of current sources. Now if they are limited by the, if V_x and V_y is limited by the gate overdrive of the current sources which is actually you can say, $V_{GS} - V_{tn}$ for NMOS and $V_{SG} - |V_{tp}|$ for PMOS, is limited by this. This in turn increases the size of your switches. Earlier you were having the gate overdrive for the switches as the maximum allowed in a given process.

Because the source was pulled to VDD for PMOS and for NMOS, it was pulled down to zero, that is why you had the maximum overdrive. When you had the maximum overdrive, then the possibility of using a smaller size is more as compared to the case when you have a limited overdrive. You cannot make this voltage zero, it cannot be, you cannot make this voltage negative.

If you think that I can make this zero to a negative value, it is not possible in the given case. Similarly, your MN_1 gate voltage, you cannot increase more than VDD in a given process. So, with these two limitations, it automatically increases the switch size. When the switch size increases, then another problem comes that you have the capacitance connected from gate to drain and you

have transitions from 0 to 1 or 1 to 0 on these gate-switched nodes. Similarly on this side, these transitions now directly couple to the output. Previously that coupling was coming through the current source. Now, this coupling is directly to the V_{ctrl} node and the clock feed through effect is, so, you can say increased clock feed through.

So, looking at it, the good or bad part about it is that, by the way, the way we are looking at is we are only seeing the bad part about this drain-switched charge-pump. The bad part is that in off state, you have the current sources in linear region, they make a transition from linear to saturation when you turn on which creates the transition delays.

The second thing is that your switch sizes automatically increase because they are operating with a lesser gate overdrive. Now if they have a lesser gate overdrive, if they have a larger switch size, you have increased clock feed through and then you have increased clock feed through, you have increased ripple at the output.

So, this is something which you would not like to use if all these things are problematic. Maybe in some case, it is like in some cases, you may like to use PMOS because in this case you think that this is operating as a current source and if you have some current source biasing like this, you may try to use it but you will face all these problems.

So, that is about the drain-switched charge-pump. Thank you. In the next session, we will look at the gate-switched charge-pump.