Phase-Locked Loops
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Lecture – 51
Circuit-level Design of Charge Pump: Part I

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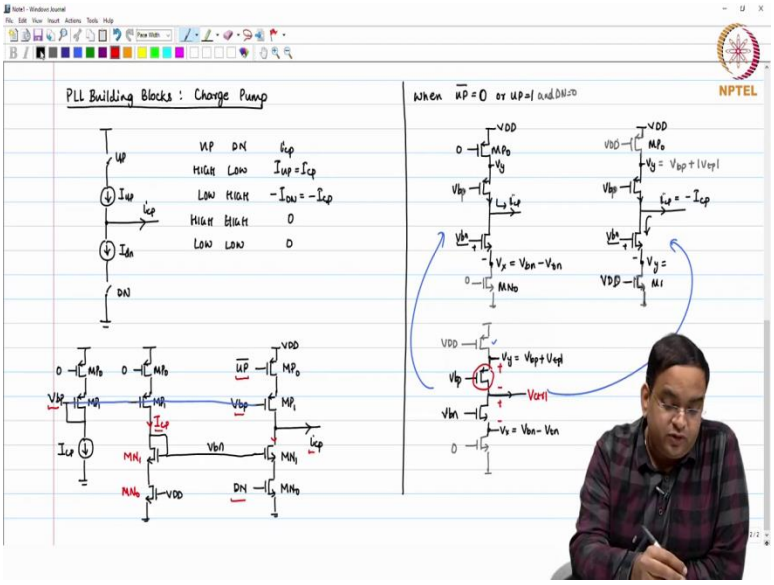

Hello everyone. Welcome to this session. We will continue our discussion on PLL building blocks and next under discussion is the charge-pump. So, if you look at it, the ideal charge-pump block diagram which we have used is this. This is triggered by UP, this is your I_{UP} current source which is typically equal to I_{DN} also and this is the DN switch, this is what we need. Ideally, when UP is high or if you want to have UP as logic high and DN is low, $i_{cp} = I_{UP} = I_{CP}$, the constant current.

When UP is low and DN is high and this $i_{cp} = -I_{DN} = -I_{CP}$. When both are high, at that particular time, your $i_{cp} = 0$ and when both are low, ideally no current flows, that is also 0. So, we want such kinds of characteristics from our charge-pump. So, let us look at what we can do.

So, to simply replace these UP and DN switches and the current source using MOSFETs, what I am going to do is, the switch UP is replaced with PMOS. And the current source is the current source which is having the current from top to bottom. So, this is also I am going to replace with

PMOS and this and DN current is going to be replaced by NMOS and DN switch is also going to be replaced by NMOS. This is connected to VDD.

Here, the DN switch or the PMOS switch, so, let us write MP_0, this is MP_1, this is MN_1 and this is MN_0, these are the switches. So, it will be controlled by $\overline{UP}$ because PMOS gets active when you have large V_{GS} and when $\overline{UP} = 0$. For this, you need to provide a bias voltage V_{bp} and here you need to provide a bias voltage V_{bn} and this one signal is DN, this is your output node, i_{cp}.

So, the way we are going to find, use this current source or this particular charge-pump, we have to generate the bias voltage in such a way that you get the desired current. So, to do that, the easiest way would be whatever switch I am using here, I use a replica of that switch and always connect to 0, let us say MP_0 and then you have a PMOS where I am going to find the bias voltage V_{bp}, going to generate this with an external current I_{CP}. So, this is, you can say, the ideal current source.

Similarly, this is your MP_1 only, the size is going to be the same. Similarly, I will use the same current, here I will pass on whatever bias voltage I have generated from the previous circuit. I will connect this V_{bp} here, pass this current or you can say force this current through NMOS and you have NMOS switch which is connected to VDD because when it operates, that is, switches VDD and you generate this voltage. So, what is going to happen is this particular node is V_{bn} and this node is V_{bp}.

Now, if you look at this circuit, this I_{CP} current generates the bias voltage V_{bp}, applies to PMOS and it forces the I_{CP} current through the NMOS. The size is the same, I am just writing MN_1 and MN_0 for example. It can be scaled, but for now, it is the same. When I_{CP} is forced here, you generate the bias voltage such that you get V_{bn}. So, now, in this charge-pump whenever $\overline{UP}$ signal is equal to 0, at that time your MP signal has the desired bias voltage and it is going to give the current $i_{cp} = I_{CP}$.

And whenever you have this DN signal as 1, at that time you have this current as I_{CP}. So, if you look at it, you look at both the operations, what is going to happen is that when $\overline{UP} = 0$ or $UP = 1$, at that time you are going to have in the charge-pump, this is 0, this is VDD and you have the current, this is V_{bp}. So, you have the current going, you have the option for the current to go out.

What you have on the other side is also NMOS whose voltage is V_{bn} and you have NMOS also connected whose gate voltage is 0 when $UP = 1$ and $DN = 0$.

So, in this case what is going to happen is the i_{cp} current which you see here, whatever current you get from the top, that current goes this side. Because of the presence of V_{bn}, this node potential, there is no path to the ground. This node potential will if I call this let us say as V_x and similarly this potential as V_y, your V_x potential will be such that the $V_{GS} - V_t$ for this transistor will be equal to 0.

So, this potential will be, during this state, it will be $V_{bn} - V_{tn}$ and the transistor cuts off. So, this is the case when you have UP signal as high. Similarly, what you will see is, when your DN signal is high, at that time your PMOS here will be turned off because this is VDD and you have your, this is V_{bp} by the way, and this V_y potential is given by,

$$V_y = V_{SG} - |V_{tp}| = 0$$

So, this potential will be,

$$V_y = V_{bp} + |V_{tp}|$$

and in this case, you are going to have, this is VDD. So, there is a current which is flowing from here in this direction. So, $i_{cp} = -I_{CP}$. So, if you look at it, the switch gets turned off because you have, here switch MP_0 is turned off, here switch MN_0 is turned off, here switch MP_0 is turned off, because their gate overdrive is equal to 0 and V_x and V_y potential, these potentials, depending on the voltage, these two potentials will actually change.

Now, so, this is the case how it operates. When you have both of them turned on, then the current flows from top to bottom. Now, what happens here is that when you are in the off state, when both the MOSFETs are off, so, if both the MOSFETs are off, we are in the state where you have this PMOS turned off and the bias current, you still have the bias voltage V_{bp}, you have the bias voltage V_{bn} and the NMOS is also turned off. From off state, you go to either of these on states.

This is what you have. So, these two potentials which you see, these two potentials, V_x and V_y in the off state are given by,

$$V_y = V_{bp} + |V_{tp}|$$

$$V_x = V_{bn} - V_{tn}$$

Now, when your UP or DN signals, they change their sign and one of it goes to either of these two states, then you look at the transition which is going to happen for different MOSFETs.

So, your PMOS switch is actually in cut-off, current source actually if you look at it, this current source, PMOS current source, you have, well, this is actually $V_{GS} - V_t = 0$ but V_{DS} which is your output voltage which is normally called as a control voltage, this control voltage will be somewhere in between the supply and this control voltage, your V_{SD} for this transistor and similarly V_{DS} for this transistor are quite large.

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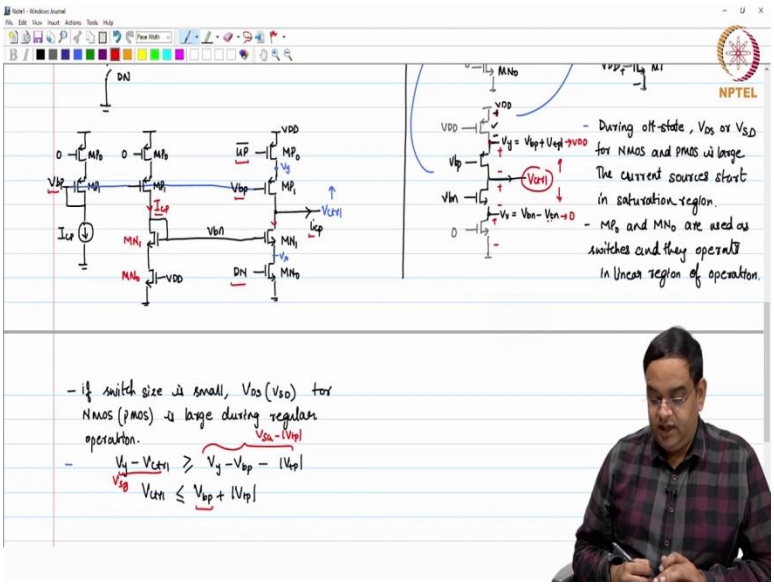

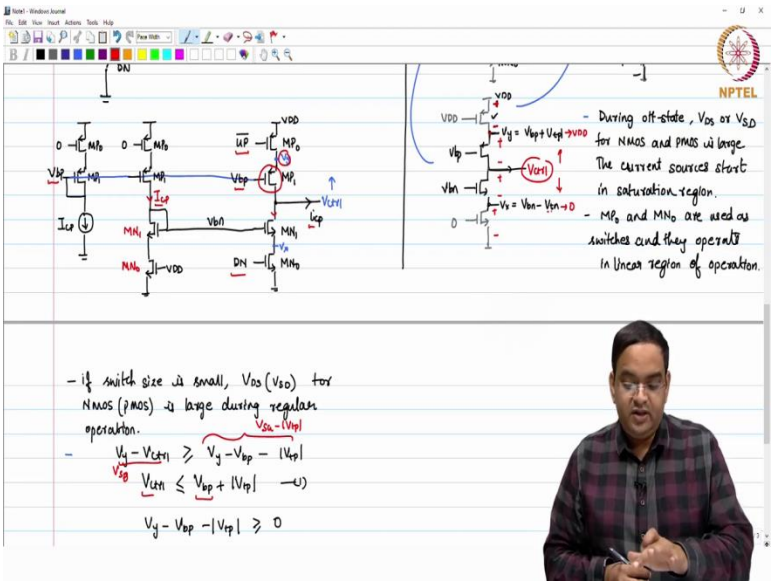

So, your current source is, I can write it that during off state, let me just make the arrow like this and write it here. During off state, V_{DS} or V_{SD} for NMOS and PMOS is large. And the current sources when you turn it on, the current sources start in saturation region. Why in saturation region? Because when you turn on this, as soon as your signal goes VDD or anything goes low or high, your V_y signal, in case it turns or your PMOS transistor turns high, your V_y signal will go to VDD, your V_{SD} will be large, your transistor will start in saturation.

Similarly, this particular potential will go to 0, V_{DS} will become large and you will start in a or V_{DS} is large to begin with and as soon as you start, V_y goes to VDD, V_x goes to 0, you start with a large V_{DS}, you start the current source in saturation region. That is what you will see. Now, it comes that these two transistors MP_0 and MN_0, these two transistors are used as switches. When these two transistors are used as switches, they operate in linear region of operation.

So, the current sources are in saturation region, the switches are in linear region of operation. So, when you are designing this particular charge-pump, the question will be that what size are you going to choose for these switches. So, for any given supply voltage if you look at, you know that I need some amount of current like i_{cp} depending on the headroom which you make available for your PMOS or NMOS switches during operation, you can choose the size of these two switches.

Now, if you choose a very low device size, if MP_0 and MN_0, they are having very small sizes, then what will happen is for the same amount of current because the gate overdrive is maximum when

they operate, it is either VDD here, $VDD - V_{tp}$ or this is $VDD - V_{tn}$. So, the gate overdrive for PMOS and NMOS switches is quite large whenever they operate. The only way you can reduce the potential drop across the V_{DS} terminals is by increasing the size.

So, you can say if switch size is small, then V_{DS} or V_{SD} for NMOS or PMOS is large during regular operation. Now, what will be the problem because of this? The problem is that if you have large V_{DS} or V_{SD} for NMOS or PMOS, then it limits the control voltage, how much control voltage it can go high or low, that is limited because we want the current source to remain in saturation. If the current source remains in saturation, then the maximum voltage which this V_{ctrl} can go is limited by this voltage.

So, for example, if you just want to look at it, you can think that, let me just put it here. This is our V_y and this is our V_x, these are the two nodes. So, your V_{ctrl}, we want our V_{ctrl} to vary for the VCO and V_{ctrl} can increase upwards till the time your PMOS remains in saturation. So, what is that value? So, we get,

$$V_y - V_{ctrl} \geq V_y - V_{bp} - |V_{tp}|$$

So, we get,

$$V_{ctrl} \leq V_{bp} + |V_{tp}|$$

That is the maximum that V_{ctrl} can go. If there is anything wrong, let us just check it. This is V_{SD} for PMOS transistor and this is $V_{SG} - |V_{tp}|$. So, when it is operating, this should happen. Now, this V_{bp}, here you do not see any direct relation with respect to V_y, but V_{bp} you also know that the transistor should operate. So, we have,

$$V_y - V_{bp} - |V_{tp}| \geq 0$$

This means that,

$$V_{bp} \leq V_y - |V_{tp}|$$

So, now, you see these two equations, because the transistor should also be on and V_{bp} is this, so $V_{bp} \leq V_y - |V_{tp}|$. So, you will see that how high V_{bp} can go which is this, and there should also be some, it cannot be directly equal to 0.

So, there is some kind of overdrive which you will have. So, because it is limited by V_y, so, your V_{ctrl} will finally get limited by V_y. So, while keeping the PMOS in saturation, this current source in saturation region during our regular operation, we have to keep our V_y large. Similarly, we have to keep V_x low and if your switch size is small, then you cannot do this. So, there is some optimum value which you need to choose.

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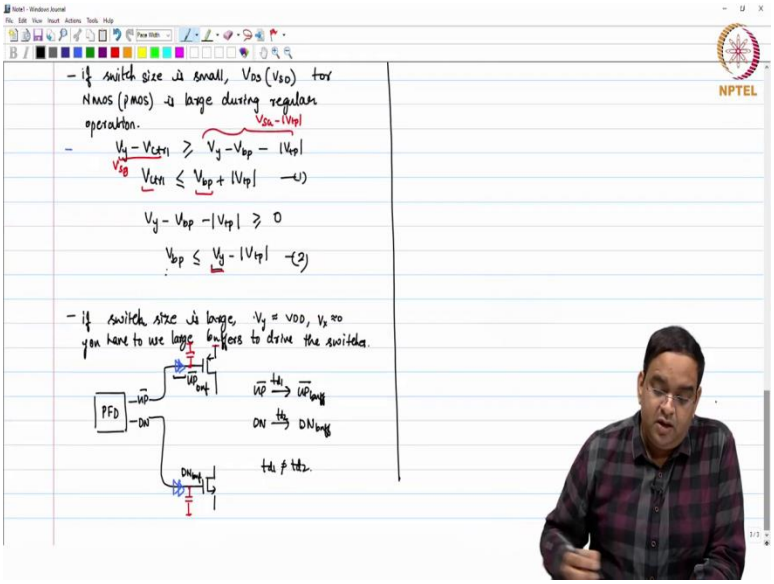

Then you say if switch size is a problem, then what I can do is I will choose a large switch size. If the switch size is large, then what happens? $V_y \approx VDD$ and $V_x \approx 0$. The switch size is large which means you can have a large amount of current without having a significant potential drop between the source and the drain terminal.

Now, what is the problem? The problem is two-fold. This particular switch whatever we are using in the charge-pump, these switches are going to be interfaced with the PFD. Let us say PFD gives you $\overline{UP}$ signal and it also gives you DN signal. So, somehow you have to connect this $\overline{UP}$ signal here and DN signal here.

So, if the gate size becomes too large, then C_{gs} of the PMOS transistor and C_{gs} of the NMOS transistor, these two transistors start dominating the load driven by PFD, and it is not something which any PFD can drive, you have seen the NAND based PFD. So, what do you need to do? To address that, you need to add buffers in between, you cannot directly drive it.

So, since you cannot drive it, you are going to add buffers in the chain. When you add buffers in the chain, if switch size is large, you have to use large buffers to drive the switches. This will increase the power consumption in the buffers and this will also increase the susceptibility of difference in the delay from the UP and DN pulse which is driving the switches.

So, this is $\overline{UP}_{buff}$ and this is DN_{buff}. Now you may get your $\overline{UP}$ and DN signal perfectly timed but when you are driving different loads, PMOS and NMOS, they have different mobilities. So, you will have a different switch size and you have increased the switch size so much that you have parasitic capacitor which needs some buffer to drive it.

So, you will add buffers. So, the delay from $\overline{UP}$ to $\overline{UP}_{buff}$, this is t_{d1} and the delay from DN signal to DN_{buff} which is t_{d2}, these two delays may not be equal and we have seen during the case of non-linearities in the charge-pump PLL, if these two delays are different, then you will see some leakage current going through the loop filter which will lead to an increase in the ripple.

So, this is one drawback of using a large switch size. The drawback of using a small switch size, you have also seen that it limits the control voltage. So, when you are designing this charge-pump, you need to take care of both of these. So, while doing that, you need to know how much control voltage do I need to sweep during the regular operation, based on that you will optimize the sizes.

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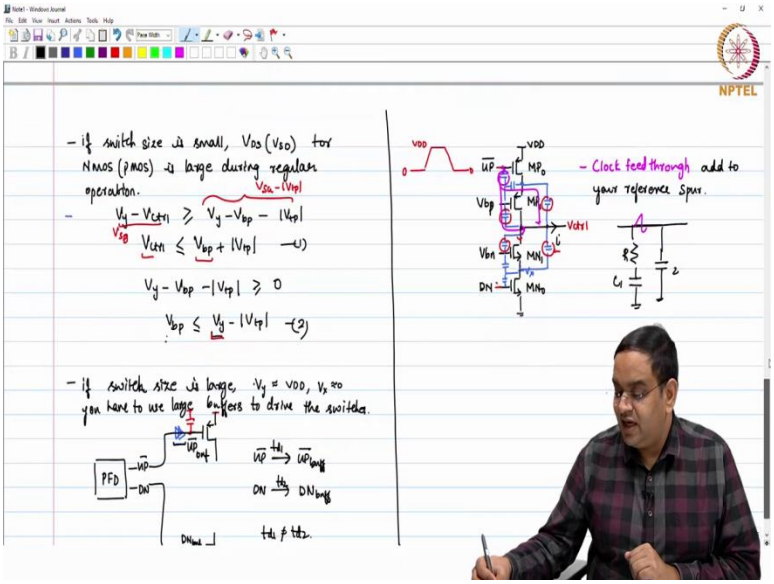

Then another problem is the following, when you have a large switch size by the way, it is not only that your driving is a problem, the other problem which you also see is the following. So, in this case, the case which we are considering with the charge-pump, there are capacitors for this current source itself because the current source operates in saturation region. So, normally the current source has a large size because its overdrive is small.

So, you have these capacitors connected C_{gd} like this. Similarly, you are going to have capacitors connected here and capacitors connected in this manner. These capacitors, they are not the same value but I am just drawing all these capacitors you have. Then there is also capacitor between C_{gd} here, so it is like every two nodes, I am showing you a capacitor because you have it there.

Now, two things will happen. One, because of these capacitors which are loading your output node, if you somehow keep these switch sizes or the current sources pretty large, you are going to change the loading at the charge-pump output. So, earlier you were having a loop filter with R, C_1 and C_2, now, all these capacitors give you another effective loading at the V_{ctrl} node.

So, when you design the loop filter, you may have that C_2 is some value and then when you put everything in the PLL, it turns out to be that the effective C_2 which you are seeing here is larger than the C_2 which you used here. And all that is coming because of the increased loading at this

point. So, if it happens, the problem is easy to fix, you can vary your C_2, extra C_2 which you are adding after taking these capacitors from the charge-pump into account, that is one thing.

The other thing is that when you make a transition at UP and DN node, whether you are making a transition going from 0 to 1 or you are going to make a transition from 1 to 0. So, when you make that particular transition, what happens is you see that at this particular node, the transition is going from 0 to VDD. So, it is not a small voltage difference transition.

So, any transition here travels to the output node because of these capacitors, it has multiple paths to travel. So, it travels to the output node in this particular manner and it causes a disturbance at V_{ctrl} node. This is called as clock feed through because UP and DN signals are coming at the clock rate and you are switching them.

So, it is like a clock and when this switching happens, the voltage here you think about it, $\overline{UP}$ voltage is changing from 0 to VDD, no matter who is driving it. So, this particular capacitor undergoes the transition and that charge flows through other capacitors and it travels to the output. So, because of the clock feed through at every reference frequency, you may see some kind of ripple.

So, clock feed through adds to your reference spur by the way. Ideally, how can you reduce that reference spur? By having a lesser number of capacitors. How can I have a lesser number of capacitors? By using small switch size. If I have a small switch size, is there a problem? Surely, there is a problem because then my V_{ctrl} voltage, that cannot go much higher. So, all these are trade-offs which you will see during the design of the charge-pump and you have to optimize based on your needs.

And then either that is the case or if your needs are much more than what the design can support, you look for some other architecture. Now, this kind of charge-pump which you see here, in this charge-pump, you are effectively switching the source node of the current sources, your MP_1 and MN_1, they are current sources, you are switching the source nodes of the current sources.

So, it is normally called as source-switched charge-pump. So, you have seen all the good and bad parts of this particular charge-pump and now you may think that if I am switching at the source, I am seeing this stuff. So, is there a way that I can do something better, let us say in terms of the

output swing or V_{ctrl} swing or in terms of the region of operation. So, let us look at it in the next session. Thank you.