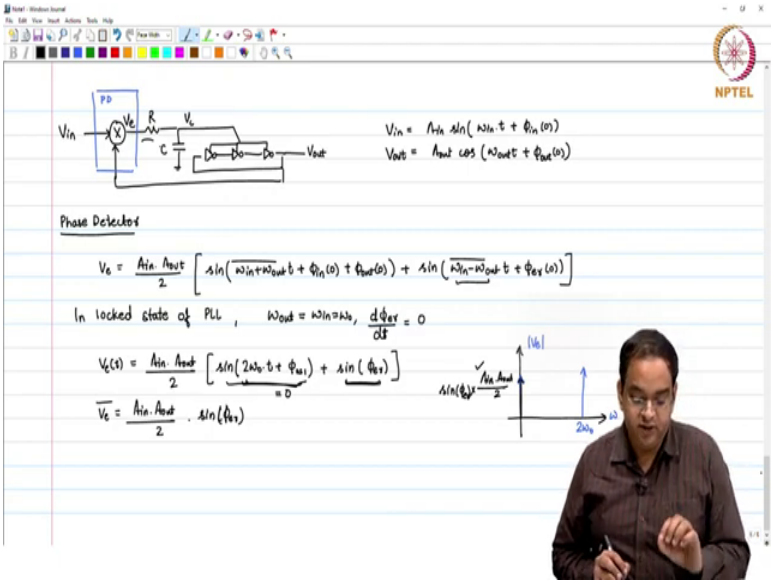
Phase-Locked Loops
Dr. Saurabh Saxena
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture − 5
Input-Output Characteristics of Basic PLL Blocks

(Refer Slide Time: 00:15)



In this session, we are going to look at the PLL blocks which we used in our simple implementation of the PLL block diagram where we used a mixer to get the phase error, then we had a loop filter followed by the VCO. So, first part was the phase detector, and this is something which we have seen, we will go in a little bit more detail for this phase error detector.

So, this part is phase detector. Our input and output signals are sinusoidal, so I will just write it here.

$$V_{in} = A_{in}\sin\left(\omega_{in}t + \varphi_{in}(0)\right)$$
$$V_{out} = A_{out}\cos\left(\omega_{out}t + \varphi_{out}(0)\right)$$

So, from the previous exercise, we know that,

$$V_e = \frac{A_{in}A_{out}}{2}\left[\sin\left((\omega_{in} + \omega_{out})t + \varphi_{in}(0) + \varphi_{out}(0)\right) + \sin\left((\omega_{in} - \omega_{out})t + \varphi_{er}(0)\right)\right]$$

This is to begin with.

So, this is what we have as the error voltage for the phase error detector in the locked state of the PLL. When will we say that the PLL is locked or in steady state? When the output frequency is equal to the input frequency and when the phase error does not change, you have a constant phase error, if any. So, if that is the case, then,

In the locked state of PLL: $\omega_{in} = \omega_{out} = \omega_0$, $\frac{d\varphi_{er}}{dt} = 0$

The error voltage is given by,

$$V_e(t) = \frac{A_{in}A_{out}}{2}[\sin(2\omega_0 t + \varphi_{os1}) + \sin(\varphi_{er})]$$

So, you will have some steady state phase error, whether that is zero or not that is not something which is important for the locking of the PLL. What is important is whatever phase error you have, that should be constant in the locked state. So, in the locked state, you have the error voltage given by this.

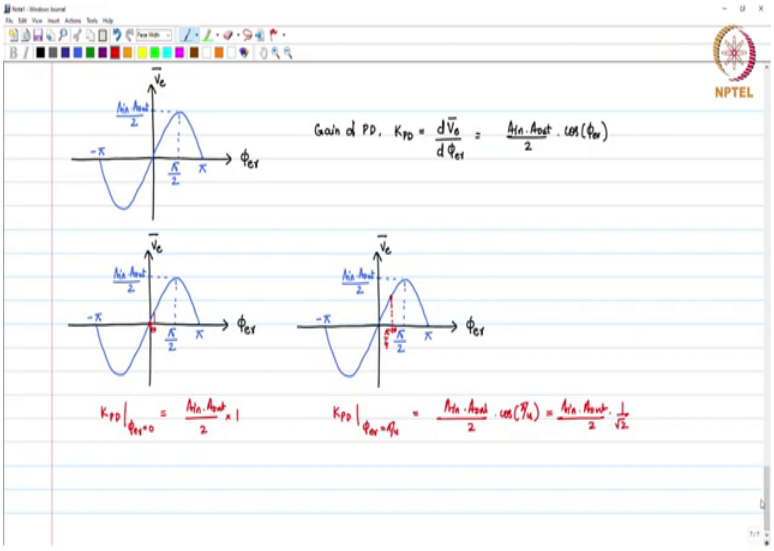
Now, if the error voltage is like this, it is having a $2\omega_0$ component and it has a fixed component. So, there are two portions, one is variable and the other which is not changing. If you have a filter at the output of the phase error detector, then the filter will pass on the DC component of the phase error. So, I will just plot here what all error voltage components you have. You have here, one is you have a DC component which is $\sin(\varphi_{er})$ and the other component is at $2\omega_0$.

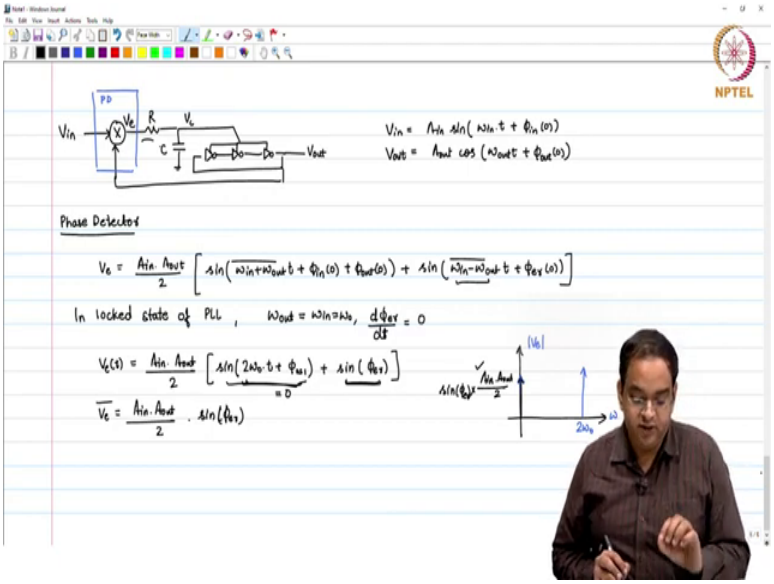
So, this is the frequency spectrum of the error voltage. So, for phase error detector, we define the average of the error voltage in steady state. The average of the error voltage in steady state is given by,

$$\overline{V_e} = \frac{A_{in}A_{out}}{2}\sin(\varphi_{er})$$

The average voltage for $\sin(2\omega_0 t + \varphi_{os1})$ term will be equal to 0. So, the component which you are going to see here is $\frac{A_{in}A_{out}}{2}\sin(\varphi_{er})$. So, if you look at the operation of the phase error detector as we saw earlier, there are two components and the average voltage of the phase error detector output is $\sin(\varphi_{er})$.

(Refer Slide Time: 06:57)





As I said, in locked state, the phase error does not change. If the phase error does not change, the average error voltage is going to be fixed and this average error voltage as you see is having $\sin(\varphi_{er})$. So, this is little interesting that the average error voltage at the output of the phase detector is not a linear function of the phase error. It is actually a non-linear function and that non-linear function is sin wave here, like this.

This is your phase error π and this is your phase error -π. The peak amplitude is going to be $\frac{A_{in}A_{out}}{2}$ and the peak appears at phase error π/2. So, if I would like to define the gain of this phase error

detector (K_{PD}). It is defined as the derivative of the average error voltage with respect to phase error.

$$K_{PD} = \frac{d\overline{V_e}}{d\varphi_{er}} = \frac{A_{in}A_{out}}{2} cos(\varphi_{er})$$

Why is this important? It is important because in case your PLL is locked and you make any change, so, let me just pick up this case that my PLL is locked and I will use two cases. In one case, the PLL is locked to phase error of 0. So, if I lock to a phase error 0, at this particular point, if I make any change in the input phase of the PLL, that means that I am going to change some phase here at the input of the PLL, the gain by which my output is going to change, that gain is going to be close to the value which you have near phase error equal to 0.

So, what is the gain for phase error equal to 0?

$$K_{PD}|_{\varphi_{er}=0} = \frac{A_{in}A_{out}}{2} \times 1$$

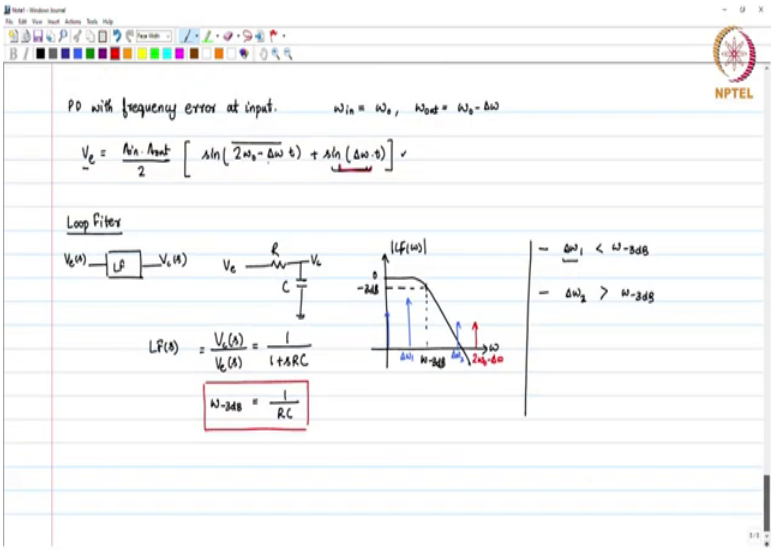
If the phase error in the locked state happens to be π/4 and I make any small change around that phase error of π/4 in steady state, the gain of the phase error detector is different.

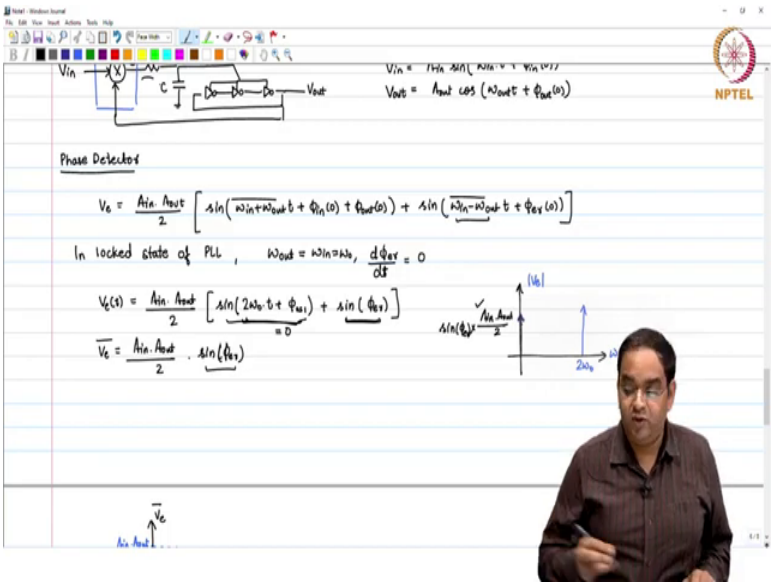
$$K_{PD}|_{\varphi_{er}=\pi/4} = \frac{A_{in}A_{out}}{2} \times cos(\pi/4) = \frac{A_{in}A_{out}}{2} \times \frac{1}{\sqrt{2}}$$

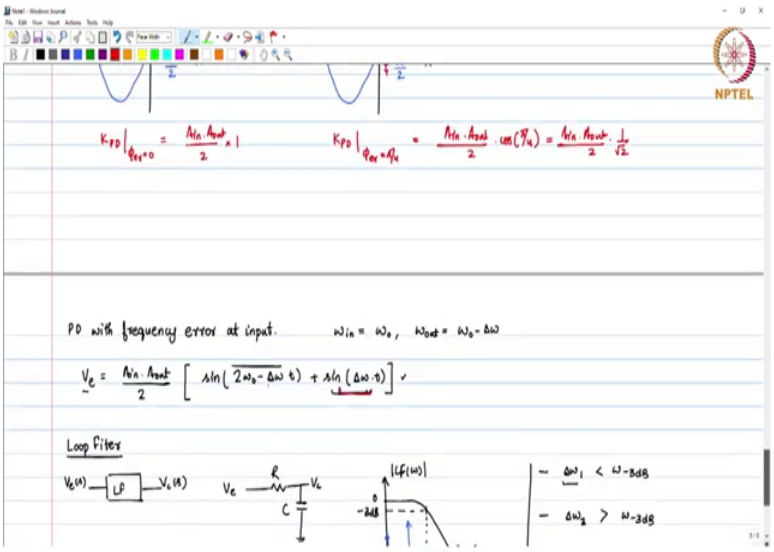
So, if you think about it, in the same PLL in locked state, we can have different phase errors and in the locked state, if you make any change in the input phase errors, then what you will see is the gain by which your error voltage is going to change is going to be different.

So, it is not linear, that is why this happens. Whether this will have any consequence on the operation of the loop in steady state, this is something which we will see later. Now, for this particular phase error detector, we see how it operates. Another important part here is the case when you have frequency error. So, I will just deal with the case with frequency error.

(Refer Slide Time: 12:00)







PD with frequency error at the input:

So, let us say when you start your PLL, you have frequency error at the input. So, I will just write here that $\omega_{in} = \omega_0$, and $\omega_{out} = \omega_0 - \Delta\omega$ so that our expressions simplify. So, in this case, the error voltage is given by,

$$V_e = \frac{A_{in}A_{out}}{2}\left[\sin\left((2\omega_0 - \Delta\omega)t\right) + \sin(\Delta\omega t)\right]$$

So, even when you do not have phase error to begin with, you have only frequency error, we have seen earlier you get a component which is proportional to $\Delta\omega$. So, for small frequency errors $\Delta\omega$, the error voltage is going to be proportional to that frequency error. This is important when we are considering the loop filter. That is why I brought this up here that the output of the phase error detector does not have information only about the phase error, but it has information about the frequency error also.

So, when we consider the loop filter which we have seen earlier as a simple RC filter, you can have any kind of filter there, but to begin with, we used a simple RC filter. So, this is $V_e(s)$ and $V_c(s)$ in our case. The example which we took earlier was this R and C, this is our V_e, this is our V_c. The loop filter transfer function in this case is going to be,

$$LF(s) = \frac{V_c(s)}{V_e(s)} = \frac{1}{1 + sRC}$$

The bandwidth of this filter (ω_{-3dB}) in radians per second is given by,

$$\omega_{-3dB} = \frac{1}{RC}$$

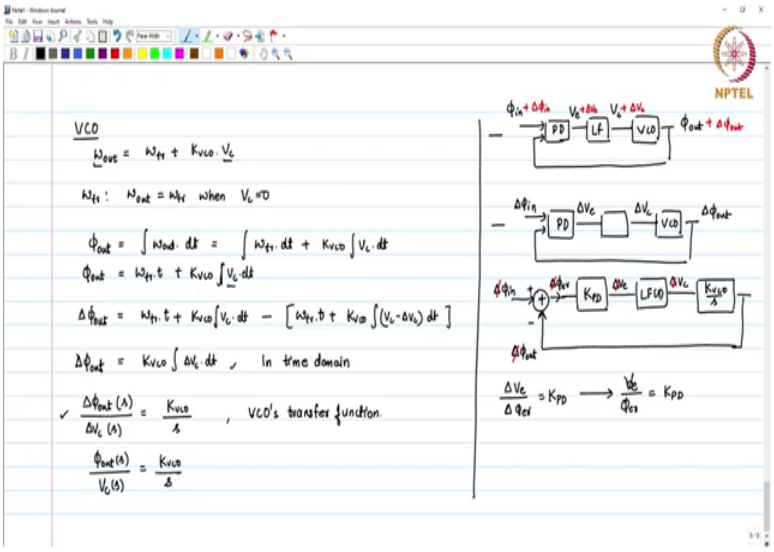
So, for this particular loop filter, I will write this as |LF(ω)| here and what we have is this filter transfer function and we can take this as -3 dB bandwidth.

Now, when we considered the phase error detector with only phase error with no frequency error, we had a constant term which is DC term. So, a loop filter with any bandwidth will be able to process that phase error information with no frequency error like the phase error in steady state or the phase offset. But if you have this frequency error $\Delta\omega$, it very much depends whether you are having this $\Delta\omega$ component here or you are having the $\Delta\omega$ component here.

We take two cases, $\Delta\omega_1$ and $\Delta\omega_2$. In the first case, $\Delta\omega_1 < \omega_{-3dB}$. So, when you start your PLL, you have frequency error and if the frequency error is lesser than the bandwidth of the filter, the information about the frequency error is present in this variable, $\sin(\Delta\omega t)$. It is not going to be filtered by the loop filter and the output frequency of the VCO will change in the desired manner. In the other case, where $\Delta\omega_2 > \omega_{-3dB}$, even when you have the frequency error information in the error voltage, that is going to be filtered by the loop filter because that is coming beyond your filter bandwidth. So, if you are rejecting the frequency error information by the loop filter, the VCO will not be able to correct for that frequency error.

In both the cases, if the frequency error is small, most of the time your other frequency component which is $2\omega_0 - \Delta\omega$ will lie much beyond the filter bandwidth, that will be rejected most of the time unless you choose a very wide filter where even the $2\omega_0 - \Delta\omega$ component will come in, that is not a practical case. So, while you are choosing the filter bandwidth, it is very important to keep in mind what kind of frequency error you are targeting to compensate or trying to recover in the PLL. So, this is a very basic implementation and basic requirement of the loop filter.

(Refer Slide Time: 18:26)



The next important block which we have been using is the voltage controlled oscillator. We need to know how this output frequency changes. So, here we have seen earlier that,

$$\omega_{out} = \omega_{fr} + K_{VCO}V_c$$

This is what we have seen earlier. Now, in this particular case, if you make any change in the control voltage, you are going to change ω_{out}. ω_{fr} is the free running frequency which you have as ω_{out} when the control voltage is 0.

$$\omega_{out} = \omega_{fr}, \text{ when } V_c = 0$$

Here, we are considering that our control voltage is greater than 0.

$$\varphi_{out} = \int \omega_{out}\, dt = \int \omega_{fr}\, dt + K_{VCO} \int V_c\, dt$$

$$\varphi_{out} = \omega_{fr}\, t + K_{VCO} \int V_c\, dt$$

So, what you see here is that you have an integral with respect to control voltage.

Now, given this relationship where ω_{fr} is always there, most of the time we are interested in the change in output phase with respect to the change in the control voltage as given by,

$$\Delta\varphi_{out} = \omega_{fr}\, t + K_{VCO} \int V_c\, dt - \left[\omega_{fr}\, t + K_{VCO} \int (V_c - \Delta V_c)\, dt\right]$$

So, the change in the output phase with respect to the change in the control voltage is given by,

$$\Delta\varphi_{out} = K_{VCO} \int \Delta V_c\, dt, \qquad \text{In time domain}$$

Why are we interested in this? Because in locked state, if you make any change in the phase error by changing either the input phase or output phase, that is going to change the error voltage which will change the control voltage. So, we would like to see how we change the output phase and the relationship is shown here. Now, an interesting part is the expression which you are seeing is in time domain. If we convert this expression into frequency domain, what is it going to be?

$$\frac{\Delta\varphi_{out}(s)}{\Delta V_c(s)} = \frac{K_{VCO}}{s}$$

This is an integrator. This is the transfer function of the VCO. So, interestingly, if you look at it, for the phase error, we found the time domain waveforms and most of the time we use K_{PD} which is proportional to the phase error, a constant gain, most of the time that is what we are going to use, that gain may vary depending on the phase error which you have in the locked state. With respect to the loop filter, we have a fixed voltage transfer function and with respect to the VCO, our transfer function is from the control voltage to the output phase.

So, quite often what we do is that we become lazy in writing Δ all the time. So, we say,

$$\frac{\varphi_{out}(s)}{V_c(s)} = \frac{K_{VCO}}{s}$$

This is the transfer function of the VCO. Well, it may or may not be necessary that these things are mentioned explicitly, but when we are writing the transfer functions for the PLL block where you see all kinds of non-linearities, you have a mixer, you have a voltage to frequency change and so on, most of the time we are interested only in small changes in the PLL block while writing the transfer functions of the PLL.

So, let me just write it down that in actual PLL, you have PD, you have loop filter and you have VCO. When I represent all these blocks by their respective gains, what I am interested in is for the small changes in the input and the output. So, absolute terms are φ_{in}, φ_{out}, V_e, V_c. When I define

the gain of different blocks, the interesting thing to me is when I change my input phase by $\Delta\varphi_{in}$, it is going to change the error voltage by ΔV_e which will change the control voltage by ΔV_c which will change the output phase by $\Delta\varphi_{out}$.

So, these are all the small changes in steady state error, phase and frequency variables and the voltages. So, when we write the gain of all these blocks, what we are analyzing actually is, we have phase detector, loop filter and VCO, and the interesting parts to us are $\Delta\varphi_{in}$, ΔV_e, ΔV_c, and $\Delta\varphi_{out}$. For a small change in the phase error, we have seen for the phase error detector what kind of gain do we have, K_{PD}. So, this is operating on the phase error.

So, the small signal block diagram or you can say the analysis block diagram for the PLL, you have phase error which comes at the output of the PD. So, I have $\Delta\varphi_{in}$, and $\Delta\varphi_{out}$ to be coming from the feedback, this is positive, this is negative. This is $\Delta\varphi_{er}$ and this error gets multiplied by the gain K_{PD}. It gives you error voltage ΔV_e which gets multiplied by the loop filter transfer function. By the way, the loop filter is passive here with R and C, it does not change whether the input is small or large. You have ΔV_c here and then you have VCO whose transfer function we found is $\frac{K_{VCO}}{s}$.

So, this is the block diagram, or you can say the small signal diagram which we are going to use in our analysis for small changes in the input and output. And because we have to draw this diagram time and again, what are we going to do? We are going to drop this Δ everywhere and we say, we are having φ_{in}, φ_{er}, and so on. So, actually, we have,

$$\frac{\Delta V_e}{\Delta\varphi_{er}} = K_{PD}$$

But, mostly we will write,

$$\frac{V_e}{\varphi_{er}} = K_{PD}$$

This is just to drop the Δ from our analysis, but we are dealing with small changes only. Thank you.