Phase-Locked Loops
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Lecture – 49
Circuit-level Design of PFD: Part II

Welcome to this session. We were discussing the D flip-flop based PFD in the last session, and the problem which we found was that the reset time period and the overlap delay were the same, and in order to increase the overlap delay, you will end up increasing the reset delay, and what you will see there is that if you have a large T_{RST} delay, then it limits the reference frequency at which your PFD can be clocked.

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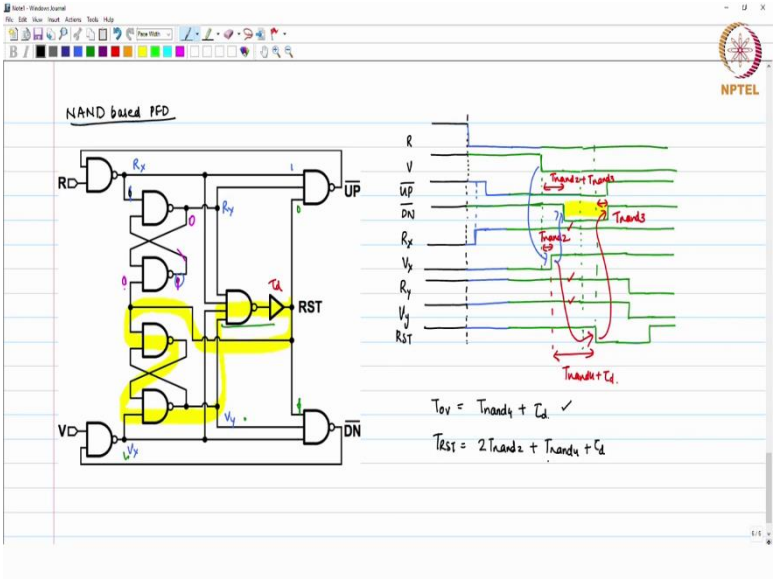

So, to overcome some of those problems, we have a NAND based PFD. Let us try to understand that. So, in this NAND based PFD, let us name these nodes so that it is easier to understand how it operates. So, what you have, this node is R_X and this node is R_Y. Similarly, this node is V_x and this node is V_y. Here, this particular PFD changes when you have negative transitions at R and V.

So, to begin with, let us say your R and V both are actually high. This is just an example. So, I am taking R and V both as high. If R and V both are high and then what you have here is that your $\overline{UP}$ and $\overline{DN}$, these two nodes are also high. So, $\overline{UP}$, when $\overline{UP}$ and $\overline{DN}$ are also high, in that case, your R_X will happen to be 0 because it is a NAND gate, both the inputs are high, V_x will also be equal to 0.

So, R_X is 0, V_x is 0 which will reinforce that R_Y is high and similarly, V_y will also be high initially. So, R_Y and V_y are high, and your R_X and V_x are 0. And if you look at the reset, in the reset, you have R_X, R_Y, V_x and V_y. So, the reset pin is going to be, because you have 0 at the input of the NAND gate, what you will have is reset is also going to be high.

So, reset is high. Now, you look at it, this is 1, this one is 0. So, 0 is going to give you 1 here, and 1 is 1, 0 this is enforced. Now, you have a transition here on the negative edge, you have a R transition here, when R goes from 1 to 0, your R_X is going to go from 0 to 1. R_X goes from 0 to 1. So, when your R goes from 1 to 0, R_X goes from 0 to 1.

When R_X goes from 0 to 1, what you have this R_Y was already 1, reset was 1 and this goes also to 1, your $\overline{UP}$ signal will actually go from 1 to 0. This is what will happen at $\overline{UP}$. So, R_X goes from 0 to 1, this signal becomes 1. So, reset did not change. So, it is a NAND input. If we had 0 here on this branch earlier, then this is still reinforced, R_Y does not change. So, all the signals carry the same way.

Now, after some time when the other rising edge comes, your V signal goes from high to low, let us say. This goes from high to low. When V signal goes from high to low, the DN signal will also go low, but before DN signal, your actually V_x signal goes high, and V_x signal goes high after how much delay? V_x signal will go high after one NAND2 delay.

So, V_x signal goes high. When V_x signal goes high and then after the V_x signal, your $\overline{DN}$ signal will go low. So, now you look at it, at this particular point, you have your V_x signal high, you have your R_X signal high. So, both R_X and V_x are high, R_Y and V_y were high earlier. If all the signals for this NAND gate become high, then the reset signal will go low. So, these two signals continue now.

Now, as the reset signal goes low after some time, what happens? Reset signal goes low, so your $\overline{UP}$ and $\overline{DN}$ signal both will now go back to high again. So, based on our reset signal going low, our $\overline{UP}$ and $\overline{DN}$ signal go high again. Well, R and V, they are still 0 here. So, R_X and V_x, since R and V signal are 0, R_X and V_x signal will remain 1, they will not change. So, R_X and V_x signals do not change.

Now, what happens to R_Y and V_y? Now, you see reset signal goes low. Then just trace this curve, reset signal goes low, it becomes, this is low. If this becomes low, then this is 1. If this

is 1, and for this NAND gate it was already 1, so, it was already 1, this will become 0. So, R_Y will become 0 and R_Y is going to become 0 after two NAND delays.

So, R_Y, R_X, this is here, R_Y goes to 0 after two NAND delays and V_y signal will also go to 0. So, R_Y and V_y signals, both these signals will go to 0. As R_Y and V_y signals go to 0, then after this NAND4 delay, your reset signal will again become high because the input is 0. So, your reset signal again becomes high, V_y has changed to 0, it remains at 0 and reset becomes high.

So, what you get is V_y remains here like this because R_Y is held at 0, and then that anything will change only when your R signal will go high again. So, this is what you have. Now, let us just look at the delays and the overlap period. So, if you look at it, the overlap period between the UP and DN signals or $\overline{UP}$ and $\overline{DN}$ signals in this case is this much. And how do we calculate this overlap?

So, whenever V goes low, with respect to V, your $\overline{DN}$ goes low. And when you have V, first V_x goes low, then from V_x, your $\overline{DN}$ signal goes low. So, what you see here that delay is from V to V_x, V_x to $\overline{DN}$, that is one nand2 and one nand3 delay. And after that, from your V_x signal because everything was high. So, your $\overline{DN}$ signal is here, from your V_x signal, your reset signal actually goes, look because your V_y was already 1, R_Y was 1 and R_X was also 1, what you only required was V_x as 1.

Once V_x goes 1, then after this, you get the reset signal. So, this delay itself is your T_{nand4} plus whatever this delay τ_d if you are having, you have this delay here τ_d. Now, till this $\overline{DN}$ is this much delay is only $T_{nand2} + T_{nand3}$, this is the delay. And from your reset signal to your this particular one is T_{nand3}, this one is only T_{nand3}. So, you can actually and this delay is V_x delay is only T_{nand2} delay.

So, if you work out all these things, what you are going to find is that,

$$T_{ov} = T_{nand4} + \tau_d$$

That is the thing which you have. And the reset signal if you think about it, the reset signal is without going to the diagram also, you can see once the reset signal goes high, it goes through these two NAND gates, and then one $T_{nand4} + \tau_d$. So, we get,

$$T_{RST} = 2T_{nand2} + T_{nand4} + \tau_d$$

So, here you can say your reset time appears to be or it is actually large, and your overlap time is smaller, but there is some kind of, you can say earlier we had both the overlap time and the reset time, they were same, but now they are depending on the gate delay.

Normally, you have your clock-to-Q and your flip-flop delays larger than the gate delays. So, we are able to reduce the reset time by having only the logic delays. So, with the gate delays, we are able to reduce the reset time but at the same time, at the same instant, we are also reducing the overlap time. So, we have to do something where our overlap time is actually larger, and our reset time is actually smaller, or we can increase our overlap time.

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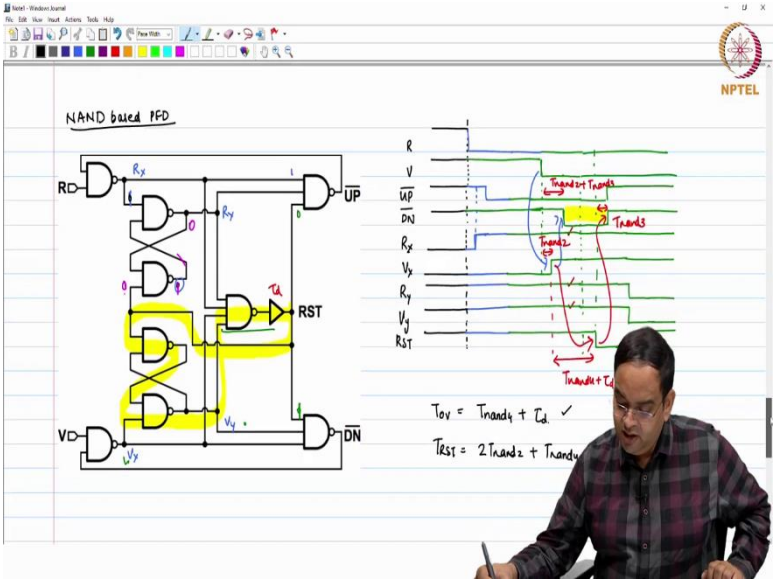

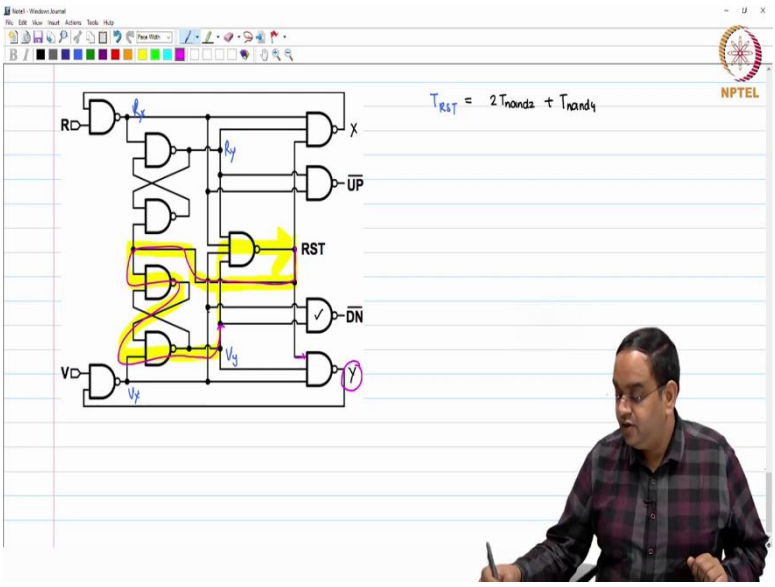

So, in this particular case, we remove τ_d which was earlier, this is same t_d which was earlier here, this t_d we removed, so, we do not have this anymore, and if you look at it, in this case, the T_{RST} delay, since we have gone through one of the NAND based PFDs in more detail. So, looking at the reset, once the reset goes high, it is going to go come through the latch, and this latch is going to come back like this. So, we get,

$$T_{RST} = 2T_{nand2} + T_{nand4}$$

Now, the other thing is if you look at, earlier, we named these nodes as R_X, R_Y and this one was V_x and V_y. So, in this particular case when our V_x node, when in the previous case, as soon as V goes low, what happens is our V_x node will also go low.

As V, because $\overline{UP}$ and $\overline{DN}$, these two signals, let us call these two signals X and Y. X and Y signals were initially high and R and V were also high. As V signal goes low, V_x will go high, and when V_x goes high, V_y and other signals were already, what were these signals V_y and R_Y? They were already high. So, when those two signals were already high, then it took like nand3 delay to get them.

So, now, here what happens is, as soon as V_x, V_y was already high, as soon as V_x signal goes high, you have one nand2 delay after which it goes, $\overline{DN}$ signal goes low. The difference here is that once your reset signal goes high, it actually, previously the reset signal was making our Y signal to go high again. Now, the reset signal has to, even if the reset signal goes high, it has to wait and come through these NAND latches, and then make our V_y signal to go high. So, you increase this V_y. Only when V_y signal will change, then only things will change here.

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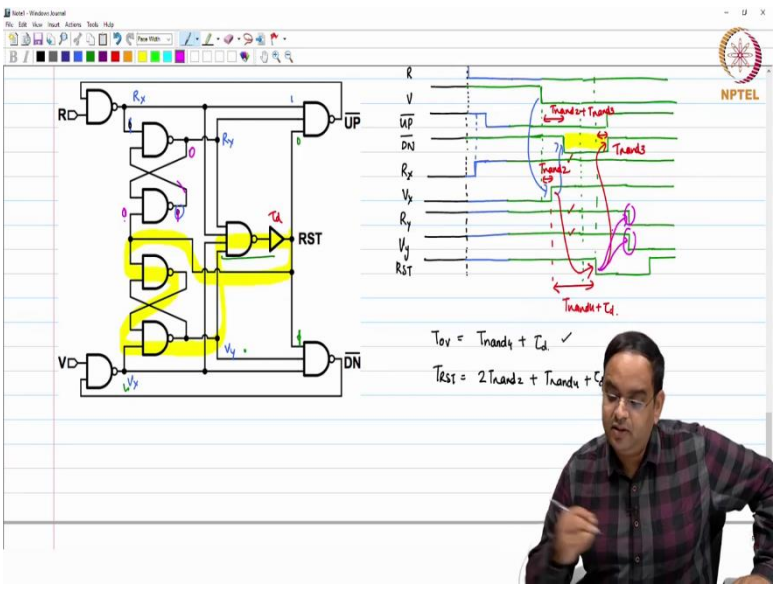

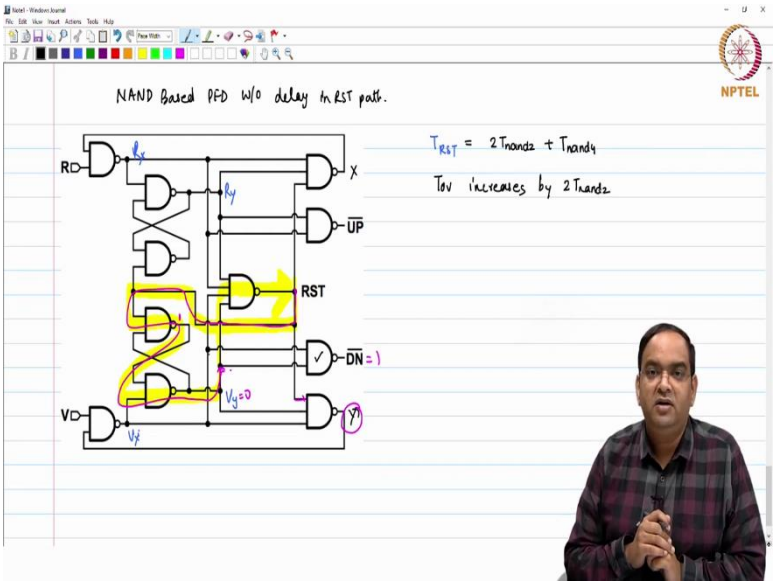

So, if you look at it, our R_Y and V_y signal, the reset signal is actually making a change here. So, when reset signal goes low, as you see when reset signal goes low, this output is going to be 1, this output is 1, V_x was already 1, then V_y will go to 0. And then when V_y goes to 0, then this $\overline{DN}$ signal will go back again. So, effectively, you increase the delay of UP and DN signal by two of these NAND gates.

So, I will call this as NAND based PFD without delay in the reset path. In this particular case, you see that your T_{ov} increases. Earlier, as soon as the reset signal went low, what happened? You actually made Y=0. But now it has to come through, we have used one more NAND gate, now it increases by $2T_{nand2}$. So, we want to increase T_{ov}, we are able to increase T_{ov} without changing the reset time. Thank you.