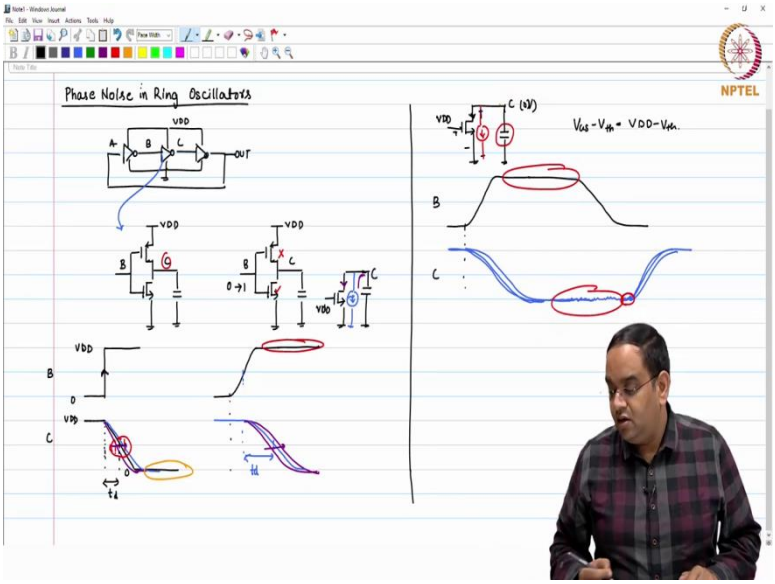
Phase-Locked Loops
Dr. Saurabh Saxena
Department of Electrical Engineering
Indian Institute of Technology Madras

Lecture – 47
Phase Noise in Ring Oscillators

(Refer Slide Time: 00:16)



Hello everyone. Welcome to this session. In this session, we will talk about the phase noise in ring oscillators. So, we have so far learnt how to design full-swing ring oscillators. And now we will look at phase noise in ring oscillators at least to understand how these sources of noise affect your output jitter.

So, consider that you have inverters in the ring oscillator, that is what we all know and they are all controlled by the supply voltage whether that is regulated or not, it depends. So, you have this. You pick up any one inverter, let us say, you pick this inverter. So, what you have is PMOS and NMOS and it is loaded by another inverter, by the way, in this case. It has this VDD and you have output here, so I will mark this as VDD. Let us call this as A, B and C.

So, I am modelling all the capacitor which you have here like this, C capacitor. So, if you consider only this inverter, let us consider two cases when, first case is for this inverter, I will take B=0. This is 0 and it changes from 0 to 1. So, when it changes from 0 to 1, for easy understanding, I will say, let us say, you have this change from 0 to 1 like this, 0 to VDD in our case. So, when you have 0 to VDD, at that time, when B was 0, C would be high.

So, here I will consider that B changed from 0 to VDD, this is just a signal which I am showing you and when this happens, your NMOS gets activated and your PMOS is turned off. So, what happens is when PMOS is turned off, I can say that this particular MOSFET is turned off, then you are effectively discharging the capacitor with NMOS whose input has gone to VDD.

When you are discharging this particular capacitor from 0 to VDD, ideally, if the current in the NMOS is the only current source which discharges this capacitor to ground, then no matter whether the transition comes now or the transition comes sometime later, you would always discharge in the same way.

If the current through the MOSFET without any noise, if the MOSFET follows whatever, whether it follows linear, saturation or any particular equation, any particular relation, if that remains fixed, then the transition from VDD to 0 will always happen at a fixed interval of time t_d but what happens in reality is that this MOSFET comes with a noise source. Whenever this MOSFET is active, it has a noise source.

When you have a noise source, this transition point changes, sometimes it can be like this, sometimes it can be like this, it will keep on varying, this transition will keep on varying. And this transition itself is whatever transition you are having from VDD to 0, this 0 midpoint, crossing of the midpoint is the reflection of how much the phase deviates or whether there is an error or not in the midpoint crossing in the clock.

So, in case of clock, we always look for the time instant of transition, whether from 0 to VDD or VDD to 0. So, here in the presence of noise, this transition will change. I showed you initially that you have a straight line like 0 to 1 going in a fixed manner or in zero amount of time, but you are going to have rising edge like this. In response to this rising edge, ideally your falling edge should be, whatever it is, it should always be fixed.

If the rising edge is fixed, the falling edge should also, this t_d should be fixed, but what happens in the presence of noise because when you are discharging the capacitor, the time instant at which this voltage will reach $\frac{VDD}{2}$, it depends on the current in the MOSFET and the noise also, noise of the MOSFET will also play a role.

So, what you see, you see something moving like this. Sometimes it is like this, these things keep on changing. And it is random, it is not fixed. At one instant of time, it will be δ_1, at other instant of time, it will be δ_2 and so on. So, this is how the noise affects the clock transitions when you are charging or when you are discharging, in both the cases.

Then what happens is that let us say when you have discharged the capacitor, at that particular instant of time, the input has reached VDD and the output is actually, this output has reached to ground also, for C node, the output is equal to 0, 0 V. But if you look at it, you have this particular NMOS transistor whose gate overdrive $V_{GS} - V_{th} = VDD - V_{th}$. This is like a good amount of gate overdrive.

So, the reason that there is no current is because $V_{DS} = 0$. Now, there will be some kind of leakage current or V_{DS}, depending on that V_{DS} voltage is absolutely 0 or not 0, you can say, you still have some noise even during this phase, when the output has saturated either to VDD or it has saturated either to ground.

When it is cut-off, that is a separate case, but when you have this in the off state with $V_{DS} = 0$, at that particular instant of time also or during that duration, you have some noise current through the transistor and that noise current you can think that during all this high time, it is getting filtered by the capacitor.

So, depending on this filter bandwidth, you will have residual noise at the capacitor. So, for example, if just you take one particular inverter from going from B to C. So, this is our B signal, depending on the noise current, your C signal will vary either this way or it can have this also or something like this also. Anything can happen, then ideally, we think that this voltage should be zero. But this voltage will not be zero because the NMOS transistor, it has $V_{GS} - V_{th} > 0$. There will be some current and if you look at the absolute value, it might be some fixed value.

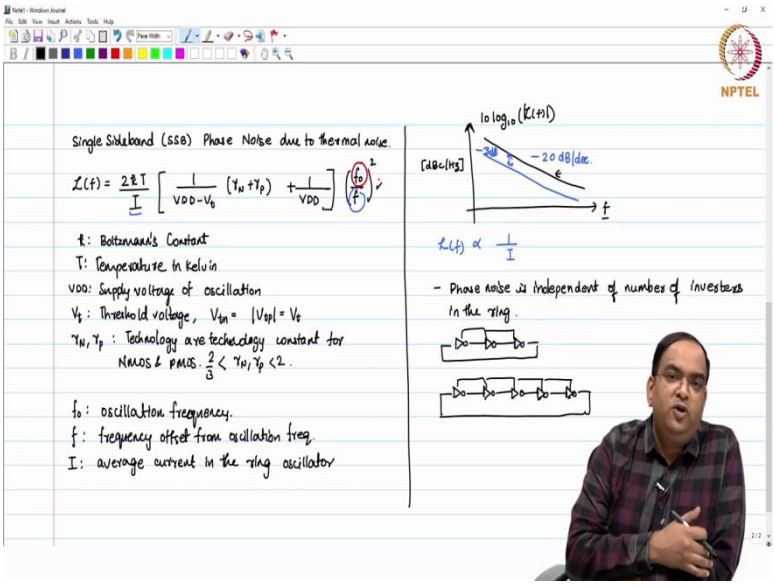
Then, in the next cycle, when your B goes from high to low, in that particular cycle, it depends on what was the previous value from which it starts ramping up. So, surely this transition will change but the absolute value of the voltage at node C will depend on the noise which is filtered on the capacitor during all-time high or all-time low mode.

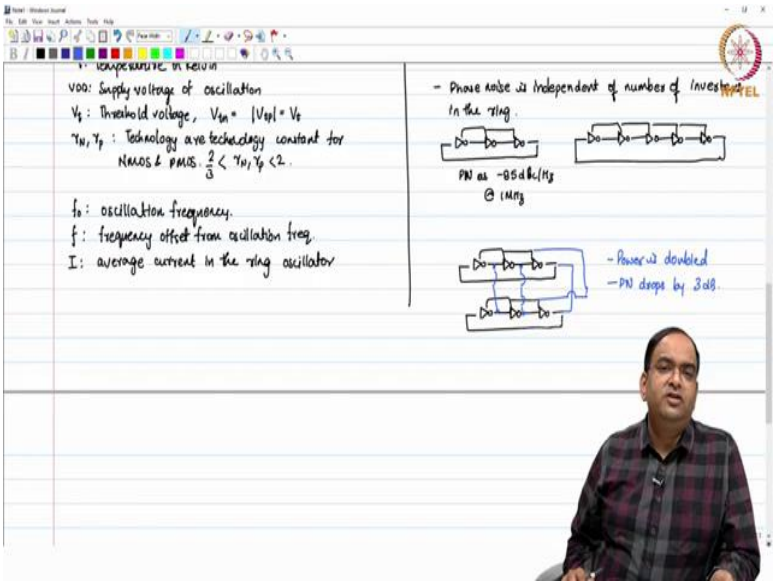
So, the noise is affecting in two ways. One, during the time of charging and discharging the capacitor at the inverter output, depending on the noise, your midpoint will change or your $\frac{VDD}{2}$ or transition point is going to change. The second thing is that when the input is held high or the input is held low, during that time the gate overdrive of both PMOS and NMOS transistor is greater than zero.

They will conduct some amount of current which is going to change the voltage at the output and this will affect the next transition cycle because the absolute value from where it starts changing from either 0 to VDD or VDD to 0, that will depend on the initial value and that initial

value depends on the noise which is filtered on the capacitor. So, these are the two noise sources which are present in the ring oscillator.

(Refer Slide Time: 10:57)





Now, after going through a lot of maths which we will skip for this discussion, after going through a lot of maths, you have the phase noise only due to thermal noise, so, let me just write it. Single sideband, we will use the formula which was derived earlier by other authors. So, we are seeing the single sideband phase noise only due to thermal noise for the ring oscillator. What is this thermal noise? Thermal noise for the MOSFET is like $\frac{8kT}{3g_m}$ which is a white noise which you have. So, the single sideband phase noise is given by,

$$L(f) = \frac{2kT}{I}\left[\frac{1}{VDD - V_t}(\gamma_N + \gamma_P) + \frac{1}{VDD}\right]\left(\frac{f_0}{f}\right)^2$$

So, let us try to make sense of each term here.

k: Boltzmann's constant
T: Temperature in Kelvin
VDD: Supply voltage of oscillation

In this particular derivation, we have used V_t as the threshold voltage for PMOS and NMOS both, so, let me just write it first and then differentiate between NMOS and PMOS.

V_t: Threshold voltage, $V_{tn} = |V_{tp}| = V_t$
where, V_{tn} is the threshold voltage of NMOS and V_{tp} is the threshold voltage of PMOS. The derivation is under this assumption.

γ_N, γ_P: Technology constant for PMOS and NMOS. Typically, $\frac{2}{3} < \gamma_N, \gamma_P < 2$. They take 2 for short-channel MOSFETs in general.

f_0: Oscillation frequency
f: Frequency offset from the oscillation frequency
I: Average current in the ring oscillator

So, whenever we talk about the phase noise, I have discussed earlier that phase noise, you can think about it as a power spectral density of the phase error for the oscillator. So, here if you think, if you look at it, your phase noise is directly proportional to ${f_0}^2$. By the way, this is noise, so, the units are in power. So, if you want, if you have this expression and you want to plot the phase noise in dBc/Hz, then you take this value and take 10 log of this particular expression, that will be the phase noise in dBc/Hz.

So, with respect to frequency, we always plot with respect to frequency offset here. So, do not think that this particular formula will apply when you have $f = 0$ also, no that will not apply, so, f is always slightly larger. This derivation is a simplification of the phase noise in ring oscillator. So, it is not like this will be the exact value which you will simulate and get it. It is simplification but it is a very good approximation of the phase noise in ring oscillator.

So, if I take $10\log_{10}$ of the phase noise expression which you are seeing on the left, that is normally plotted in dBc/Hz units and this may typically be something like this. So, here if I look at it, it is directly proportional to ${f_0}^2$ which means that if your output frequency increases, for the same jitter, you may think that the phase noise will actually increase.

If I double the output frequency, my phase noise will increase by 4 times and your phase noise in dBc, that will increase by 6 dBc. Then the other thing which you look at here is, it is inversely proportional to f and when we say inversely proportional to f, that is what you also see here that the phase noise keeps on decreasing, it is like -20 dB/dec due to the thermal noise.

The phase noise is also inversely proportional to, from this expression only, inversely proportional to current and inversely proportional to VDD. So, if I say that I have an oscillator where I am getting some amount of phase noise, if I double the current, if you increase the current to 2 times, then what will happen? The phase noise will come down by 3dB, doubling the current will reduce the phase noise by 3 dB.

Similarly, if you are able to double the power supply VDD without increasing the current, then also the phase noise will actually reduce. So, if you have the same oscillator operating at lower supply voltage and higher supply voltage with the same amount of current, you will have a lower phase noise for the higher supply voltage and if you think about it, the power consumption is also doubled.

So, to improve the phase noise, you have to spend more power. An interesting thing here is that the phase noise is independent of the number of inverters in the ring. So, what actually happens is that when you have more number of inverters in the ring, at that time, you have actually more stages to contribute to the noise.

But at the same time, this is something which we saw earlier also, at the same time, rising and falling of inverters, each transition time is actually also lesser if the oscillator is oscillating at the same frequency. So, we are talking about if you have a ring oscillator oscillating at same frequency whether with 3 inverters or you have with 5 inverters, let us say. So, 3 or 5 inverters, if the output frequency is same, if VDD is same, then what you will see is the one with the 5 inverters or 3 inverters, they both will have the same phase noise.

So, what we normally do is if we know the parameters which will help in increasing or reducing the phase noise, we can very easily do our system-level analysis. For example, we design an oscillator which gives me this phase noise in black and I do my system analysis. After doing my system analysis, I find that I have to reduce my phase noise.

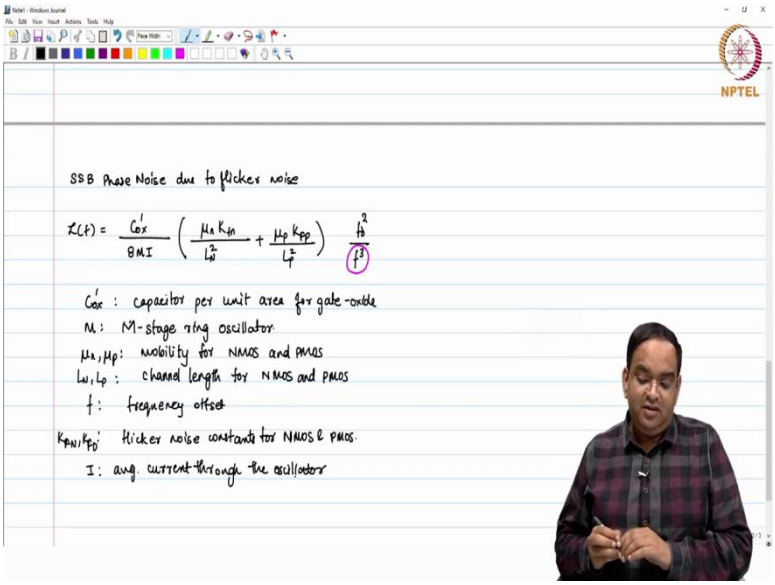
So, reducing the phase noise, looking at this expression, I know, if I want to reduce the phase noise, if I double the current, my phase noise will actually reduce by 3 dB. So, without going back to your circuit simulation, you can reduce your phase noise by 3 dB everywhere.

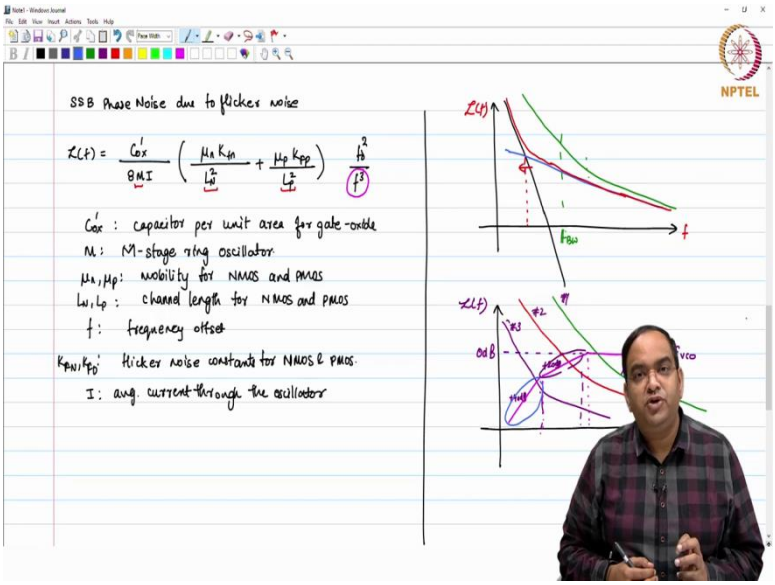
So, let us say, this particular oscillator has phase noise as -85 dBc/Hz at 1 MHz and I want to reduce the phase noise, what I can do is I can just take the copy of this oscillator and effectively in circuit also it will work pretty well. I just take the copy of this oscillator and make connections as I am going to show.

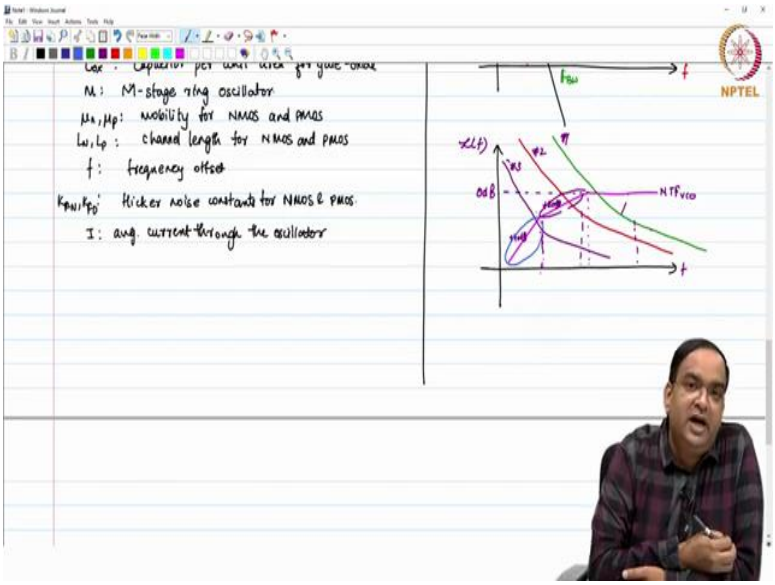
So, output is connected to output, supply is connected to supply and each node is connected. If you do this, what you are doing is you are doubling the size or doubling the power consumption. So, power is doubled and phase noise drops by 3 dB. So, this is something which you can always use.

Similarly, if you see that the oscillator which I have designed in circuit, for that my phase noise whichever I am getting, that particular phase noise is lesser than what I require, then I can reduce the power consumption if I do this scaling of 1:2, I half the sizes of the MOSFETs in the ring oscillator, power consumption will be halved, the oscillator will still oscillate at the same frequency and phase noise will increase by 3dB. So, you can use this formula for design.

(Refer Slide Time: 23:07)







Now, there is a flicker noise also. The one which we have seen is only with the white noise or thermal noise. You also have flicker noise for the MOSFETs and flicker noise is $\frac{1}{f}$ noise for each MOSFET. So, I will just write it, the single sideband phase noise due to flicker noise and both these noise sources are present.

So, it is not that only one is present, but the analysis for both of them is actually different because the way they affect the transition is different. So, this phase noise output due to flicker noise is given by,

$$L(f) = \frac{C_{ox}'}{8MI}\left(\frac{\mu_n K_{fn}}{L_N^2} + \frac{\mu_p K_{fp}}{L_P^2}\right)\frac{f_0^2}{f^3}$$

So, the first big difference between the thermal noise and the flicker noise is f^3. Previously the phase noise was reducing with respect to $\frac{1}{f^2}$, now, it reduces $\frac{1}{f^3}$. Let me define all the terms here. So, C'_{ox} is the capacitor per unit area, this is your gate oxide capacitor. So, capacitor per unit area for gate oxide, it is a M-inverter or M-stage ring oscillator, so there are M inverters in the ring.

So, you see that the phase noise due to flicker noise actually depends on the number of inverters in the ring, then μ_n and μ_p are the mobilities for NMOS and PMOS, L_N and L_P are the channel-length for NMOS and PMOS, f_0, you know is the output frequency, f is the frequency offset and K_{fn} and K_{fp} are the flicker noise constants for NMOS and PMOS, I is the average current through the oscillator.

So, what you see here is that if, see other than ${f_0}^2$, f^3, it is inversely proportional to the current. So, you increase the current and the output phase noise will reduce. So, if your flicker noise starts dominating, you should see which of the factors starts dominating and L_N and L_P, you can target them by increasing L_N and L_P both.

So, if you increase the length of the channel, the flicker noise drops. If you increase the number of stages in the ring oscillator while making the oscillator to oscillate at the same frequency for the same current, then also flicker noise is going to drop. So, when you plot the phase noise of the oscillator, you will see that it has both these components and if I draw them independently, maybe you will see the flicker noise components going like this and your thermal noise components may be going like this.

So, well, you will not see them independently, what you will see is something like this, finally it will be like this only. So, wherever your flicker noise corner is, flicker noise is equal to your thermal noise, you can call that as a flicker noise corner. So, depending on your PLL bandwidth, you would like to push this flicker noise corner to a lower frequency.

So, in one case, you can think that if my flicker noise corner happens to be quite large, that means I am having something kind of this. If the noise is some value like this, then you would see, if you keep your PLL bandwidth much smaller, let us say PLL bandwidth is much smaller, then you will not be able to suppress the noise properly.

So, let me just take two examples and show you why this flicker noise corner is important. So, here we know that the noise transfer function of the VCO is $\frac{1}{1+LG}$ which is actually a high pass

transfer function something like this. It is a second order which you see and then you have your flicker noise #1. So, #1 flicker noise I am going to choose, let us say, let us just pick up this curve itself, this is better.

So, in one case, I choose let us say something like this. And then in another case, I am choosing a value like this, you can have noise like this. So, it is #1, #2 and #3. So, this is the phase noise you have for the ring oscillator and the noise transfer function for the VCO is shown to you here.

Now, you can see that in the case #1, you have a lot of noise actually passed and the flicker noise corner appears to be somewhere here, for this case, here, for this case, it is here. So, suppression in case your flicker noise, so, this is like a 0 dB line for the noise transfer function.

So, when you have, by the way, this is going at the rate of +40 dB/dec, this goes at +20 dB/dec, but if you see for the phase noise in 1, you are passing the phase noise as such to the output. In the second case, you are suppressing the flicker noise by some amount using a lower value whereas in this case, you are suppressing the phase noise a lot with a much higher value. So, depending on where your flicker noise corner is with respect to your PLL bandwidth, you will have the suppression of the phase noise.

So, when you are designing a PLL, you can look at this, the phase noise of the oscillator at the or you can say the exact position of the flicker noise corner with respect to the PLL bandwidth, or with respect to the bandwidth for the noise transfer function of VCO.

Based on that, you can take a call whether you need to reduce the flicker noise or not. Reducing the flicker noise by increasing the length of the device is not coming without any trade-off because as soon as you increase the length of the device to make it oscillate at the same frequency, you also have to increase the width of the device to keep the same delay like $\frac{W}{L}$, same for the MOSFET.

If you increase width and length of the device both, then you are increasing the overall capacitance for the inverter and when you increase the overall capacitance for the inverter, you will increase the, for the same supply, you have to burn more current. So, that is the trade-off which you will see. These two formulae are quite good to understand the noise contribution of different transistors and which particular parameter we should target to reduce the phase noise. Thank you.