Phase-Locked Loops
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Lecture – 46
Supply Regulated VCO: Part III

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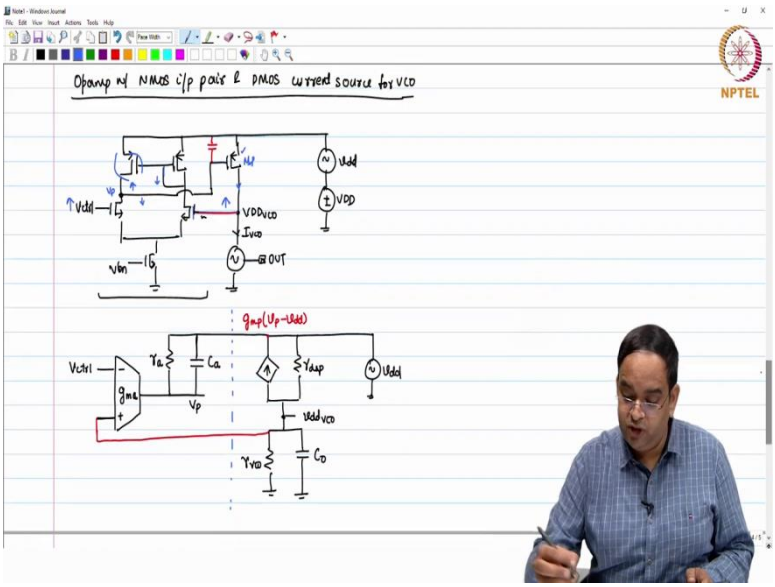

Hello, welcome to this session. So, given that we will use Opamp with NMOS input pair and PMOS current source for VCO, we have to analyze the supply noise rejection. Now, we will bring in the capacitors which are there in the opamp and see how the supply noise rejection depends on the frequency of the supply noise.

So, our amplifier is this and we know that each transistor comes with its own baggage of capacitors and other things. So, here we are going to use it like this. We will check whether our sign for the amplifier or the feedback is correct. So, this is our oscillator. This is V_{bn}, this is our V_{ctrl} and this, the voltage, there is no external voltage, but I am just calling this node as VDD_{VCO} and the average current here is I_{VCO}.

You have output of the oscillator as OUT like this. Here you have VDD and DC voltage and the noise on the supply, this is vdd. Now, just to cross check the sign, if I increase V_{ctrl}, because of this NMOS action, this particular node, I am calling this as V_p, the V_p voltage will drop and if V_p voltage drops, what happens is, there is another connection here which is this.

So, if V_p voltage drops, you push in more current through the PMOS transistor, I call this as M_p and your VDD_{VCO} goes up, if your VDD_{VCO} goes up, with this diode connection, this node potential will go down. If this node potential goes down, then because of the PMOS, you will push in the current and V_p will go up.

So, this is in negative feedback. Now, you have all the capacitors and other things for each transistor, what we are going to do is we are going to simplify the small signal model of this amplifier as shown. So, here I will say, the effective model of this amplifier, it behaves like a current source here which is g_{ma}, g_{ma} stands for the g_m for the amplifier.

This is your V_{ctrl}, this will be our feedback node and the effective resistance of the amplifier and effective capacitance, normally the capacitance at the gate of this PMOS transistor dominates. So, it is the C_{gs} of the PMOS transistor, so most of the time, this capacitor is dominant, but I am adding all those capacitors as effective capacitance C_a.

So, this is the model of the amplifier with this V_p and this particular node is the feedback node which you, which is this particular node which is this one. So, when you connect through the PMOS transistor, you have voltage controlled current source with resistor here which I call as r_{dsp} for the PMOS transistor and this current source as g_{mp} times, we have to write it specifically, I will just do that and the effective resistance of the VCO is r_{VCO}.

And normally, you will see that there is a load capacitor which comes at the supply of the VCO which is normally the dominant cap. So, I will write this as C_o. This node is vdd_{VCO}, we are looking at small signal analysis, so I will just write this as vdd_{VCO} and then you have the supply noise which is modelled like this, vdd here, this connects to the vdd_{VCO} here.

So, this is our feedback, this current source is $g_{mp}(v_p - vdd)$ because this is the source node. So, this is the small signal model of our supply regulated oscillator and if I just draw a dashed line, the left side is actually amplifier and the right side is your PMOS current source and the respective load from the oscillator.

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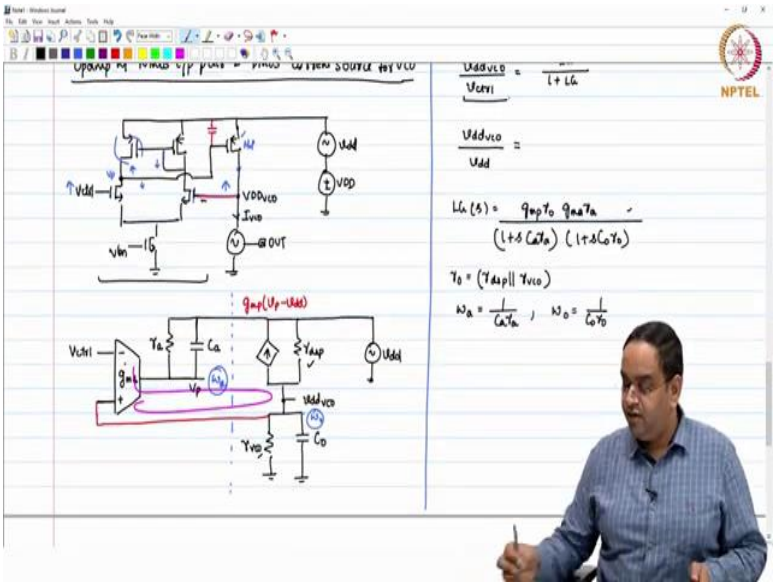

Now, given this, we have to look for two things. One, when we are going to use this supply regulated oscillator in the PLL loop, then the bandwidth from v_{ctrl} to vdd_{VCO}, this particular bandwidth should be larger than the PLL, the other transfer function or the way we want to find is how vdd from the supply noise comes at vdd_{VCO}.

So, that is something which we need to find. So, if I just look at this $\frac{vdd_{VCO}}{v_{ctrl}}$, what we will find here is that this is low pass transfer function with two poles dominantly and one pole is here, one pole is at the output of the opamp which you can say ω_a which is the dominant pole and the other is at the load which is ω_o. So, these two are the dominant poles which we have in general.

So, let us just look at both these transfer functions. So, let us look at the transfer function $\frac{vdd_{VCO}}{v_{ctrl}}$. To find this transfer function, one easy way is that you go and calculate the loop gain from v_{ctrl} and the loop gain from v_{ctrl}, you can find by looking at this loop gain and this loop gain happens to be equal to, this is loop gain for this regulator loop.

This is given by,

$$LG(s) = \frac{g_{mp} r_o g_{ma} r_a}{(1 + sC_a r_a)(1 + sC_o r_o)}$$

Here, we have,

$$r_o = \left(r_{dsp} || r_{VCO}\right)$$

Normally, we can also write,

$$\omega_a = \frac{1}{C_a r_a}$$

$$\omega_o = \frac{1}{C_o r_o}$$

So, you see a lot of DC gain. It depends on the DC gain of the amplifier and the DC gain of the PMOS stage.

So, the transfer function from v_{ctrl} to vdd_{VCO} is given by,

$$\frac{vdd_{VCO}}{v_{ctrl}} = \frac{LG}{1+LG}$$

This is a low pass transfer function and we need to make sure that the bandwidth of this low pass transfer function is larger than the PLL bandwidth.

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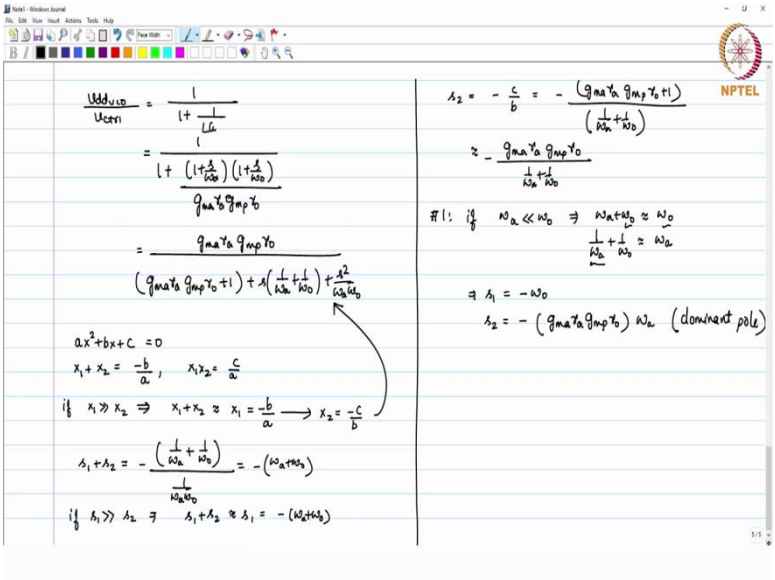

So, if you try to find this bandwidth, let us just look at it. So, we have,

$$\frac{vdd_{VCO}}{v_{ctrl}} = \frac{1}{1+\frac{1}{LG}}$$

$$\frac{vdd_{VCO}}{v_{ctrl}} = \frac{1}{1 + \frac{\left(1 + \frac{s}{\omega_a}\right)\left(1 + \frac{s}{\omega_o}\right)}{g_{ma} r_a g_{mp} r_o}}$$

So, you can just write it as follows:

$$\frac{vdd_{VCO}}{v_{ctrl}} = \frac{g_{ma} r_a g_{mp} r_o}{\left(g_{ma} r_a g_{mp} r_o + 1\right) + s\left(\frac{1}{\omega_a} + \frac{1}{\omega_o}\right) + \frac{s^2}{\omega_a \omega_o}}$$

So, this is the denominator. Now, you have two poles in open loop. In closed loop also, you are actually having two poles here. Now, well, you can decide which of these two poles is going to be dominant.

So, here quite often we use this approximation, if you have a quadratic equation as given below,

$$ax^2 + bx + c = 0$$

you know that we have the following relationship for the roots of this equation x_1 and x_2:

$$x_1 + x_2 = \frac{-b}{a}$$

$$x_1 x_2 = \frac{c}{a}$$

If I assume that $x_1 \gg x_2$, then I can say,

$$x_1 + x_2 \approx x_1 \approx \frac{-b}{a}$$

Then substituting this in the product equation, I can write,

$$x_2 \approx \frac{-c}{b}$$

So, among these two poles, if I am going to apply this concept here and I want to find two poles, then I can very well say there are two poles, s_1 and s_2, these two poles, and we have,

$$s_1 + s_2 = -\frac{\left(\frac{1}{\omega_a} + \frac{1}{\omega_o}\right)}{\frac{1}{\omega_a \omega_o}} = -(\omega_a + \omega_o)$$

If $s_1 \gg s_2$, we get,

$$s_1 + s_2 \approx s_1 \approx -(\omega_a + \omega_o)$$

So, effectively, you will get one pole at $(\omega_a + \omega_o)$. This is just an assumption here and by using this same logic, I will have,

$$s_2 = \frac{-c}{b} = -\frac{\left(g_{ma} r_a g_{mp} r_o + 1\right)}{\left(\frac{1}{\omega_a} + \frac{1}{\omega_o}\right)}$$

$$s_2 \approx -\frac{g_{ma} r_a g_{mp} r_o}{\frac{1}{\omega_a} + \frac{1}{\omega_o}}$$

So, this is our second pole. So, in closed loop, you are going to get two poles like this. Now, we can make two assumptions here. So, let us write the first assumption as follows:

#1: If $\omega_a \ll \omega_o$ which implies that $\omega_a + \omega_o \approx \omega_o$ and $\frac{1}{\omega_a} + \frac{1}{\omega_o} \approx \frac{1}{\omega_a}$. So, this is nothing but saying that $\omega_a + \omega_o$, the larger value is going to dominate, this is ω_o and in this case, because it is $\frac{1}{\omega_a} + \frac{1}{\omega_o}$, the smaller one is going to dominate. So, given this, our two poles which we are looking at are at are given as,

$$s_1 = -\omega_o$$

This is not dominant by the way and the other pole is s_2 which is given by,

$$s_2 = -\left(g_{ma} r_a g_{mp} r_o\right)\omega_a$$

This is the dominant pole as per our assumptions.

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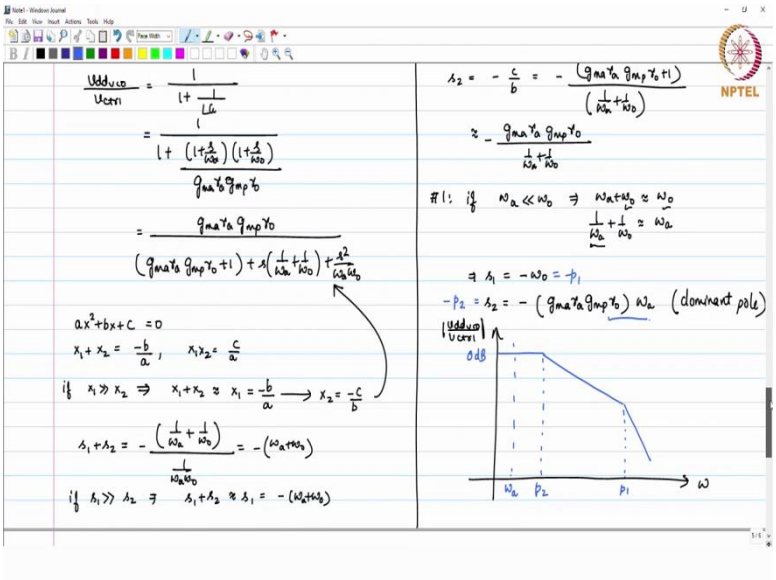

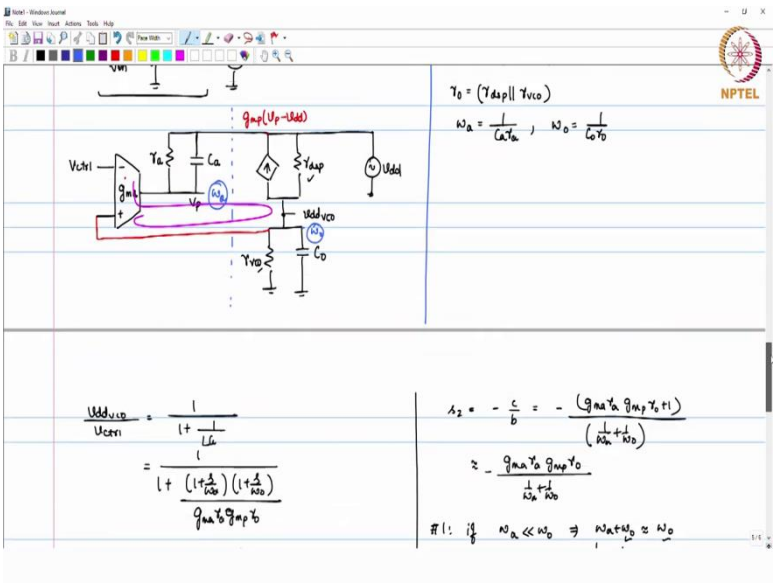

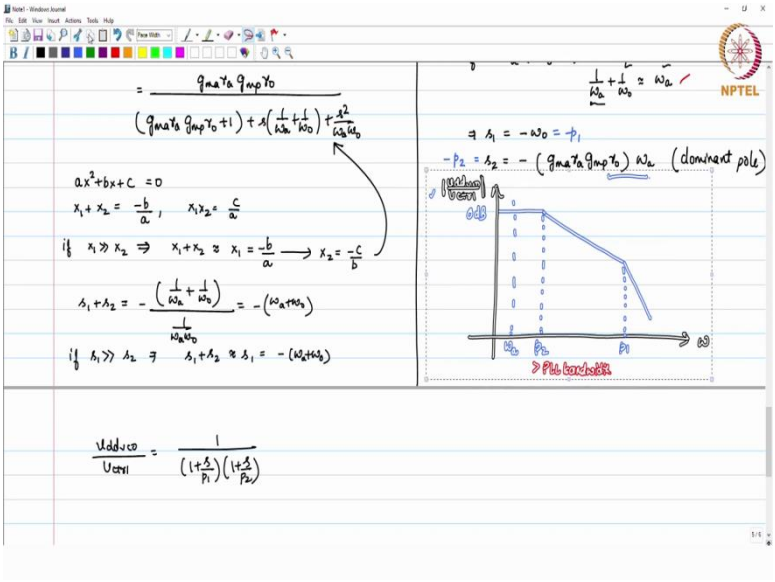

So, if you look at it, the transfer function $\frac{vdd_{VCO}}{v_{ctrl}}$, this transfer function, I am going to plot in dB. So, the DC gain is close to 1, by the way, $g_{ma}r_a g_{mp}r_o$ and all these things, the DC gain is close to 1, actually slightly lesser than 1, that is fine. So, this is like a 0 dB line and then you get first pole and if in your open loop case, your ω_a was the dominant pole, then in closed loop, your dominant pole is s_2.

So, I just write, let us say, $s_1 = -\omega_o = -p_1$ and $s_2 = -(g_{ma}r_a g_{mp}r_o)\omega_a = -p_2$. It is difficult to write this whole value, so, I will just write p_2 here. So, you get this p_2 and then after the p_2, you will have p_1 and then you have -40 dB/dec and your ω_a is much lesser.

So, when you are using this particular amplifier in feedback, your transfer function from v_{ctrl} to vdd_{VCO} is shown here and I can write the simplified expression $\frac{vdd_{VCO}}{v_{ctrl}}$ is given by,

$$\frac{vdd_{VCO}}{v_{ctrl}} = \frac{1}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}$$

where p_2 is the pole which dominates.

So, we should keep our p_2 larger than our PLL bandwidth, our regulator, this is the VCO regulator. So, the regulator bandwidth has to be larger than, this has to be larger than the PLL bandwidth. The things will just, your ω_a and ω_o will just exchange their roles if I say that ω_o is going to be dominant. So, in another case, I can say that everything else will remain the same.

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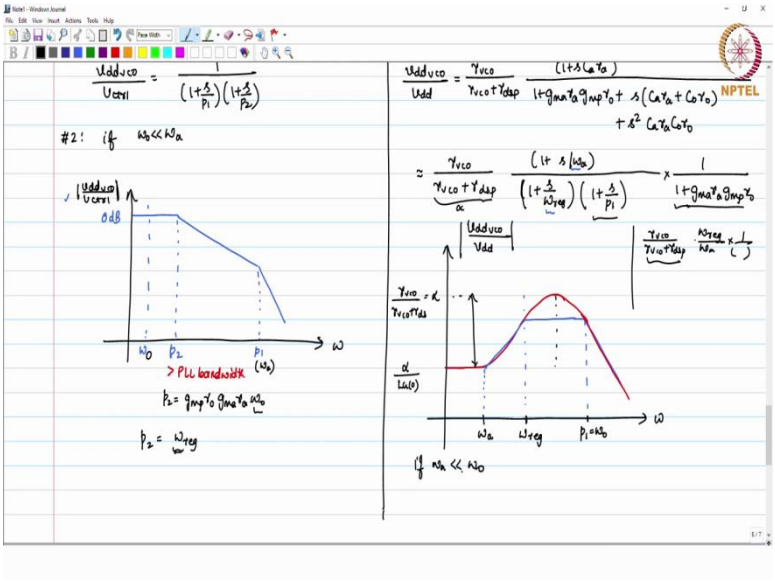

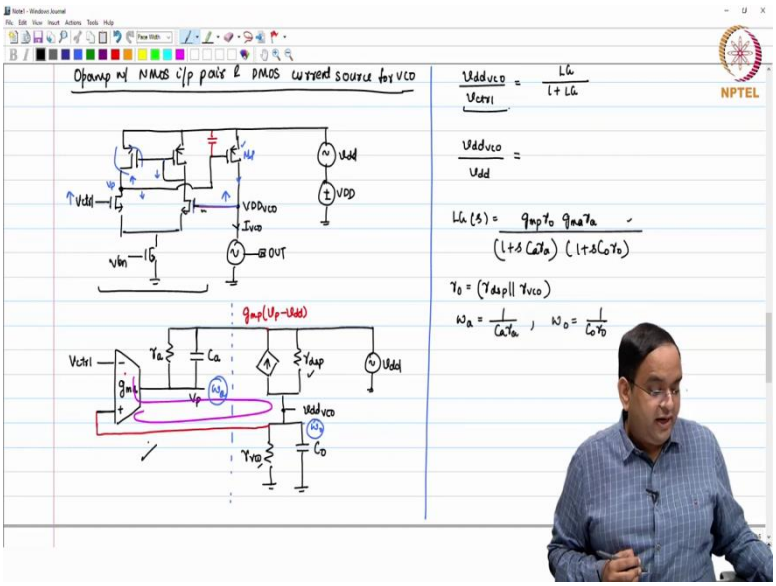

So, for case #2, If $\omega_o \ll \omega_a$, then these roles will just change. This is ω_o and this p_1 will be close to ω_a and $p_2 = g_{mp} r_o g_{ma} r_a \omega_o$. Everything else remains the same. In this case also, this has to be greater than the PLL bandwidth.

So, this is simple. Now, we just need to ensure that the regulator bandwidth is greater than the PLL loop bandwidth. Now, we have to look at the expression $\frac{vdd_{VCO}}{vdd}$. So, again you write KCL and KVL for this small signal circuit and when you are going to do that, you will find the transfer function. The transfer function is going to be,

$$\frac{vdd_{VCO}}{vdd} = \frac{r_{VCO}}{r_{VCO} + r_{dsp}} \frac{(1 + sC_aR_a)}{(g_{ma} r_a g_{mp} r_o + 1) + s(C_aR_a + C_oR_o) + s^2 C_aR_aC_oR_o}$$

This is your exact expression. Now, in this expression, I can simplify this expression. In both the cases, if you look at it, this p_2 pole whether it is DC gain times ω_a or it is DC gain times ω_o, this pole has to be greater than your PLL bandwidth and I can call this pole p_2 in both the cases ω_{reg}.

Approximately, it is either times ω_a or times ω_o, but this can be called as ω_{reg}. So now, I will just write this as,

$$\frac{vdd_{VCO}}{vdd} = \frac{r_{VCO}}{r_{VCO} + r_{dsp}} \frac{\left(1 + \frac{s}{\omega_a}\right)}{\left(1 + \frac{s}{\omega_{reg}}\right)\left(1 + \frac{s}{p_1}\right)} \frac{1}{g_{ma} r_a g_{mp} r_o}$$

So now, as we look at the transfer function, there are two cases which you will have. So, let us look at both the cases, and I am going to plot this transfer function, supply noise rejection to the control voltage of the VCO or vdd_{VCO}, this, with respect to ω. So, let us choose the first case where $\omega_a \ll \omega_o$.

So, if $\omega_a \ll \omega_o$, I will have ω_a as one frequency and $\omega_{reg} > \omega_a$ and p_1 pole which we have, p_1 is effectively ω_o. So, ω_o is coming at p_1 which is ω_o. These are the three frequencies which you have. So, the first one is if you look at it, ω_a is a zero. So, first you will get the zero frequency.

So, here you are going to see a zero frequency and then you are going to see the regulator frequency and then you are going to see p_1. So, the transfer function will effectively look something like this. The Bode plot will appear like this, a smoother curve will look something

like this. So, what you see here is that there is a DC value and then there is a lot of gain and this is something which is not desired but this is something which you will get it.

What is this value? So, if I call all of this term as let us say α and this is $\frac{1}{A_{DC}}$. So, what you are having is α times DC part of the loop gain. So, I can write this as $LG(0)$. And then, when the things peak, so what happens at the peak? Peaking frequency is slightly larger than your regulator frequency. And this is going to peak value of actually α itself which is $\frac{r_{VCO}}{r_{VCO}+r_{dsp}}$. How are you going to find out?

Well, if you see that the peaking is happening after ω_{reg} and before p_1, you can neglect this term. And what you are going to get here is the value as $\frac{r_{VCO}}{r_{VCO}+r_{dsp}} \frac{\omega_{reg}}{\omega_a} \frac{1}{DC\ Gain}$ and this is what you know is only $\frac{r_{VCO}}{r_{VCO}+r_{dsp}}$. So, this is the case when, all this analysis is if $\omega_a \ll \omega_o$.

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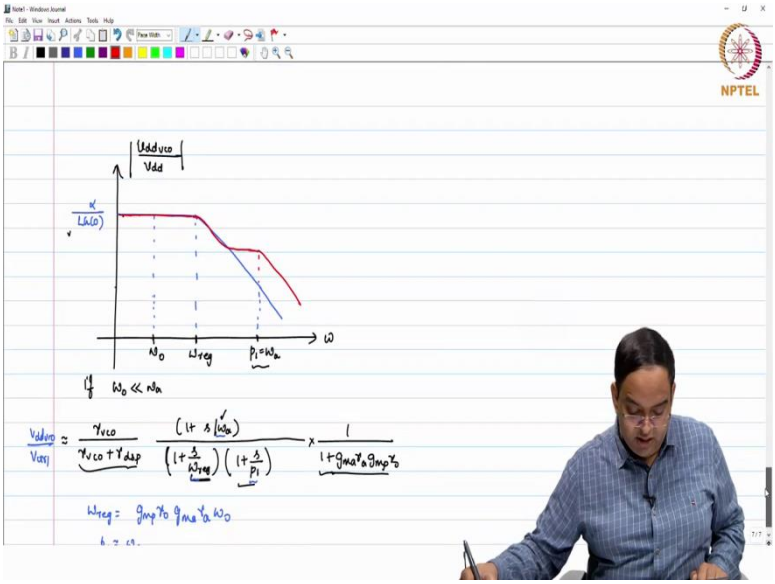

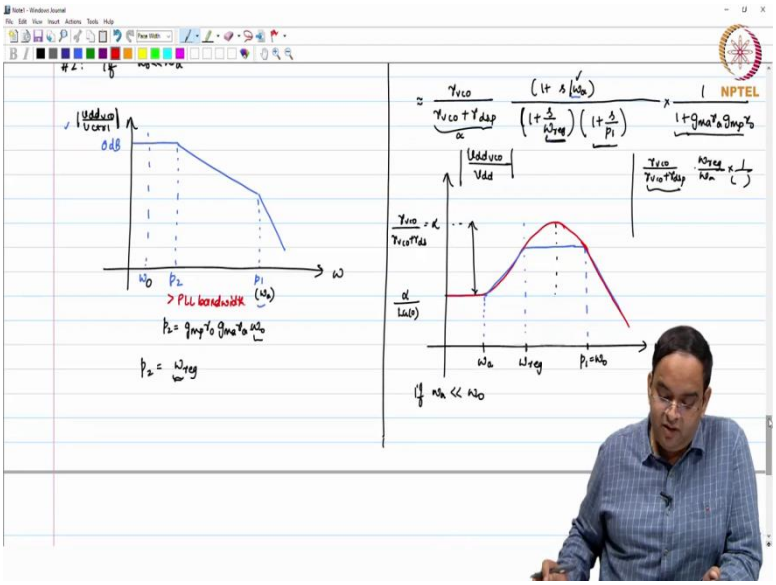

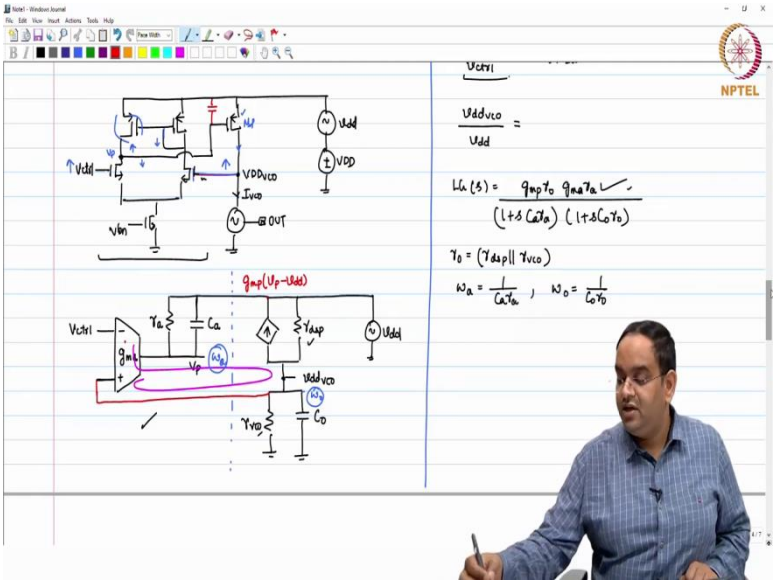

Then, you have another case where I am going to say that ω_o is the dominant one. $\omega_o \ll \omega_a$, so this is ω_o, this will be apparently be ω_a. So, in this case, if you go back and look at the expression, what do you have here? So, I will just draw it slightly, so, you get a zero, zero position does not change, zero is at ω_a.

So, you get a zero at ω_a but before that, you get regulator bandwidth. So, in closed loop, you get ω_{reg} pole first, zero and another pole later. And what was the p_1? If you look at it, p_1 will be ω_a. So, the transfer function which you are going to see is something like this. So, first you are going to see ω_{reg} and then you will have -20 dB/dec.

So, we have this transfer function which is $\frac{vdd_{VCO}}{v_{ctrl}}$ and if I say $\omega_o \ll \omega_a$, then our $\omega_{reg} = g_{mp} r_o g_{ma} r_a \omega_o$ and p_1 pole effectively, so, from our equation, your $p_1 \approx \omega_a$. That is an

approximation that p_1 is at ω_a. So, you will see some kind of, because you see a pole and a zero effectively.

So, you will see this kind of expression and what will be the DC value? Well, the DC value is going to be the same what we have checked earlier which is $LG(0)$. So, now, in this particular case, see the assumption is that your p_1 and your zero location, they are at the same but quite often you will see, because this is an approximation, you may see that you get transfer functions like, you may see zero little earlier and then you may see a pole.

So, you see two cases. In one case, your ω_o was dominant, in another case, your ω_a was dominant, depending on which pole is the dominant, you will see the supply noise rejection. What we need to make sure is that our PLL bandwidth, in this case, if you look at it, our PLL bandwidth has to be lesser than our regulator bandwidth, that is something which we should make sure.

The PLL bandwidth has to be lesser than the regulator bandwidth. Now, it depends whether that regulator bandwidth is dominated by the pole at the output of the amplifier or the pole at the output load. So, that is something when we design, we need to take care of that. Thank you.