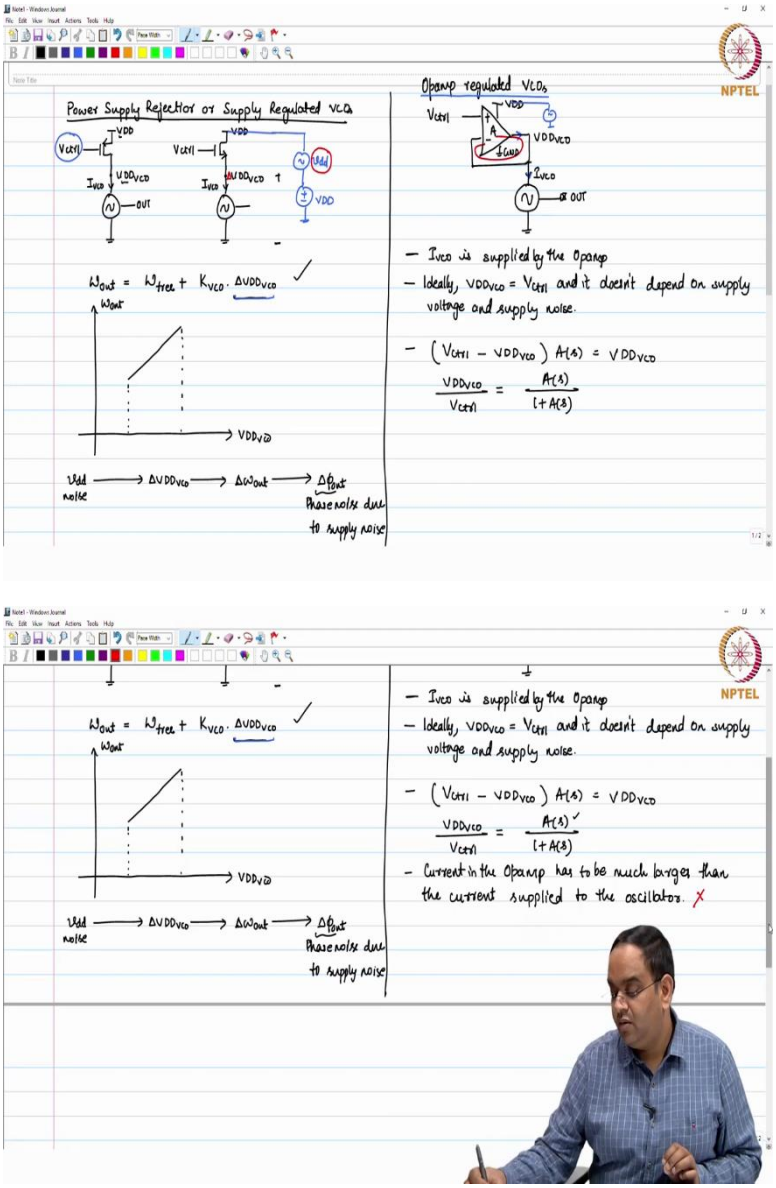
Phase-Locked Loops
Dr. Saurabh Saxena
Department of Electrical Engineering
Indian Institute of Technology Madras

Lecture – 45
Supply Regulated VCO: Part II

(Refer Slide Time: 0:15)



Hello everyone. Welcome to this session. In the previous session, we looked at the regulation of the oscillator using either PMOS or NMOS. So, all this comes under power supply rejection for the oscillator or you can call supply regulated VCO.

So, what we have seen so far is that we have an oscillator and the oscillator is controlled either by PMOS or by NMOS. So, I call this voltage as VDD_{VCO} and the current which is flowing

through the oscillator, the average current is I_{VCO}. You have a control voltage here and similarly, you have NMOS control where everything remains same, only in place of PMOS, you control with NMOS.

And what we have seen is that in the case of NMOS, you get better rejection for the supply noise because of the nature of this control, but you also saw that when you use NMOS, you have limited headroom for the oscillator. This VDD_{VCO} gets limited for a given supply voltage in case of NMOS as compared to PMOS and what we looked at is we only looked at when the supply noise was at DC. So, what did we do? We said you are applying a vdd noise on the top of the DC bias voltage, that is what we looked at.

Now, the thing is that you do not have a MOSFET without any capacitor. So, the capacitors will also come and based on that, you will have the supply frequency dependent supply noise rejection. This is applicable to both of these cases because you get limited in one case and you have poor supply noise rejection in the other case. So, there are other options which do exist to suppress the supply noise from VDD to VDD_{VCO} and later from VDD_{VCO} to OUT.

So, in all these cases, one important thing you can always make sure is that,

$$\omega_{out} = \omega_{free} + K_{VCO}.\Delta VDD_{VCO}$$

You can very well write it like this that there will be, it is not like your oscillator will keep on oscillating even if you reduce the voltage VDD_{VCO} to zero, that will not happen.

So, in some range, you will find the oscillator frequency to be linearly related to the change in the control voltage. So, I can write it like this, or if you look at it, this is VDD_{VCO}, then you can have, quite often you can have such kind of characteristics. And since we know that VDD_{VCO} is going to be a function of V_{ctrl}, you can define your K_{VCO} with respect to V_{ctrl} also. So, there is no problem with that.

So, when we are going to find the supply noise rejection to the output, what actually we are doing is we are finding this from the vdd, how my ΔVDD_{VCO} changes and when we know ΔVDD_{VCO}, then from, so, we can say from vdd noise to ΔVDD_{VCO} and from ΔVDD_{VCO}, using the K_{VCO}, we know $\Delta\omega_{out}$ and from $\Delta\omega_{out}$, you can very well find $\Delta\varphi_{out}$.

So, if this is noise, then whatever $\Delta\varphi_{out}$ you are getting is the phase you can say phase noise due to supply noise. So, what we would like to do is that we would like to look at other options

so that we can suppress the supply noise to the output. If we can suppress the supply noise from vdd to ΔVDD_{VCO}, then from VDD_{VCO} to φ_{out}, there is a very simple relationship given by this equation.

So, one of the options which you have to reject the supply noise is that the supply of the oscillator is controlled using an amplifier in this manner. So, the amplifier gives the current to the oscillator and the amplifier is connected in negative, this is negative, this is positive terminal of the amplifier, let us say the gain of the amplifier is A.

So, here you have V_{ctrl} and this voltage you call this as VDD_{VCO} and the current which is given is I_{VCO}, the output of the oscillator is this. So, we can say this is Opamp regulated VCO. Now, here, look at a couple of things that whatever current is going in the VCO, that current is coming out of the amplifier. So, the amplifier has to supply the current to the VCO. During the regular operation, I_{VCO} is supplied by the Opamp.

Now, well, Opamp will itself be connected to a supply voltage. So, you have VDD connected to the Opamp, VDD and ground. So, ideally VDD_{VCO} is equal to V_{ctrl} here and it does not depend on supply voltage or supply noise. Now, this is a very big statement and you can say that under ideal condition, this happens but under regular condition, this is not going to happen.

So, whatever supply noise you have at the amplifier, note if you have some supply noise here, that supply noise will get at the output but under this through this amplifier, so whatever you have, we cannot avoid it. But this is one of the, you can say, best ways to regulate the supply voltage of the supply of the oscillator because this negative feedback operation here is trying to fix the supply voltage of the oscillator. If you want to look at it, you can say that if the gain of the oscillator is A, then I can write,

$$(V_{ctrl} - VDD_{VCO})A(s) = VDD_{VCO}$$

This is just writing a simple equation, this is in Laplace domain.

So, I can write,

$$\frac{VDD_{VCO}}{V_{ctrl}} = \frac{A(s)}{1 + A(s)}$$

where, $A(s)$ is the transfer function of the Opamp in open loop. Now, if you are supplying a lot of current to the oscillator, then the current, current in the Opamp has to be much larger

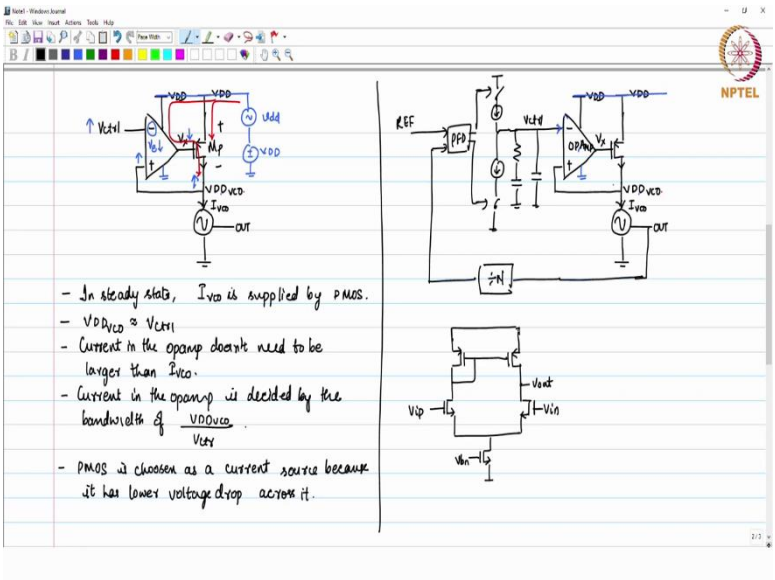
than the current supplied to the oscillator. Otherwise, you cannot approximate this Opamp because Opamp is also made up of MOSFETs, you cannot approximate the Opamp with a linear gain model as $A(s)$.

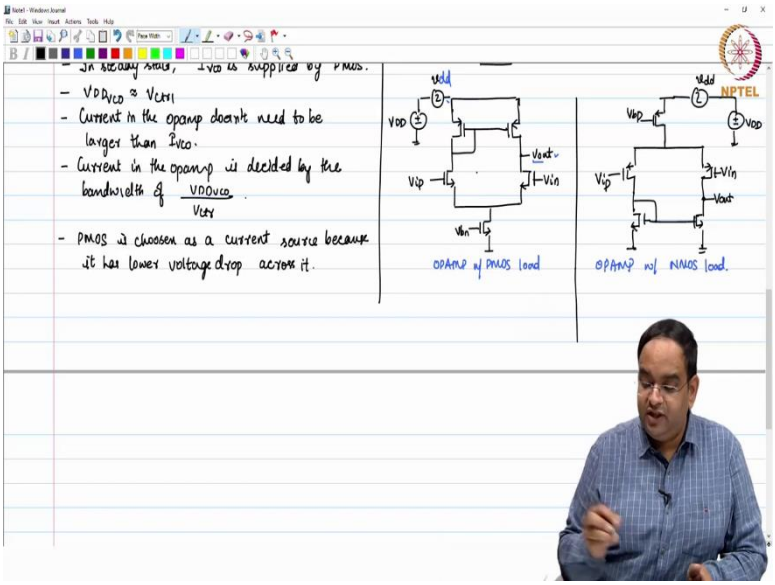
The Opamp has to be much larger than the current supplied to the oscillator. This is one of the problems in such kind of control, I have just marked it in red, because this is a problem in case of the Opamp regulation because then you may burn a lot of current in the Opamp just to supply the required maybe 4 or 5 x times I_{VCO} just to supply that I_{VCO} current and maintain a linear gain relationship between V_{ctrl} to VDD_{VCO}.

If you sacrifice any bandwidth in this transfer function $A(s)$, then this is going to limit your PLL loop bandwidth because think about it, this particular node is going to be connected to the loop filter output. So, the bandwidth from V_{ctrl} to VDD_{VCO} has to be first much larger than the bandwidth of the PLL loop and then because you want to supply this current, so, the current consumption in the Opamp has to be much larger than the current supplied to the VCO. So, this is one problem here but it gives you a really good supply noise rejection.

Now, because you have this problem, so, you will look for a solution and what that solution is, what we want to do is we want to regulate the current or the voltage of the oscillator using an Opamp, but at the same time, we do not want to supply the current of the oscillator through the amplifier.

(Refer Slide Time: 12:45)





So, in that case, we can come up with another circuit where we have the Opamp, we regulate the Opamp here using either NMOS or PMOS, both of them can be used. So, let us say, if you use PMOS and why do we use PMOS? Because PMOS offers a lower voltage, a lower potential drop. So, you have the Opamp connected to VDD, you have the PMOS connected to VDD and you have this V_{ctrl} here. So, let us try to understand this. So, you have VDD_{VCO}, current I_{VCO} and this is the output of the oscillator. So, what we have here is that if your V_{ctrl} increases, we need to check whether the signs of the amplifier are correct or not.

If V_{ctrl} increases, then your V_x will drop because you have a negative sign here. Your V_x drops, so, PMOS is going to push in more current at VDD_{VCO} node which will bring this up. So, as the positive sign goes up, the error between your positive and negative terminal drops. So, this is the correct sign for the amplifier.

So, here in steady state, you can say or when things have settled, in steady state, the average VCO current or I_{VCO}, whenever I am writing here as I_{VCO}, you can think that this is the average VCO current. The average VCO current is supplied by PMOS, M_p, you can write it like this and your VDD_{VCO} is roughly equal to, depending on the gain of the amplifier, is equal to V_{ctrl}.

Now, when you are connecting these two through a supply VDD because both of these blocks, they are connected to the supply voltage. So, this is VDD and you have vdd noise. So, this noise is going to affect the VDD_{VCO} in two ways. One, it will come, affect through this and other it is going to affect through this. So, there are two paths for the supply noise to appear at VDD_{VCO}. Whether it is good or bad, we can check that thing when we look at the amplifier circuit.

So, here the current in the Opamp does not need to be much larger or even to be larger than I_{VCO}. The current consumption in this Opamp is decided by the bandwidth of $\frac{VDD_{VCO}}{V_{ctrl}}$ because this bandwidth has to be larger than the PLL bandwidth because this whole block is going to come in the PLL.

So, let me just show you because it is a long time since we have seen the PLL block diagram. So, where will this block come? We can just take this block here and build our PLL around it. So, you have the supply here, this is fine. So, you will have the loop filter which is connected to the charge-pump like this and this is controlled by UP and DN pulses with the help of PFD. So, PFD drives this and the inputs of PFD are the reference clock and the feedback clock. The feedback clock is coming from the divider and the output of the VCO is connected like this. So, a charge-pump PLL with supply regulated VCO is shown here.

So, if you think about it, then this V_{ctrl} is going to the amplifier and if you design the Opamp using MOSFETs, then the DC current which is going inside the amplifier is zero. So, V_{ctrl} will not vary because of the Opamp. The Opamp may offer a capacitive loading to the loop filter but it will not offer any kind of DC resistance loading.

So now, given this is the common way of regulating the oscillator in a PLL, the other thing here is that PMOS is chosen as a current source because it has a lower voltage drop across it. And how does it help? Well, if you have a lower voltage drop across PMOS, then it means under a given supply voltage VDD, your VDD_{VCO} can actually be larger and you can have a larger output frequency.

So, that is what you do in place of NMOS. Though NMOS offers a better supply noise rejection but because of this, you prefer sometimes. Now, we want to see how this Opamp is going to suppress the noise. So, we need to know the internal structure of the Opamp. We will go with a very simple design of the amplifier. So, let me look at it.

So, here a simple Opamp, there are two options for this Opamp because we are looking at only simple amplifiers, we are not looking for any complicated ones. So, just remember we need to add transistors and we need not just because we have space and we connect transistors. So, this is a simple amplifier with NMOS input and PMOS as a load, it has differential input and so this is V_{bn}, you can say, this is V_{ip} and this is V_{in}.

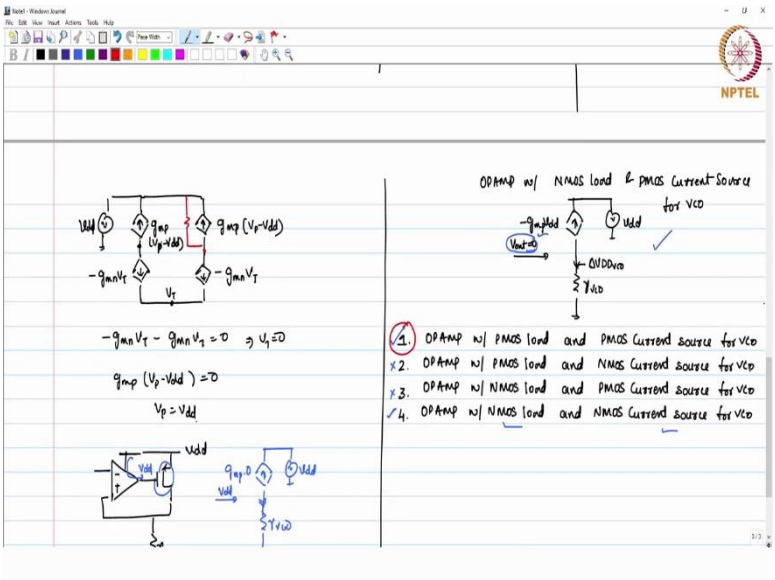
So, this is one amplifier, so, let me just call this like this, this is V_{out} for the amplifier. So, you have, it has a differential input and single-ended output. Similarly, you have an option, another amplifier where you have PMOS as a current source, V_{bp}, it is biased with V_{bp} and PMOS as the input pair and NMOS as a load.

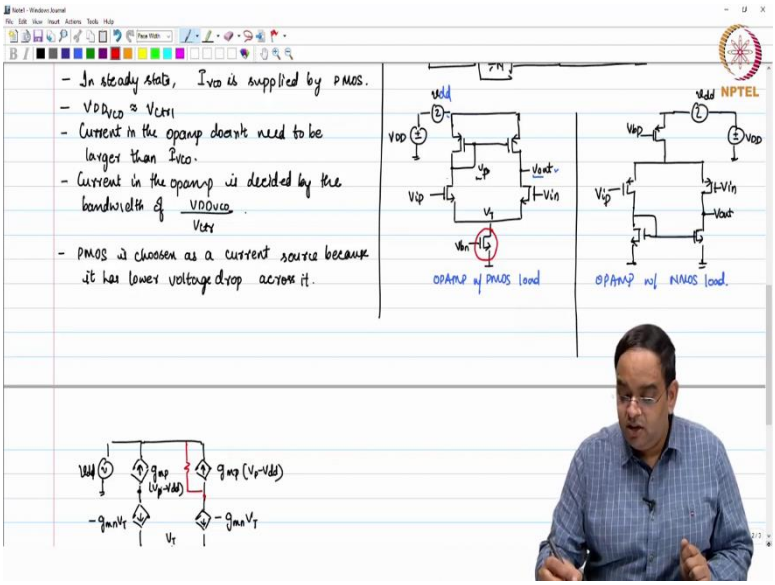
So, I can say this is V_{ip}, this is V_{in} and this is V_{out}. Now, in both these amplifiers, you have an option that you can design both these amplifiers with the same amount of current and so on, you may get the same bandwidth and other things. So, here I will just mimic the supply noise like small signal vdd with same supply noises, supply is here.

Similarly, I can have the small signal vdd supply noise and VDD. So, one thing which we are looking here is that when we design this amplifier, the gain and the bandwidth of both the amplifiers is the same. So, this amplifier is going to be connected to either PMOS or NMOS. So, as I told that I prefer PMOS here for the reason that I have a lower voltage drop across PMOS because of which I can increase VDD_{VCO} and I can operate at a higher frequency. So, now, if you have any supply noise at vdd, then what happens if you have supply noise at vdd? In the extreme case, you will find that V_{out} will also go to VDD.

So, let us call this as Opamp with PMOS load which it is and the other one is Opamp with NMOS load. Now, in both these cases, if you have noise vdd, any noise here for this Opamp, then that particular noise comes at the output. So, how are you going to find this? So, for the given amplifier, you can draw the small signal model for this amplifier.

(Refer Slide Time: 24:07)





So, small signal model of the amplifier will be simply further left and Opamp with PMOS load is going to be this. There is no input, you are only looking at, so, let me just do it this way. It is a more ideal block, I am just rejecting right now or not including the r_{ds}. Let us just look at this, so, this is what you have and you are applying supply noise here which is vdd, small signal vdd, this is your V-tail node.

So, I call this as V_T, you have here $-g_{mn}V_T$. This is also $-g_{mn}V_T$ and then this particular node if you call this as, this is V_{out}, let us call this as V_p. So, as per the PMOS, this is $g_{mp}(V_p - vdd)$, V_p is this voltage, vdd here you have and because the drain and gate both are shorted and this is also going to be $g_{mp}(V_p - vdd)$. So, you can have this.

Now, if you want, you can add the resistors, r_{ds} resistor for both PMOS and NMOS transistors and this will just become a little bit more complicated. So, what you are going to see here is, for this simple analysis, you will see that at V_T node, both the currents should be equal to zero, so we have,

$$-g_{mn}V_T - g_{mn}V_T = 0$$

$$V_T = 0$$

So, there is no current coming here which means that,

$$g_{mp}(V_p - vdd) = 0$$

$$V_p = vdd$$

Now, what you see here is that the gate voltage, this particular node voltage this will go to VDD and this node voltage will also go to VDD provided I take these resistors here, $V_p = vdd$ but we are not able to say anything about V_{out} and we can talk about V_{out} when we have this resistor, there is no current.

So, overall, the assumptions in this analysis we have made that the NMOS offers an infinite resistance, first thing, because supply noise will act as a common-mode noise here and then simplifying our analysis, you can do a detailed analysis, you will find that V_{out} will be close to VDD.

Now, when we club this particular amplifier with our PMOS, so, just think about it that you are using this amplifier with PMOS like this and you are having a supply noise in both the cases and you have effectively the VCO resistance r_{VCO} which we talked about in the last session.

So, through the amplifier, what you are going to get here is ideally vdd itself. So, when you have a PMOS and the source is at vdd, so, we are looking like this. So, here we are applying a supply noise which is vdd, the gate terminal of the PMOS transistor also somehow gets to vdd. So, $g_{mp}.0$, so, it will not ideally, it will not add any noise current to the oscillators. So, ideally it seems to be a good choice.

Practically, there will be some deviation and so you will see some noise leaks through. Similarly, if you look at the Opamp with NMOS load, when you have an Opamp with NMOS load, assuming that the effective resistance of the current source which you have, this current source resistance tends to infinity, then no noise comes to the resistor, no supply noise comes through the current source and if no noise comes through the current source and you are looking at the equivalent model of the PMOS load, then what you will see here is the gate voltage which is V_{out} here, the gate voltage is actually at 0, it does not change because of the supply noise and you have here vdd noise like this and then you have the resistor r_{VCO}.

So, the current which you are going to see is $g_{mp}vdd$. So, this noise current flows through the oscillator resistance, equivalent resistance for the oscillator and you will have ΔVDD_{VCO}. So, for Opamp with NMOS load, you have supply noise with NMOS load and PMOS current source for VCO. You have supply noise which leaks through the current source and it does not get rejected effectively.

So, there are options which you would like to use. So, if I just list it, there are four options. We are using Opamp with PMOS load and PMOS current source for VCO. So, this is something which we see that it works better because you reject the DC supply noise coming to the gate of the current source. So, this is one option which is actually preferred, but you have all possibilities that you can have, so, I will just list all of them.

So, with PMOS load and NMOS current source and then I will have here with NMOS load and NMOS current source. So, this is the one which works good because you have PMOS load and PMOS current source, the way why it works better, we have looked at it. With PMOS load and NMOS current source, if you have PMOS load and NMOS current source, then you will have the supply noise coming to the gate of the PMOS and it will get actually added to the VDD_{VCO}.

So, this is not a good option. Then Opamp with NMOS load which is this amplifier and PMOS current source, analysis is shown here, it is not good because you have the supply noise is not coming at the gate and the source connected to vdd.

Opamp with NMOS load and NMOS current source, this is good because when you have NMOS load, the gate of the NMOS current source will not have the supply noise and the NMOS current source offers like an ideal current source there. So, it will not allow the noise from vdd to come at the output. So, these two options are better options and this is chosen here for the fact that we get a lower headroom for the current source for the oscillator and we can have a larger frequency of oscillation.

Sometimes you choose this also, but in that case the highest frequency will be limited but you will have a better supply noise rejection. So, next we will see how to analyze this supply noise coming at the output. Thank you.