Phase-Locked Loops
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Lecture – 44
Supply Regulated VCO: Part I

Hello everyone. Welcome to this session. So, by now, we have studied single-ended ring oscillator, pseudo-differential ring oscillator which gives you phases, I, Q phases. And both these oscillators, their frequency can be controlled. So, by changing their supply voltage, we have seen previously that by controlling the current of the oscillator or designing the inverter as a current starved inverter, you can control their output frequency. Now, we are going to deal with this frequency control in a little bit more detail.

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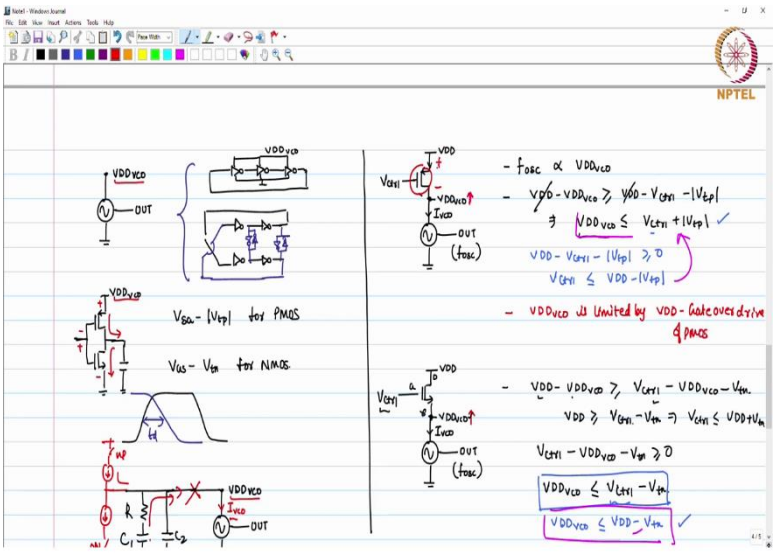

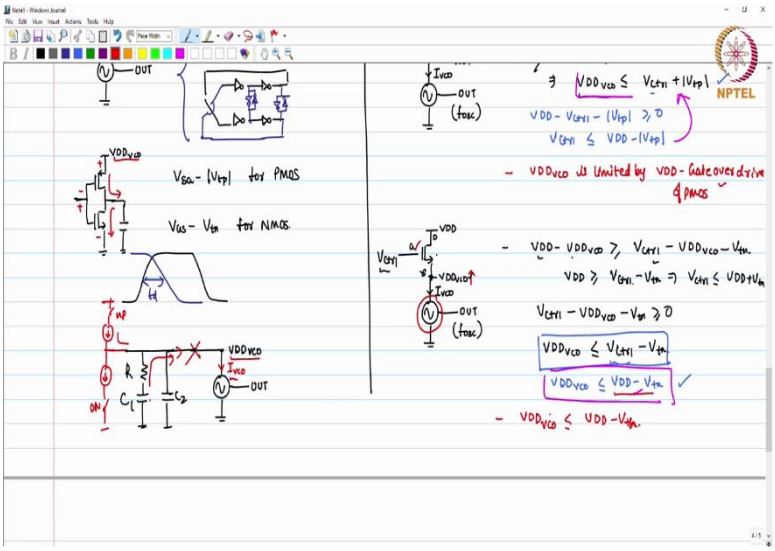

So, just as an example, I am going to just draw a symbol for the VCO which is like this and here this supply is VDD_{VCO}. Now, whether you control VDD_{VCO} using current source or voltage source, that is your choice and this is your output, any one of the nodes of the oscillator can be chosen as an output. If you want multiple phases, you will take multiple phases in output. This oscillator can be a simple inverter, three inverters in the ring which is odd number of inverters or you can have pseudo-differential ring oscillator also. So, this is just to tell you that the oscillator can be any of these blocks.

Now, well, you need to have cross-coupled inverter here, you connect it. So, these are the two oscillators which we are considering. Now, the supply of these two oscillators which is VDD_{VCO}, this is VDD_{VCO} and similarly, you have VDD_{VCO} for the bottom oscillator. Now, what we want to do is we want to control the frequency of the oscillator by controlling VDD_{VCO} because we know that when you have an inverter connected to the, you designed an inverter and you have this voltage as VDD_{VCO}, by the way the parasitic capacitance which you are going to have, that is fixed.

So, the charge and the discharge rate, charging rate through PMOS and discharging rate through NMOS depends on the gate overdrive for PMOS and similarly gate overdrive for NMOS. Now, gate overdrive for PMOS and gate overdrive for NMOS, that depends on the supply voltage. When I say gate overdrive, gate overdrive means the following:

$$V_{SG} - |V_{tp}| \text{ for PMOS}$$

$$V_{GS} - V_{tn} \text{ for NMOS}$$

So, this is valid that if you vary the supply of the inverter, you are going to vary the delay of the inverter, and what delay are we talking about? We are talking about midpoint to midpoint zero crossing point, midpoint-midpoint zero crossing.

So, if I give this input and the output, this is the delay which we are talking about. So, what happens is that in order to vary or we know that if we vary VDD_{VCO}, we can control the frequency of the oscillator. Now, if this particular oscillator is used in the PLL with the loop filter, then what you have is the loop filter is something like this, R C_1 C_2 and this normally we used V_{ctrl} voltage to control the frequency of the oscillator if you recall the PLL block. Well, one way you can say is that if that is the case, I can very well go and connect the oscillator to this so that I can vary the frequency.

But this is not feasible because oscillator draws a certain amount of current and if I take that DC current out from the loop filter, then I am discharging the control voltage of the loop filter because the charge-pump which connects to the loop filter, this particular charge-pump gives the current to the loop filter once in a reference cycle.

So, whenever you get UP and DN pulses which control these switches, they are turned off, there is no current coming from the charge-pump and the current required by the VCO will be taken from the capacitor. So, your control voltage will keep on changing a lot and your frequency will vary. So, this is not the solution.

So, one way to supply the current to the oscillator without discharging the loop filter is the following. We have seen this thing previously also. So, we can have a current source, you can have a PMOS control current source like this, this is VDD and we hope that this voltage will be VDD_{VCO} such that I get I_{VCO} current for a given output at frequency f_{osc} and this voltage is V_{ctrl} and this V_{ctrl} can be connected to the loop filter. So, in this case, if you look at it, our VDD_{VCO}, so, the first thing we should understand that $f_{osc} \propto VDD_{VCO}$.

In order that this PMOS acts as a current source when it operates in saturation region. So, the condition for the saturation region is that,

$$VDD - VDD_{VCO} \geq VDD - V_{ctrl} - |V_{tp}|$$

$$VDD_{VCO} \leq V_{ctrl} + |V_{tp}|$$

So, because your output supply voltage is, this particular supply voltage is less than equal to $V_{ctrl} + |V_{tp}|$, you will have the limit on the frequency. Well, that is what you have. So, this is one way of controlling the oscillator and supplying the current required for the oscillator.

Similarly, you can control the current through the oscillator by using an NMOS. So, in place of PMOS, let us say, if I use NMOS. So, this is V_{ctrl}. I will choose my V_{ctrl} in such a way that I get the desired VDD_{VCO} and I_{VCO}, that I will have. Now, here the thing is that this NMOS, if NMOS operates as a current source, it should operate in saturation region which means that,

$$VDD - VDD_{VCO} \geq V_{ctrl} - VDD_{VCO} - V_{tn}$$

So, here the only thing which we may need to make sure is that,

$$VDD \geq V_{ctrl} - V_{tn}$$

This is one condition. The problem here is if you try to increase your VDD_{VCO}, then what you will see is that your $V_{GS} - V_{th}$ for the NMOS transistor will be 0. So, what we need is,

$$V_{ctrl} - VDD_{VCO} - V_{tn} \geq 0$$

$$VDD_{VCO} \leq V_{ctrl} - V_{tn}$$

You know from here that V_{ctrl} is to keep the transistor in saturation region, and we have,

$$V_{ctrl} \leq VDD + V_{tn}$$

So, you can plug that in that V_{ctrl} is $VDD + V_{tn}$ but think about it, you are using this transistor for a given supply voltage. So, V_{ctrl} will automatically be limited by VDD, you cannot have V_{ctrl} larger than VDD. If V_{ctrl} is not larger than VDD, then we have,

$$VDD_{VCO} \leq VDD - V_{tn}$$

You compare these two conditions that in one case, your VDD_{VCO}, here also the same relationship will be there for V_{ctrl}. What is that? So, we have,

$$VDD - V_{ctrl} - |V_{tp}| \geq 0$$

$$V_{ctrl} \leq VDD - |V_{tp}|$$

Here, V_{ctrl} can go to 0 by the way, because it is a PMOS. So, what we see in this particular case is that here VDD_{VCO} is limited by $V_{ctrl} - V_{tn}$ or $VDD - V_{tn}$. In the previous case, your

VDD_{VCO} is limited by again VDD. So, if you substitute this here, then you will see that VDD_{VCO} at max can go to VDD but depending on VDD_{VCO}, I push this to VDD and what will happen is this transistor will appear into linear region. So, for PMOS, it is the case if you keep on reducing the overdrive, then your VDD_{VCO} can keep on increasing, but in that case, the size of this transistor will be very large. So, practically that is not possible. In case of NMOS, what you see here is that you have an upper limit $VDD - V_{tn}$ which is a problem.

So, in this case, VDD_{VCO} is limited by the headroom which you want for the PMOS transistor and this headroom you can say is effectively the gate overdrive of the PMOS transistor, gate overdrive $V_{GS} - V_{th}$. So, this can be, depending on which process you are using, this can be 100, 200 or 300 mV whichever you want. So, if we want to increase the VCO frequency, we want to maximize this, but there is an upper limit that we have to maintain V_{DS} equal to overdrive of the PMOS transistor. So, VDD_{VCO} is limited by VDD minus gate overdrive of PMOS. In the second case, your VDD_{VCO} is actually limited. There is an upper limit, VDD_{VCO} is limited by $VDD - V_{th}$. I am using V_{tn} for the threshold voltage of NMOS transistor, normally, threshold voltage of NMOS transistor is larger than the gate overdrive which you can use for biasing PMOS because gate overdrive is in your control. So, if you keep gate overdrive as 100 mV, you can do that while you are having a threshold voltage of 300 or 400 mV. So, normally, the headroom for the VCO in case of NMOS control is smaller than in the case of PMOS control. So, if you want to have a higher frequency, then this is the preferred choice. So, if this is the preferred choice, why am I discussing both of them?

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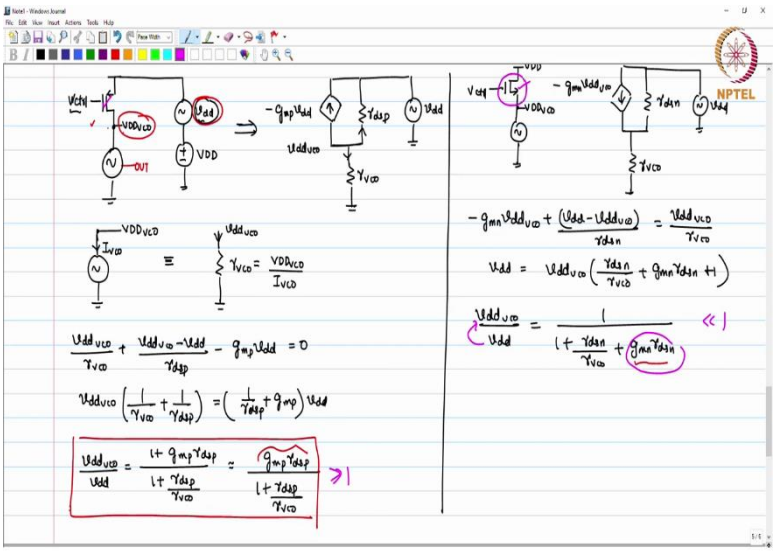

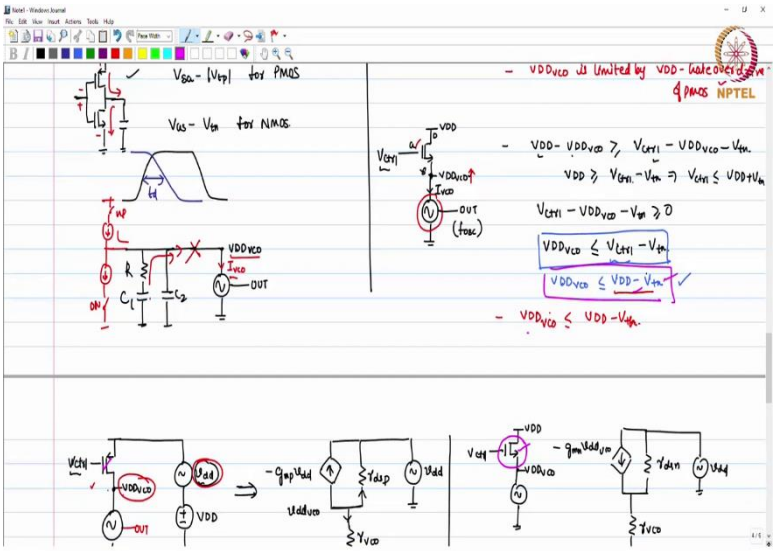

Well, the reason is that one of the other performance metrics of the oscillator which we have not discussed so far for this case is power supply rejection. So, if you take both the cases, the one which you have with respect to PMOS and try to find out how the supply noise is going to affect the oscillator. This is the oscillator and I have this, I am just calling this node as VDD_{VCO}, there is no specific voltage source connected, do not get mistaken by that. So, this is V_{ctrl} and I have the supply voltage. So, let us say I am modeling the supply voltage with some noise vdd and whatever VDD you need.

In order to find out how the supply noise is going to affect my VCO frequency or the phase noise later, I can find out how the supply noise affects my VDD_{VCO} and because this is noise, I can use, noise which is small in magnitude, I can use small signal model of this circuit. So, to begin with, I am going to model my VCO which has an operating point, it is just an example, it has a voltage VDD_{VCO}, it has the current I_{VCO}. So, I can effectively model this with a resistance, this is just a modeling where $r_{VCO} = \frac{VDD_{VCO}}{I_{VCO}}$, this is just for modeling purpose.

I will call this node as vdd_{VCO}, small signal voltage. For PMOS transistor, we all know, so, using this circuit for the small signal modeling, I will have $-g_{mp}vdd$ because you are not looking at the change in the output frequency with respect to the control voltage, you are looking at the change in the output frequency or the supply of the oscillator with respect to the supply voltage.

So, you are going to have r_{dsp}, the resistance of the PMOS transistor modeled by resistance of the voltage controlled oscillator. This is only to calculate the DC gain. I have neglected the

capacitors right now, we can take that into account while making the system more complicated sometime later. So, this is vdd, this node as I said is vdd_{VCO}.

So, using this, I need to find out $\frac{vdd_{VCO}}{vdd}$. This will tell us how the supply noise is going to change the vdd_{VCO} and we know if you change vdd_{VCO}, your frequency of the oscillator will change, from our analysis for the delay part. So, if we find this, this will help us to find the supply noise rejection. So, in order to find this, I will solve the circuit as shown, small signal circuit.

So, we get,

$$\frac{vdd_{VCO}}{r_{VCO}} + \frac{vdd_{VCO} - vdd}{r_{dsp}} - g_{mp}vdd = 0$$

So, well, you can take all the terms on one side, so, we have,

$$vdd_{VCO}\left(\frac{1}{r_{VCO}} + \frac{1}{r_{dsp}}\right) = \left(\frac{1}{r_{dsp}} + g_{mp}\right) vdd$$

So, this parameter which you are seeing here, I can just write it directly now. This is equal to,

$$\frac{vdd_{VCO}}{vdd} = \frac{1 + g_{mp}r_{dsp}}{1 + \frac{r_{dsp}}{r_{VCO}}}$$

So, we get,

$$\frac{vdd_{VCO}}{vdd} \approx \frac{g_{mp}r_{dsp}}{1 + \frac{r_{dsp}}{r_{VCO}}}$$

If $g_{mp}r_{dsp}$ which is the gain of this transistor is quite large, you can write it like this. If $g_{mp}r_{dsp}$ is quite large, then you see that $\frac{vdd_{VCO}}{vdd}$ becomes quite large.

So, depending on what is your g_{mp} and all, you will get your supply noise which is vdd is passed to vdd_{VCO}. We have to compare this thing with our NMOS case. So, what happens in case of NMOS? You have this and then your VCO, using the small signal model for the NMOS and your VCO, we can write it like this or draw it in this manner.

You have r_{dsn} and you have this as r_{VCO}, this is $-g_{mn}vdd_{VCO}$. And you are applying the supply noise here, small signal. So, we have,

$$-g_{mn}vdd_{VCO} + \frac{(vdd - vdd_{VCO})}{r_{dsn}} = \frac{vdd_{VCO}}{r_{VCO}}$$

You take the terms on one side, so what you will get here is,

$$vdd = vdd_{VCO}\left(\frac{r_{dsn}}{r_{VCO}} + g_{mn}r_{dsn} + 1\right)$$

So, we get,

$$\frac{vdd_{VCO}}{vdd} = \frac{1}{1 + \frac{r_{dsn}}{r_{VCO}} + g_{mn}r_{dsn}}$$

$g_{mn}r_{dsn}$ is the gain of the transistor similar to what you have $g_{mp}r_{dsp}$. So, if you compare the two cases, what you will see is the large part of the gain which is your $g_{mn}r_{dsn}$, in one case it is coming in the numerator and in the other case, it is coming in the denominator.

So, wherever you have in the denominator, that will help us to suppress the supply noise coming to the vdd_{VCO}. So, surely it depends on the exact value, but $\frac{vdd_{VCO}}{vdd} = \frac{1}{1+\frac{r_{dsn}}{r_{VCO}}+g_{mn}r_{dsn}} \ll 1$ whereas $\frac{vdd_{VCO}}{vdd} \approx \frac{g_{mp}r_{dsp}}{1+\frac{r_{dsp}}{r_{VCO}}} > 1$, can be $\gg 1$ if required or if designed that way.

So, you will have a lot of DC gain when you use PMOS as compared to NMOS. So, if you want to suppress the supply noise to the oscillator supply, you would prefer to use NMOS but you run into the problem of upper limit on the frequency. So, based on your requirements, you have to trade-off one way with the other. Either you can have the highest frequency in a given process or you can have a better supply noise rejection, at least for these two matters. We will see other matters in the next session. Thank you.