## Phase-Locked Loops Dr. Saurabh Saxena Department of Electrical Engineering Indian Institute of Technology Madras

## Lecture – 43 Large-Swing Ring Oscillator: Part V

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| No. 75  | NPTEL  |
| Single-Ended Ring Oscillator                                |        |
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Hello everyone. Welcome to this session. In the previous sessions, we have seen oscillators which were single-ended or to just clarify, we have seen oscillators with inverters connected, odd number of inverters connected in a chain, in a ring like this. So, we can very well say this is single-ended ring oscillator. This is what we have seen and we have been studying this, how to control their frequency, how to control their amplitude and so on.

Now, this same oscillator if you look at it, when it oscillates, the waveform which you are going to see at the nodes A, B and C and the other node is same as A, the waveforms which you will see at A and B will be something like this, they can be sinusoid also, close to sinusoid if the frequency is quite high.

So, this is the waveform A, the waveform B happens to be like this, this is waveform B and waveform C is going to be something like this. There is an important thing to understand between these waveforms. If you look at the rising edge on A and rising edge on B, these two rising edges are separated by phase, this phase is equal to actually  $240^{\circ}$ . So, this is  $240^{\circ}$ .

The rising edge on A and the rising edge on C, this is separated by  $120^{\circ}$ . If you want to look at between the rising edge on A and the falling edge on B, then that is separated by  $60^{\circ}$ . So, you

see the phase separation between the clock edges which are generated by using these odd number of inverters in the ring, they are like 120°, 240° and so on.

So, I can very well say that the phase difference here in this case is given by,

$$\Delta \varphi = k. \frac{360^{\circ}}{3}$$

So, if you are going to use odd number of inverters, depending on how many inverters you are choosing, you will have the phase difference between the rising edges as,

$$\Delta \varphi = k. \frac{360^{\circ}}{m}$$

where, m is the number of inverters which you are going to use.

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| Single-Ended Ring Oscillator       | FA. B. E. P. F      |
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| 1, 0, 1, 0                         |                     |
| 12 - Do - Do - Do - 10 Oscillation |                     |



Now, why is it a problem? Well, as such this is not a problem at all, but sometimes what you need is you do not need this phase of 120°, but you need phases like 90°, 270°. So, quite often you need clock with phases 0°, 90°, 180° and 270°. These are by the way called as quadrature clocks where I can say I, Q,  $\overline{I}$  and  $\overline{Q}$  and ring oscillators give you an opportunity to generate such kind of phases. But there is one thing which we have seen earlier that if we employ even number of inverters in the ring, then we know that there will be no oscillations.

So, if I just look at the formula here, I would say that if I choose m = 4, then I will get 90° as desired, but when I go and connect this m = 4, there are no oscillations at all and this is something which we have seen, you cannot have oscillations, it is going to saturate to values *VDD* and ground for this case.

So, what we can do is the following. In place of having this even number of inverters in the ring, what we do is we still keep even number of inverters like this and somehow we try to enforce that there is a phase difference between the input and the output of this chain. So, let me just call this as A, B, C, D.

So, what I am trying to say let me just first draw it. You have the same inverter, so in the case of odd number of inverters, what you saw that when you feed a rising edge of the clock here, in response to this rising edge, you are going to have falling edge, then again rising edge and then again falling edge and what you feedback is falling edge. So, you give rising edge at the input and you want to feed the falling edge and if you can maintain that, then you can have sustained oscillations.

So, what we do here is we keep two inverter chains as shown here and in one case, I feed rising edge and in other case, I feed falling edge somehow. So, in response to these rising and falling edges, what we are going to get at the output, this will be falling edge transition in response to input A, you will have rising here, falling here and then again rising here. If we feed it back, there will be no oscillations. But in response to the falling edge here, you get rising, then again falling, then rising and then falling edge.

So, if at a given instant of time, I gave the rising edge at input A and falling edge at input, let us call this as now as  $\overline{A}$ , then you will get the output here, I call this as E and  $\overline{E}$ . I will get the output at E as a rising edge and a falling edge on  $\overline{E}$  after the same delay which is 4 times the delay of inverters. So, this delay is 4 times the delay of the inverter, same delay. Now, I will go and connect the falling edge of the inverter with this in this manner and the rising edge here is going to be connected to the falling edge input A.

Now, you just look how this is going to work. Again, there is an assumption here that somehow we are going to, this is A,  $\overline{B}$ ,  $\overline{C}$ ,  $\overline{D}$  and  $\overline{E}$  which you see here. So, somehow, I am going to enforce that if you have a rising edge at A, then you have a falling edge at  $\overline{A}$ . If I can enforce this relationship, then very well I can connect it in this manner and when you apply a rising edge after delay 4  $t_d$ , you get a falling edge here and then when you have a falling edge at input A, then again after delay 4  $t_d$ , you will get a rising edge. So, it would become similar to what you have here.

So, let us do this. The delay of each inverter is  $t_d$ , the total delay of these 4 inverters is 4  $t_d$  as you see and what I need to do is I need to enforce a relationship between, I have to write it at

the bottom actually,  $\overline{A}$ ,  $\overline{B}$ ,  $\overline{C}$ ,  $\overline{D}$ . I have to enforce a relationship between A and  $\overline{A}$  in such a way that the clock transitions are opposite at these two nodes, and they should be at each inverter output also. So, to enforce that, one easiest way is that you connect a cross-coupled inverter like this. So, this cross-coupled inverter, I am going to connect at each output, so this is connected like this.

So, what is this cross-coupled inverter doing? Let us just look at it. So, you have an inverter connected in this manner like this, you connect between A and  $\overline{A}$ , B and  $\overline{B}$  and so on. So, this inverter is like you will have a supply also for this inverter and this inverter supply is the same as the other inverter supply in the circuit. So, what you can do is this, so here I am connecting like this here, so this is connected to *VDD* by the way in this case.

So, if you think that this is A and  $\overline{A}$ , if  $\overline{A}$  happens to be 0, then what will happen? If  $\overline{A} = 0$ , you are applying 0 to the gate of PMOS which will make this particular signal as 1 and when you get 1 here, it will through this MOSFET, it will enforce that your A remains 0. So, this cross-coupled latch actually maintains the inverted relationship between its two outputs. So, it has the two outputs which you are looking at, they are these nodes, so if you have 1 on one side, then the other node will become 0 and it will enforce this relationship.

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180,2 Phase Difference, Ad = 180°



So, if you think about it, if I take this, the main inverter which you have and then I have a crosscoupled inverter connected in between, so consider that the first input here, the input is 0 and here the input is 1, 1 is for logic high, if this input 0 becomes, if this is 0 and this is 1, then the output of the inverters will be 1 and 0, inverter.

So, when this 0 becomes 1 and 1 becomes 0, if this 0 becomes 1, then the output of the inverter will go to 0 and through this inverter, the output of this inverter will become 1 to 0 and then using this inverter, it will try to force this to 1. Also, at the same time, the 0 here will make this output as 1 and through this inverter, it will try to enforce this as 0.

So, this is going to happen that for changes here, these two outputs, the output of the two main inverters, you can say they are assisted by these two inverters also so that it maintains a same phase relationship at the output whatever phase relationship you have at the input. So, such an oscillator is actually you can say, it is called as a pseudo-differential oscillator, pseudodifferential ring oscillator, you get phases which are inverted.

So, if you try to find what is the phase relationship between the nodes A, B, C and D, well, what we are saying is that after 4  $t_d$  delay here, your output clock is inverted, that is like you are having time period  $\frac{T}{2}$  or 180° phase.

So, when you have this 180° phase for time, for a delay of  $t_d$ , then the phase difference between these four inverters with nodes *A*, *B*, *C* and *D*, that phase difference is going to be,

$$\Delta \varphi = \frac{180^{\circ}}{4} = 45^{\circ}$$

So, the phase difference is going to be  $45^{\circ}$  in  $\pm$  and then you will have  $180^{\circ}$  phase. (Refer Slide Time: 16:17)



So, for example, let us just look at this oscillator and make sure what is happening, whatever is happening, we understand it correctly. So, this is the oscillator, if you think that your signal at *A* happens to be like this, then signal *B*, signal *B* is going to be like this, this is signal *B*, it is separated here by 45°, the 0 crossing is separated by 45°, signal *C* is going to be something like this, this is signal *C* and signal *D* is going to be like this, this is signal *D*. So, the separation between your *A* and *C* signal is 90° and whatever you are seeing with signals *A*, *B*, *C* and *D*, exactly the same thing is going to happen between  $\overline{A}$ ,  $\overline{B}$ ,  $\overline{C}$ ,  $\overline{D}$  just in inverted phase.

So, I will just draw a couple of them. So, if you are having A signal as shown at the top, then your  $\overline{A}$  signal is just an inverted signal of your A. So,  $\overline{A}$  signal is going to be like this, this is your  $\overline{A}$  and your  $\overline{C}$  signal is just the opposite of your C signal which is going to be like this, this is  $\overline{C}$ , what you can see here is that we can have  $\overline{A}$  and  $\overline{C}$  signal as complementary of A and C signals and A and C signals are 90° separated and  $\overline{A}$  and  $\overline{C}$  signals are also 90° separated.

So, if I want *I*, *Q* and  $\overline{I}$ ,  $\overline{Q}$  clocks, I can very well use these phases here. This will be phase *A*, this is going to be *C*, this will be  $\overline{A}$  and this is  $\overline{C}$  and these inverters have an important role to play because they help us to maintain the same relation, have a 180° relationship between the two phases.

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So, now given this, the question always is how you are going to size these inverters for the pseudo-differential ring oscillator. So, whenever we want even number of phases, we can do so. Now, I will just take one cell or one part of this pseudo-differential ring oscillator because that is something which is repeated, and I have this cross-coupled inverter here. So, these nodes which we are using, they are A,  $\overline{A}$  and this is B and  $\overline{B}$ . I will say that the size of this inverter is X, let us say, and this inverter is Y.

So, one problem while using this cross-coupled inverter is the following and here by the way all the inverters are connected to *VDD*, *VDD*, same *VDD*. So, the problem with the inverter connected back-to-back is that it consumes a lot of power. So, if you understand this that how it is being connected, so what happens is this is connected here and this is connected here.

So, what is going to happen is that these inputs to this inverter which we are connecting between A and  $\overline{A}$ , here in between B and  $\overline{B}$ . So, when you have let us say B = 1 and  $\overline{B} = 0$ , when B = 1 and  $\overline{B} = 0$ , you can say your NMOS, this NMOS is turned off and this PMOS is turned off and these two MOSFETS, they are, because the output  $V_{DS} = 0$ , that is why they are turned off, but the other ones NMOS and PMOS are turned off because their gate overdrive is less than 0.

So, what happens is that during the transitions at B and  $\overline{B}$ , what you see here is during the transitions, they will also consume good amount of current, first thing. So, they consume a good amount of current and the power consumption in this cross-coupled inverter, this is by the way, you also call this as cross-coupled inverter, the power consumption in the cross-coupled inverters can be very high if you do not pay attention.

So, let us look at two things. One, the power consumption in cross-coupled inverter, that is one thing and the second thing is the relationship between *B* and  $\overline{B}$ , whether *B* and  $\overline{B}$  maintains a perfectly 180° phase or not. So, phase relationship between *B* and  $\overline{B}$ , these are the two things which decide the size of the inverter Y as compared to the main inverter X.

So, if you consider this cross-coupled inverter like this and let us assume that the size of this cross-coupled inverter Y>>X. If Y>>X, then you run into two problems. One problem is that if Y>>X, so I am having this cross-coupled inverter and using inverter *A*, an inverter connected to *A* and inverter connected to  $\overline{A}$ , if I make a rising edge transition here and I make a falling edge transition here and consider that previously B = 1 and  $\overline{B} = 0$ .

If that B = 1 and  $\overline{B} = 0$  was the initial condition and A goes from 0 to 1, so, ideally your B should go from 1 to 0, but before B can go from 1 to 0, the other inverter whose output was initially 0, it is trying to enforce this voltage as 1 itself. So, this cross-coupled inverter is trying to oppose the transitions which are initiated by signals A and  $\overline{A}$ .

So, if you make A and  $\overline{A}$ , if you make your cross-coupled inverter size much larger than your main inverters for the ring oscillator, then these cross-coupled inverters will oppose the changes, they will oppose the changes, so opposing the changes effectively means that you have to give a larger input or you have to continuously, your delay at the output will actually increase.

So, one thing is if you just have an inverter with some parasitic load and you go from 0 to 1, your output will more or less go from 1 to 0 with the delay dictated by the capacitor. But what happens when you have, for the same inverter when you have a circuit which opposes this transition going from 1 to 0 and who opposes? The other inverter opposes the transition because it holds till the time the input of this inverter changes.

So, let me say, so when you make a change here at *A*, *B* resists the change, so till the time you are able to change the input of this inverter. So, if you are not able to change the gate input, gate of this inverter, then because the previous value was 0, it will just hold that value at 1, so, it opposes. When you have some circuit which is opposing the transition, the transition will effectively be delayed.

So, if you increase the size of the inverter, cross-coupled inverter as much larger, then your effective delay of this circuit will increase and if the delay of this circuit increases, then the maximum frequency of operation for a pseudo-differential ring oscillator will reduce. So, that is something you cannot make it much larger.

Now, if you look at, let us say, if Y is much smaller, then what happens? If Y<<X, then in that particular case, the transition in response to this transition A and  $\overline{A}$  at the input, it is B and  $\overline{B}$  may not be aligned by 180° phase, so it is like this. So, I have a transition at A like this and transition at B is exactly aligned let us say at 180°, this is the clock A and this is clock  $\overline{A}$ .

So, ideally, *B* should be like this and  $\overline{B}$  should be ideally like this, but if you have, if the size of these inverters is much smaller, then the thing is depending on the mismatch of these two inverters and variation in the loading, you may see a deviation in these phases. It may be like this, it may be like this, it can be any phase. What these inverters do is because I am able to change the output or initiate the change in the output, these inverters are not opposing to a great deal.

So, as we saw that any change from this inverter will also get triggered here. Similarly, any change from this inverter will get triggered here. So, these two are related but if the size of the inverter is much weaker, if only these two inverters start dominating everything, then depending on the mismatch between these two inverters or any variation between the loading can cause this to deviate and when this deviates, you do not have exactly 180° phase relationship.

So, the size of Y has to be optimized with respect to X. You cannot keep it quite high, if you keep it quite high, your frequency of oscillation drops. If you keep it quite low, then in the presence of mismatch between the inverters, your phase relationship between the complementary phases like A and  $\overline{A}$ , B and  $\overline{B}$ , that phase relationship will not be good.

Also, whenever you are using these cross-coupled inverters, they consume a good amount of power. That is one thing also that in whichever case if we use, we cannot use much smaller size for Y because phase relationship will not be good, so we will use some, we will optimize the size, whatever size we are using, that will have a good amount of power consumption, it adds to the power consumption of the oscillator. If you look at it, the single-ended oscillator, when we want the phases like  $\frac{360^{\circ}}{m}$  where *m* is odd, you do not have any cross-coupled inverter. You do not need any cross-coupled inverter unless you want complementary phases.

So, this is the price which you are going to pay and you will try to look for solutions where you can maintain this phase relationship without burning power in the cross-coupled inverter. We will look at another topology for the pseudo-differential ring oscillator, but if you are using cross-coupled inverter, power consumption will increase for sure. So, that is how we optimize the size of the cross-coupled with respect to the main inverter.

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Now, coming to the point that what is going to happen because it has a lot of power consumption, so what can we do? So, one possible option is, so we do not want cross-coupled inverter but we still want the phase relationship. So, one of the options which is before us is, see cross-coupled inverter was having a relationship, was added between A,  $\overline{A}$ , B,  $\overline{B}$  and so on, so it maintained that.

Now, we see here that when you have a rising edge at the input and a falling edge here, then for this falling edge, you get rising edge here and you get falling edge at this node. So, these are just the edges, let me just write this, so you get rising edge here and falling rising edge here, this is going to be a falling edge, this is rising and so on. So, when you are having a rising edge at  $\overline{A}$ , at the same time you are actually having, this is rising, you are having a rising edge at  $\overline{B}$ .

So, we try to exploit this and connect a resistor like this. So, you can say when you have a rising edge on A, at the same time, you are having a falling edge on  $\overline{A}$  and this in response to the falling edge on  $\overline{A}$ , your B should rise so you have one path leading this way and you have another path assisting it. So, you try to maintain the phase relationship between B and  $\overline{B}$  and in order to complete that, I should have another resistor which connects like this.

So, here you will have similar resistors like this connecting each of these stages and then so this by the way connects here, the other one which you have is inverter goes away, so you have a resistor here, connects like this. So, this resistor, let me call this as  $R_f$ , the resistor value is the same, so how is it helping? It is helping that the transition on  $\overline{B}$  is related also to the transition at the node A, this is not independent, you have this relation between these phases with the help of resistor  $R_f$ .

So, what we have done is we removed cross-coupled inverter and connected feed-forward resistors, you can say that. The resistors themselves, they do not draw any power directly from the supply and what you can also say is that your power consumption reduced by using these resistors here and you can still maintain the phase relationship. So, here the power consumption is not a problem because they are not drawing any current from the supply. The thing is if  $R_f$  is too large, again there is an optimization for this feed-forward resistor here. If  $R_f$  is too large, you can effectively think that if  $R_f$  is too large, it is like going close to  $R_f \rightarrow \infty$ . If  $R_f \rightarrow \infty$ , there is no relationship between the phases, it is like an open loop, the circuit will not oscillate at all. So, if  $R_f$  is too large, effectively no relationship between the phases.

Now, if  $R_f$  is too small, so I will just go to another extreme. If  $R_f$  is too small, it is like I am shorting the node A and  $\overline{B}$ . If you short the nodes A and  $\overline{B}$ , again there will be no oscillations. So, in both the cases, you will not have any oscillations. So, you have to optimize this value of  $R_f$ , this resistor  $R_f$  such that your oscillations are also maintained and your phase relationship is also there and that you can find out using simulations, mismatch simulations and regular simulations for the oscillation in this circuit. An important thing here is that as soon as you use the resistor, you are loading your output nodes also. So, if it increases the parasitic capacitors and other things, then the frequency will be lesser. So, you have to try to minimize the parasitic capacitance which is coming whenever you add anything to this circuit. So, this particular oscillator has lesser power consumption in comparison to your oscillator with cross-coupled inverters.

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#1 Removed cross-coupled investers ected feedforward resistors + Effectively no relation 610 the phas

Now, you can use either of these oscillators depending on your requirement. One interesting thing here is that if you try to, so the one which we have used is using 4 or 8 inverters in the ring you can say, but if I try to use only 2 inverters like this where I want 90° phase only, so the circuit says is that I can very well connect the circuit like this and similarly I can have connection like this.

Now, the option before you is the following. I will just copy in case of this pseudo-differential ring oscillator, you can either have cross-coupled inverters at both these. You can say this is the fastest pseudo-differential ring oscillator in a given process because you are using minimum number of inverters in the ring. The other one option which you have is the following.

So, out of these two options, what you will find is that this option one is something which you can realize and it is going to oscillate because you have cross-coupled inverters which maintain the phase relationship quite effectively as compared to your oscillator using resistors. Here also you can maintain but not as good as when you use cross-coupled inverters.

So, if you take this particular example, you will find that this one is pretty hard to in any given process. This one is very hard to make it oscillate. Well, when you are using more number of inverters in the pseudo-differential ring oscillator, you add the phase, you have a phase delay along the ring which makes it oscillate, but when you have only these four inverters in the ring connected like this with the resistors, it is very hard to maintain that phase relationship or you can say you have a very narrow tuning range for these resistors to make it oscillate.

So, whenever we would like to use pseudo-differential ring oscillator with the minimum number of stages, whether you want or not, using the cross-coupled inverter is the only choice which you have. Thank you.