**Phase-Locked Loops**
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**Lecture – 41**
**Large-Swing Ring Oscillator: Part III**

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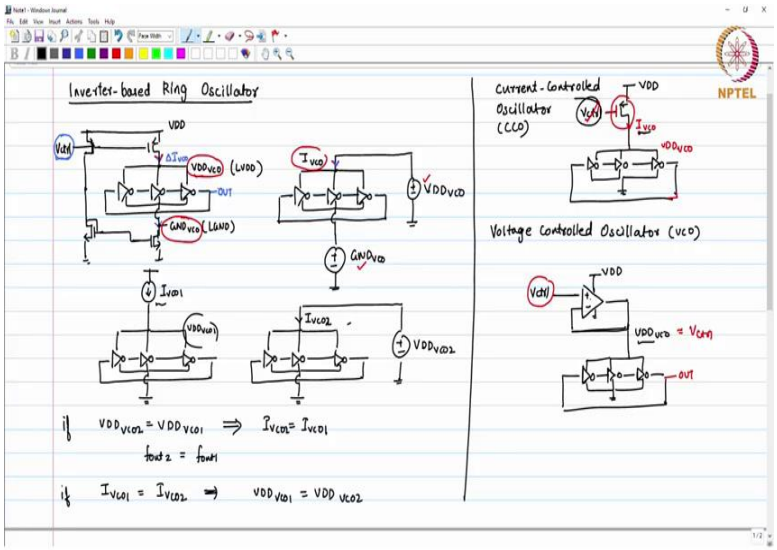


Hello, welcome to this session. In the previous session, we looked at inverter based ring oscillator where we control the frequency of the oscillator by controlling the current through the ring oscillator. So, let us just look at it. Inverter based ring oscillator is something which we studied and what we told that if we want to control the frequency of the ring oscillator, we can control the frequency of the ring oscillator by controlling the current or by changing the load.

So, here if you remember what we did we controlled the current somehow. So, we did this and by the way we controlled both the top and bottom. So, here we applied a current mirror and the current mirror was finally controlling the current. So, this was our $V_{ctrl}$. An important point here is the following that in this ring oscillator which you see, as you control $V_{ctrl}$, you are changing the current through the ring oscillator.

So, I will mark this voltage, so, the overall voltage is $VDD$ and the voltage which is at the source of the PMOS in the inverter is $VDD_{VCO}$, $VDD$ of the voltage controlled oscillator. And similarly, you have this lower voltage, this voltage is not ground, it is actually ground for the VCO.

Yes, in the previous session, I called this as local $VDD$ and local ground. Now, the thing is that because this VDD is for the oscillator, so we can call this as $VDD_{VCO}$ and $GND_{VCO}$. The important part here is that if you take this oscillator standalone, this particular node, I call, this node is $VDD_{VCO}$ and this node is $GND_{VCO}$.

So, to make it more clear, if you say that I am having a voltage source whose voltage value is $VDD_{VCO}$ and I am having another voltage source whose voltage value is $GND_{VCO}$, then whether you have the oscillator as you see on the right hand side or you have the oscillator on the left hand side, both the oscillators will operate at the same output frequency, output frequency is going to be same, so I call this as $I_{VCO}$.

So, the only difference here is that in one case, you are controlling $V_{ctrl}$. Because of the change in the $V_{ctrl}$, you change the current here. So, I call this change in the current $\Delta I_{VCO}$. So, when you change the current in the oscillator as $\Delta I_{VCO}$ and your frequency of the oscillator is some value, then you will automatically get the voltage $VDD_{VCO}$ and $GND_{VCO}$.

You are not directly fixing the value of this voltage $VDD_{VCO}$ or $GND_{VCO}$. You are fixing these two voltages indirectly. What you are doing is you are controlling the current through the oscillator and because you control the current, you will get the voltage automatically. In the other case, whatever voltage somehow it develops here at the top and bottom $VDD_{VCO}$ and $GND_{VCO}$.

Here I give these voltages $VDD_{VCO}$ and $GND_{VCO}$, then you will automatically get the current $I_{VCO}$, whatever the current $I_{VCO}$ which you have here and both the oscillators will operate at the same frequency. So, it means that if I can control for, if you just simplify it further, and if you say that I have this ring oscillator connected like this, one of the nodes can be ground or it can be some other potential, so I am connecting it to ground for easy circuit diagram here.

So, if I take this oscillator and just a copy of this, you have this oscillator. In one case, what I am doing is I am forcing the current $I_{VCO1}$ such that it develops a voltage, let us say, $VDD_{VCO1}$. In the other case, I apply a voltage source $VDD_{VCO2}$ and here you have a current $I_{VCO2}$. So, if we have,

$$VDD_{VCO2} = VDD_{VCO1}$$

then you will have,

$$I_{VCO2} = I_{VCO1}$$

If the frequency of the oscillator is going to be same, then we have,

$$f_{out2} = f_{out1}$$

where, $f_{out2}$ is the output frequency for the second oscillator and $f_{out1}$ is the output frequency for the first oscillator. Also, if I make sure that,

$$I_{VCO1} = I_{VCO2}$$

Then in that case, it will be quite clear that,

$$VDD_{VCO1} = VDD_{VCO2}$$

You may think that this is easy, this is how it should be. The thing is if we understand this, then what we can do is we can have a voltage controlled oscillator or a current controlled oscillator, both of these can be used.

So, what I can do is if I want to have a current controlled oscillator, then I can just use a current source with $VDD$ here and apply a control voltage which controls the current and I keep this as an oscillator. So, what you are doing here is effectively, though you are changing the control voltage, but actually in response to your control voltage, you are changing the current through the oscillator.

You are not fixing the voltage $VDD_{VCO}$ directly, that is what you are not doing whereas if you want to have an ideal voltage controlled oscillator, what you can do is you can use a regulator to fix the output voltage. So, I will give this as $V_{ctrl}$ and with respect to this $V_{ctrl}$ and this $V_{ctrl}$ feeds to your oscillator. So, this is there, these are all grounded. So, this is $VDD_{VCO}$. The amplifier, you can have the amplifier connected to $VDD$. This is one way.

So, here if you look at it, your $VDD_{VCO}$ is directly controlled using $V_{ctrl}$. If this amplifier has enough gain, then your $VDD_{VCO}$ will always be equal to $V_{ctrl}$. So, you control the output voltage or the voltage which is connected as a supply to the inverter and that is how you control the output frequency. In the first case, you control the voltage to the voltage of the gate for the current source which is PMOS and thereby you control the current.

In response to the current, your frequency will change. So, normally you can say that this is a current controlled oscillator, you are controlling the current, CCO is short form for that and the bottom one is voltage controlled oscillator because you control the voltage or the supply for the inverter directly.

So, one thing is also there that whether it is a current controlled oscillator or a voltage controlled oscillator, the ring oscillator is going to oscillate at the same frequency. Either you give the fixed same current in both the cases or you somehow maintain the same voltages in both the cases.

So, there is no difference with that. It is just that what you control and what is the cause and what is the effect. Here $V_{ctrl}$ is the cause and the effect is $I_{VCO}$, you directly change the current. Because you change the current, the frequency changes.

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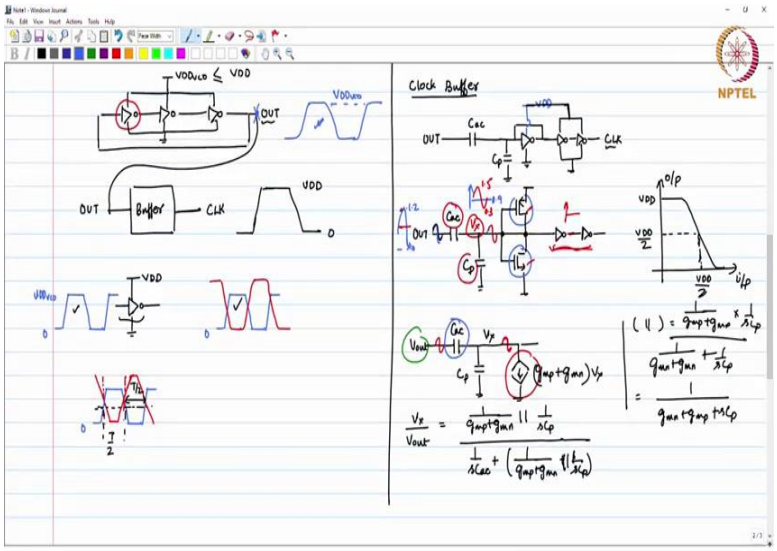

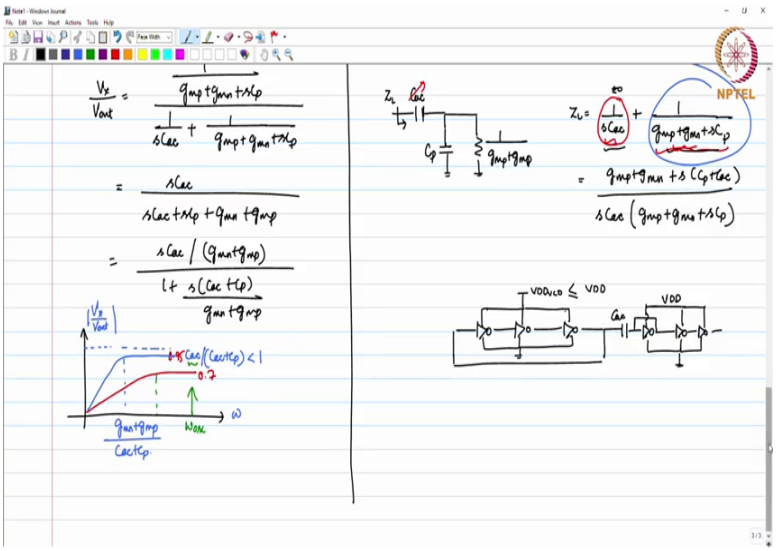


Now, so, what we have seen so far is we have seen inverter based oscillator and in order to control the frequency of the inverter, we actually ended up controlling the supply voltage or the current of the oscillator. Now, one interesting thing here is that or let me just tell you there are two things which we do not understand so far in our basic stuff.

One, this oscillator, when we control the supply of the oscillator, so, we control the supply $VDD_{VCO}$ to change the output frequency. Whether we change the current or we change the supply, at the end we are changing the supply voltage of the oscillator to change the output frequency. So, this $OUT$ signal, if your supply of the inverter is $VDD_{VCO}$ which is going to be always less than equal to the $VDD$ in a given process. If that is the case, then the $OUT$ signal is not going to swing more than $VDD_{VCO}$. So, the swing at the output signal is going to be limited by $VDD_{VCO}$.

Now, where does our logic stand that initially we were using small-swing oscillator, we shifted to full-swing oscillator because that is more useful, the swing does not depend. Now, we are saying that in order to control the frequency, you change the supply voltage so the swing argument has gone to toss. So, we have to do something that can restore the full swing without compromising on our frequency tuning.

So, what we need to do is we need a block where the output of the oscillator comes here. Let me call this as a clock, $CLK$, this is $OUT$, we should have full swing signals rail to rail, 0 and $VDD$. We want such a kind of clock to help us. So, this $OUT$ signal is this. So, we do not want to change

the frequency. We just want that whatever signal you have here, this signal you have previously the signal as shown here, that gets restored to 0 to $VDD$ and nothing else do we want to change.

So, this block should act as a buffer for the clock where the clock frequency is retained. So, the only thing is that the swing is amplified to full scale. So, one way to do is the following. So, what we have seen here is that an inverter is used in the oscillator. So, we are going to use a similar inverter here whose supply is not $VDD_{VCO}$ but $VDD$ itself, so this is not $VDD$.

So, if I give any signal here at the input, whether that signal is 0 and $VDD_{VCO}$ or $VDD$, the output of this particular inverter is going to be full swing because if you have a simple inverter, then what you will see is something like this and you will have this kind of signal. Right now do not go over the crossing points, but this is what you will see at the output.

So, this seems that if I want to buffer the clock, I can just connect an inverter and then I can get the full swing. But actually what happens is that because you have an inverter, this particular inverter, you will have a threshold voltage for NMOS and PMOS in the inverter. So, with respect to midpoint here, you may see this whole as $\frac{T}{2}$ whatever the time period you have and this also as $\frac{T}{2}$. But when you give this signal to an inverter directly, what is going to happen is that you will not get the same duty cycle.

So, the inverter which is designed with 0 to $VDD$ here, that inverter will have crossing points like this. Those crossing points will be at $\frac{VDD}{2}$, those crossing points will not be at $\frac{VDD_{VCO}}{2}$. So, your duty cycle will get distorted. So, what we should do here is the following that somehow we have to restore the duty cycle and buffer the clock. So, for that particular purpose, you can say a clock buffer is something which we need to design and we need to retain the duty cycle.

So, let us say you are getting $OUT$ from the oscillator and you are going to AC couple that output of the oscillator to an inverter which is self-biased and if it is self-biased inverter and this is grounded, you are going to connect this to the supply $VDD$ and then it follows regular inverters connected to $VDD$. So, it is connected here, same. So, if you look at the clock here, this particular clock will have full swing and it will be actually having 50% duty cycle if you have symmetric waveform here.

So, this capacitor is AC coupling cap which is $C_{ac}$. When you connect the inverter back-to-back like this, well, there will be capacitance at this node also, let me call that as $C_p$. So, when you have an inverter which is connected back-to-back, what you are doing is the following. So, $C_p$ is just a model of the cap which I have. What am I doing? I will just first draw the inverter here, the way we are having in our circuit and this is connected back-to-back and all the other inverters are same.

You are not connecting back-to-back there. Now, this is your $OUT$ and this is your $C_p$. So, you can model this. So, now, the thing is that $C_p$ is the capacitor which will come on its own because of these MOSFETs PMOS and NMOS. You need to decide on the value of $C_{ac}$ such that your output frequency is buffered. One thing is that if you bias the inverter, self-biased inverter which you have, then inverter input to output characteristics we have seen before, they are something like this.

So, normally you can design an inverter where you have input and output values as $\frac{VDD}{2}$, this can be done. So, you have that way, choose the PMOS and NMOS sizes accordingly. So, this is a nominal operating point, you get this capacitor. So, when you have any frequency coming here, what is that signal going to see? That signal is going to see a loading because of the PMOS and NMOS current sources here and $C_p$ both.

So, what you need to do is you need to choose your $C_{ac}$ value in such a way that whatever signal you get here, actually the same signal comes here. The question is whether same signal will come here or not. So, let me call this as $V_x$. So, in order to find out, I will first assume that I can model this inverter which is self-biased using its linear model. So, I will have $C_p$, $C_{ac}$ and this is nothing but because drain and gate are connected.

So, you are going to get $g_{mp}$ and $g_{mn}$. So, I will just write this as $(g_{mp} + g_{mn})V_x$, they act as a load. And here it is $V_{out}$ signal coming from your oscillator. So, we get,

$$\frac{V_x}{V_{out}} = \frac{\frac{1}{g_{mp} + g_{mn}} || \frac{1}{sC_p}}{\frac{1}{sC_{ac}} + \left(\frac{1}{g_{mp} + g_{mn}} || \frac{1}{sC_p}\right)}$$

So, to calculate that value, we have,

$$\frac{1}{g_{mp}+g_{mn}} || \frac{1}{sC_p} = \frac{\frac{1}{g_{mp}+g_{mn}} \times \frac{1}{sC_p}}{\frac{1}{g_{mp}+g_{mn}} + \frac{1}{sC_p}}$$

So, we get,

$$\frac{1}{g_{mp}+g_{mn}} || \frac{1}{sC_p} = \frac{1}{g_{mp}+g_{mn}+sC_p}$$

So, that is what you have here. So, we have,

$$\frac{V_x}{V_{out}} = \frac{\frac{1}{g_{mp}+g_{mn}+sC_p}}{\frac{1}{sC_{ac}} + \frac{1}{g_{mp}+g_{mn}+sC_p}}$$

$$\frac{V_x}{V_{out}} = \frac{sC_{ac}}{sC_{ac}+sC_p+g_{mn}+g_{mp}}$$

$$\frac{V_x}{V_{out}} = \frac{sC_{ac} \Big/ (g_{mn}+g_{mp})}{1+\frac{s(C_{ac}+C_p)}{g_{mn}+g_{mp}}}$$

So, this transfer function is actually a high pass transfer function and for this high pass transfer function, what you see there is a pole and pole is at $\frac{g_{mn}+g_{mp}}{C_{ac}+C_p}$. So, if I plot versus ω for that matter, if I plot this, it is like a high pass transfer function and then it will become flat. What is the value at which it will become flat? Well, the value is going to be, so, we are trying to evaluate at a very high frequency that you can easily evaluate and that is equal to $\frac{C_{ac}}{C_{ac}+C_p}$, it just acts like a capacitive divider and $\frac{C_{ac}}{C_{ac}+C_p} < 1$.

So, that is what you will have and the pole frequency happens to be at $\frac{g_{mn}+g_{mp}}{C_{ac}+C_p}$. So, when you are choosing this capacitor $C_{ac}$, you need to understand this transfer function. First, we want this gain to be close to 1. So, what we want is whatever frequency is coming at the input here, the same frequency should, the same magnitude should come here, that is ideally required. If you do not do

that, if you choose your $C_{ac}$ in such a way, so, let us say, one curve is like this, another curve where your $C_{ac}$ is actually smaller, another curve may be like this.

So, this curve, let me just pick a value, is 0.95, this happens to be 0.7. So, your output swing will get reduced, that will happen. The other thing is the frequency which is present at $V_{out}$, your cut-off frequency should be smaller than the frequency at the input of the buffer. So, this frequency whatever your $f_{osc}$ or $\omega_{osc}$ here, this should be greater than $\frac{g_{mn}+g_{mp}}{C_{ac}+C_p}$.

Second, if you want that the amplitude should not degrade, then you should make $C_{ac}$ large such that the degradation in the amplitude is lesser, that is how you need to choose it. So, typically, you will not choose a lower value of $C_{ac}$ because if you choose a lower value of $C_{ac}$, your amplitude will reduce. Then you can say what is the problem even if amplitude reduces.

So, what you will see is, for example, if I am having this as a 1.8 Volt supply, my swing which I am getting at the input happens to be like this where you have zero and this is for example 1.2. So, what you are going to get here is whatever the common operating point which is 0.9, so, at 0.9, I will get $\pm$0.6, so this is going to be 1.5 and 0.3, that is how the swing will appear at $V_x$ and this swing will then be amplified by another inverter based on what inverter you are using.

So, this may get amplified to 1.8 or maybe 1.75. So, it will take a couple of stages, if your swing is low at $V_x$, it will take a couple of inverter stages to amplify that particular signal to full swing. Now, whether it is good or bad, well, when it is amplifying, it is also adding noise to the system. That is a white noise, but that is what will happen.

So, ideally, you would like to get whatever swing is available here, you would like to get the same swing. If it is amplitude of 0.6, you will like 0.6 to come here. You may not be able to do it, you may get maybe 0.55, 0.57 or something but do not choose the capacitor value $C_{ac}$ such that the amplitude reduces, that will be more problematic. So, that is what we do. Then you can ask a question, well, if a large $C_{ac}$ is something which we require, then why do I go and calculate it? I will just use a large capacitor much larger than $C_p$.

Well, if you do that, let us say, you choose a much larger capacitor, the problem is not the amplitude, the problem will be your actual frequency itself. And what is that? It is $C_{ac}$ with $C_p$ is

in parallel with your impedance $\frac{1}{g_{mp}+g_{mn}}$, this acts as a load for the oscillator. So, it acts as a load for the oscillator and it is given by,

$$Z_L = \frac{1}{sC_{ac}} + \frac{1}{g_{mp} + g_{mn} + sC_p}$$

$$Z_L = \frac{g_{mp} + g_{mn} + s(C_p + C_{ac})}{sC_{ac}(g_{mp} + g_{mn} + sC_p)}$$

So, you get impedance loading on the oscillator. Now, well, this is just a series of one capacitor and another RC. So, here, if you think about it that $C_{ac}$ capacitor happens to be much larger, I do not care about it, it is 10pF or something, I may use.

Then, this impedance, this is an approximation, so, this impedance is going to be negligible. If this impedance becomes negligible, this impedance dominates in this combination. It is like you can say the capacitors which are added up in series. So, if this, if $C_{ac}$ is quite large and this impedance is going to be much lower or it is close to 0, just an example, and this impedance dominates. So, effectively you can say that this impedance loads your oscillator here at the output node.

If you load your output node of the oscillator by any impedance, this is $g_m + C_p$, depending on the fact that among $g_{mp} + g_{mn}$ and $C_p$ which dominates, you can get which is dominating factor or overall you are having this impedance, it is going to load your oscillator and if it loads your oscillator, it is going to alter the output frequency. Any loading, any loading like RC loading is going to reduce your frequency of oscillation.

So, it is not always advisable not to worry about this $C_{ac}$, you can use at any given time, you can use a large $C_{ac}$ and it will work. Well, it worked for the amplitude but it actually lowers the frequency of the oscillation also. So, while choosing this $C_{ac}$, please optimize this such that the frequency of the oscillation is not that much compromised and you get a good amount of swing at the input of the inverters chain for your buffer.

So, to convert the oscillator, just to give you a complete picture, you can actually do this. So, I just need to connect it with this here and this is going to be connected to a buffer chain, this is connected here, all these are connected to full $VDD$, this is $C_{ac}$. You do not connect any $C_p$, $C_p$ capacitor will

come on its own. That is how you convert limited swing of the inverter to full swing for the full swing clock at the output. Thank you.