Phase-Locked Loops
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Lecture – 40
Large-Swing Ring Oscillator: Part II

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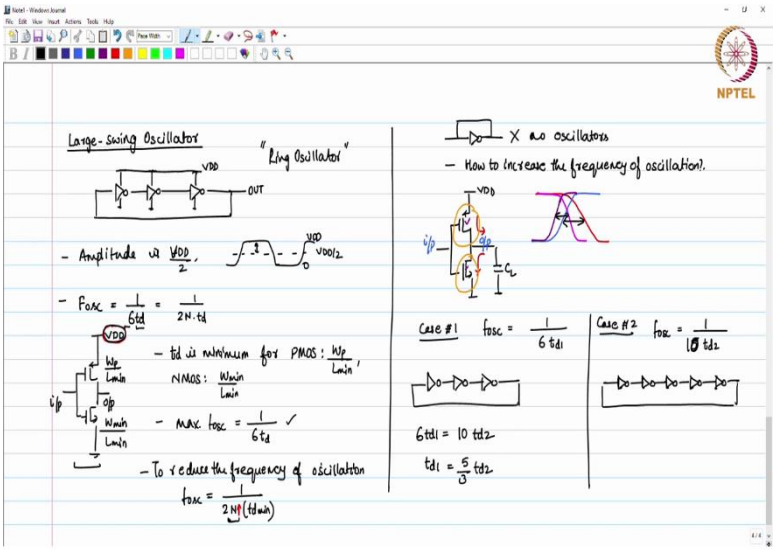

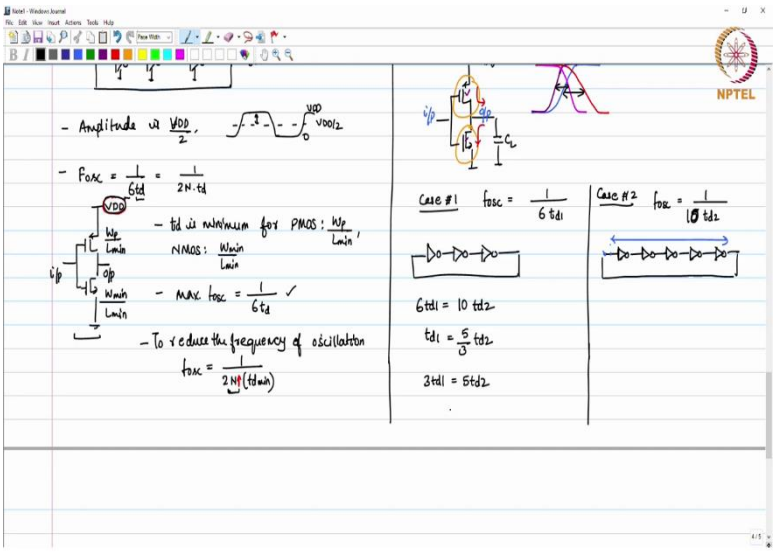

Hello, welcome to this session. In the previous session, we looked at large-swing oscillators' basic structure and we could realize large swing with odd number of inverters in the ring where the inverters were connected to VDD and ground. So, this is the same VDD which I have and I will call the output of the oscillator as OUT.

So, the amplitude is fixed for now, amplitude is $\frac{VDD}{2}$. Why did I say $\frac{VDD}{2}$? Because your output is going between 0 and VDD, so, the DC value is $\frac{VDD}{2}$ and you can say the amplitude is $\frac{VDD}{2}$. The frequency of oscillation is $\frac{1}{6t_d}$ in our case. What we need to find is when we want to design an oscillator for the desired output frequency, we can choose t_d or we can choose the number of inverters.

Now, both these parameters as we see, they are tuneable. So, which parameter you can tune and how much that is something which we need to understand while changing the frequency of the oscillator. So, let us say, you choose a certain technology. In the given technology, you will design an inverter and when you want to design an oscillator with the highest frequency possible in a given technology, highest frequency means that the input-to-output delay has to be minimum.

So, you design an inverter in such a way that parasitic loading is minimum. So, I design an inverter, mostly I am going to choose a minimum size W_{min} and L_{min} for NMOS and L_{min} will be chosen for PMOS. W_p will be chosen in such a way that you have equal rise-to-fall and fall-to-rise delay. That is how we will choose it. We know that PMOS has a lower mobility as compared to NMOS. So, PMOS size is going to be larger.

So, given this size of the inverter and the supply voltage allowed in a given process, the delay t_d is minimum for PMOS size as $\frac{W_p}{L_{min}}$, where W_p is decided in such a way that you have equal rise-to-fall and fall delay. NMOS size is $\frac{W_{min}}{L_{min}}$. So, we design this inverter.

Now, when we have an inverter with the minimum delay, at that time, the frequency of the oscillation which you can get, maximum frequency of oscillation is equal to $\frac{1}{6\,t_d}$. Now, you can ask a question why is it $\frac{1}{6\,t_d}$? Well, the first thing is that we need odd number of inverters. So, 3 is the minimum in which this particular block is going to oscillate. If you would have chosen only one inverter connected back-to-back, this is not going to oscillate at all, no oscillations here. For 2 inverters, we have seen the problem with even number of inverters.

So, this is the maximum frequency of oscillation which you can get. From here, if I want to increase or let us first look at if I want to reduce the frequency of oscillation. To reduce the frequency of oscillation, the only way I have is to increase the number of inverters. We have,

$$f_{osc} = \frac{1}{2N\ t_{dmin}}$$

So, I can only reduce the frequency of oscillation by increasing the period by increasing this N.

And if the question is that how to increase the frequency of oscillation? So, to increase the frequency of oscillation, there is only one way and that method is to increase your VDD. Why increase your VDD? Because the delay which we were considering from input to output, that depends on charging of the capacitor. So, this is under the assumption that when you have an inverter and you have a load C_L. When you have a load C_L and the frequency of the oscillation depends on the input-to-output delay, this is input, this is output.

So, it depends on the input-to-output delay. If somehow I increase the strength of the transistor which is discharging the capacitor or charging the capacitor, what does it mean? That I am going to increase the strength of the MOSFET with charges the capacitor. So, maybe this changes to something like this and similarly discharging happens also faster, then I can say I reduced this delay to only this much of delay.

That can happen under the condition that you increase the VDD of the inverter and as you increase the VDD of the inverter, your PMOS is going to work with a larger overdrive, larger gate-to-source voltage, even NMOS whenever it works, it is on, it will work with larger gate-to-source voltage and they will reduce the delay.

Now, the thing is that in a given process, you have an upper limit on the supply voltage. So, you cannot increase the supply voltage beyond a certain value. So, there will be an upper limit on the frequency of oscillation which you can realize using large-swing ring oscillator.

You always call this as a ring oscillator, it is a closed ring. You can, without doing anything else, with this you cannot reduce the time period or you cannot increase the frequency. There are other methods where we try to reduce the delay but they are more complex ones. Right now we are sticking to the simple ring oscillator. We can surely increase the time period or reduce the frequency as we have seen by having more number of stages.

So, now just consider two cases where I am trying to realize the same frequency of oscillation, f_{osc} is same. One, I am having let us say $6t_{d1}$ and in another case what we have, frequency is the same but here I am trying to realize with 5 inverters in the chain.

If oscillation frequency is same, then you know that what you are going to have is something in this case it is going to be like this and in the other case it is going to be like this. And as we see if the frequency of oscillation is same, then, we get,

$$6t_{d1} = 10t_{d2}$$

$$t_{d1} = \frac{5}{3}t_{d2}$$

So, the delay of each stage is actually different in the two cases, and you can design an inverter in such a way, you can increase the sizes of the inverters, you can add more capacitor to the inverter such that the loading is different. So, there is no reason right now to choose only 3 inverters. You can always realize with the larger one.

So, the difference between these two oscillators is going to be the following. In the case where you are having, see one thing is sure in both the cases, the delay from the first inverter to the fifth inverter is same. So, that is delay from first inverter to the third inverter is $3t_{d1} = 5t_{d2}$. The delay over the chain of inverters is the same.

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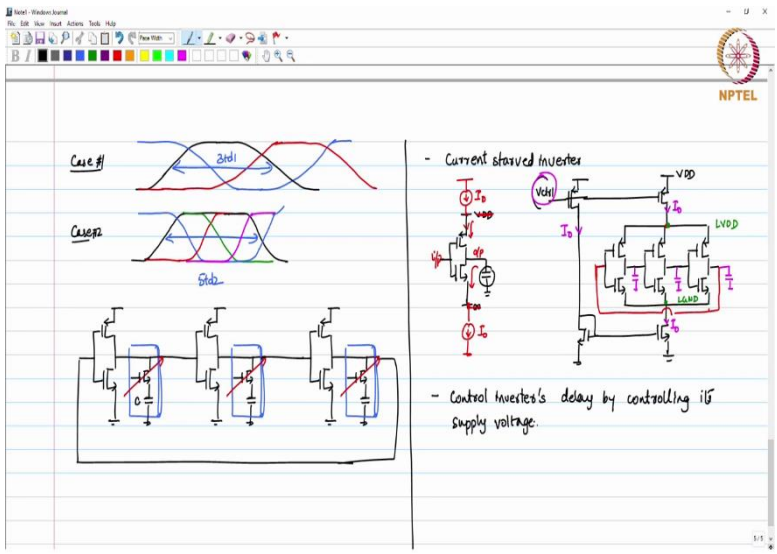

So, what is going to happen is, in case 1, you will see that the waveforms, the clock waveforms which you realize, they will have more rise and fall time. So, this will be, so, let us say this is what you get in case of case 1. So, you are going to have, it is just a waveform. So, please do not worry about this. So, you will see the clock waveforms at the three nodes something like this with a larger rise and fall time. In case 2, what you are going to see is these waveforms will have typically, they will have a shorter rise and fall time.

So, if this is the case, I have to accommodate 5 of such waveforms. So, let us see if I can do that. This is second, then you are going to have in response to this you are going to have this, then in response to the green one, I am going to have this, and this is black one. This is $3t_{d1}$ and this is $5t_{d2}$ and both the values are same.

So, in case you are using a larger number of inverters in the ring to get the same frequency as in the case where you are using lesser number of inverters, your clock waveforms will be sharper or they will have a lower rise and fall time which is kind of evident from our expression.

So, you can realize the oscillator with the same frequency with different number of inverters but what you will see is this is different. Later we will see what happens in the presence of noise but that is for the later sessions. So now, we are looking at the frequency of the oscillation. We find that there is an upper limit on the frequency which we can get in a given process. The way we can reduce the frequency is by increasing the number of inverters.

So, that is all what we can do. One other way, so, here we said that we increase the number of inverters. The other thing is how can you increase the delay? Well, I can increase the delay by adding extra load on the inverter. So, I can always have a switch with a capacitor which I can connect. This is just a switch which is used to connect this gap as on or off. You can connect it either this way or you can connect it with the switch first or the capacitor later.

So, both the options are possible. Which one is used? It depends on the process. So, if you have this inverter, for example, where this particular block I will say is customized, how much capacitor do you want? So, this block has a variation involved. So, I can use this as a single cell and then another one here.

So, it connects like this and then you can connect it. Based on how much capacitor you are switching on the inverter, you will change the load of the inverter and then you are going to vary the output frequency. So, you can do that. Another way to vary the delay or to increase the delay is using current starved inverters. Now, this is something which we need to understand.

So, all these things which I am talking about, we are reducing the frequency, we are making the frequency to be controlled, by all these methods, we are not increasing the frequency of oscillation beyond what we get with this three inverters minimum delay oscillator.

So, current starved inverters will help us to control the frequency and mostly reduce the frequency below the maximum frequency in a given process. So, what we have is that the

inverter which you have, this particular inverter has, it may have its own load, it can have extra load, this load capacitor has to be charged and discharged during every clock cycle.

So, when we were connecting this node to VDD and ground, at that time, whatever current is required from VDD, that current was used to charge this capacitor and the NMOS was able to operate with full swing to full gate-to-source voltage to discharge the capacitor. Now, we go ahead and say this is no more VDD, this is no more 0. I am going to constrain both these nodes and how can you constrain? I have, ideally speaking, the total current which you can have is limited.

So, you limit the current in the oscillator in each inverter and if you are limiting the current in each inverter, you can change the input-to-output delay for each inverter. So, such an inverter is called as a current starved inverter. Now, you can ask a question that well, if you take a fixed current source and PMOS is off, what will happen to this current source? Well, the voltage will go to VDD but at that time PMOS is off.

So, when I say this is current I_0 or I_0 in both the cases, the maximum current which the inverter can draw from the supply is I_0 and that is the maximum that can help you to charge this capacitor. Similarly, the maximum current which can be used to discharge the capacitor is also I_0. So, you are limited now, by the current which is used to charge or discharge the capacitor.

So, this is going to reduce the frequency of oscillation and it will also help in controlling the frequency of oscillation. How? Let us just look at it. So, this is the basic idea behind the current starved inverter. The way I am going to do is the following. I will take the inverter like this and let us take three copies of this inverter, this I can connect it.

So, we have this, all these three inverters I can do that and I control the current which goes to the oscillators. This is now VDD and I can control this current by using V_{ctrl}, by the way, this is let us say V_{ctrl}, I control the current, the same current I am going to mirror on the bottom side also and the oscillator is connected in feedback like this.

So, what is going to happen here is your V_{ctrl} decides what is the current, bias current, let us say I_0. So, this is going to mirror I_0 current here and I_0 current here. So, at any time, the maximum current which each inverter can draw from the supply is I_0 and this is going to limit the charge and the discharge rate for the capacitor and it is going to change the delay of each inverter, it will increase, by the way, as compared to the minimum delay and it is going to limit the output frequency.

So, you have seen a couple of ways in which you can control the frequency, one by changing the capacitive load, another by changing the current. This current method can also be looked at in a different way that when you are limiting the current, actually you are limiting the supply also on these two nodes, it is not only that you are limiting the current, this supply is not going to reach VDD.

So, I will call this as let us say local VDD ($LVDD$) and this node as local ground. So, your local VDD and local ground, they are actually limited. $LVDD$ is lesser than VDD, local ground is actually greater than ground. So, the way we controlled our inverter delay by controlling the current source, you can also control the inverter's delay by controlling its supply voltage. So, you can do both of these if you require to vary the oscillator's frequency. Thank you.