Phase-Locked Loops
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Lecture – 39
Large-Swing Ring Oscillator: Part I

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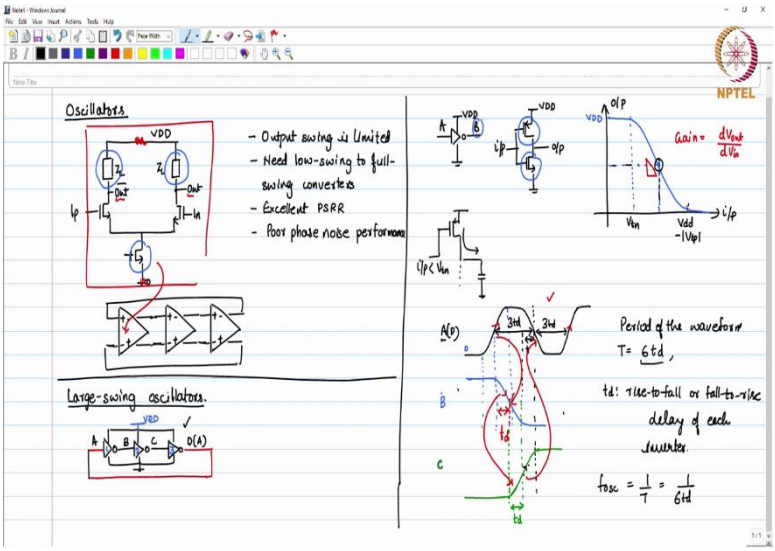

Hello everyone. Welcome to this session on oscillators. So, in the previous session, we looked at oscillators with differential delay cell and symmetric load. So, let us just have a quick update about that. So, we had load, we have seen a load where it was a simple passive resistor with a voltage-controlled resistor and then the symmetric load using Maneatis cell. So, in all these oscillators, whichever we use, so, this was the delay cell in our oscillator and this was the load Z_L, you had I_p here, I_n here, and Out and $\overline{Out}$.

This particular cell was used in the oscillator like this. So, you had minus and plus. So, we use this block and then this was connected, feedback by the way, and you had this. So, if you look at this particular oscillator where this was the delay cell, so, the load, as I told that we have seen the load as passive resistor, voltage controlled resistor as load and then symmetric load with Maneatis cell. In all these cases, the output swing of the oscillator is still controllable but the output swing is limited.

You have VDD here and you have ground, so, your swing is not between VDD and ground, swing is not VDD or ground, it is actually VDD and $VDD - IR_L$, where R_L is the load resistor. So, when we are going to use this clock somewhere in digital circuits or in any other block for

RF or for your ADCs, we need full-swing outputs. So, these oscillators need low-swing or limited-swing to full-swing converter.

These oscillators have excellent, you can say, power supply rejection ratio, excellent PSRR power supply rejection. So, if you have any supply noise, that noise gets rejected at the output because the output is out minus out differential and supply noise or even the substrate noise that will appear as a common mode noise in this circuit. So, you have excellent power supply rejection ratio. The thing is that this particular oscillator has poor phase noise performance.

And we can understand this better when we are going to look at other oscillators where the phase noise performance is better. So, this has poor phase noise performance and the main reason is that all these current sources, this current source, the load whether it is a resistor or it is Maneatis cell, all these transistors contribute noise continuously during the oscillation of this clock.

So, it has poor phase noise performance. So, there is need to look at oscillators which can actually give you full-swing, do not need low-swing to full-swing converter, and have better phase noise performance. So, we need to see if there are some options like that. So, the oscillators which we are going to see now are typically classified as large-swing oscillators and these large-swing oscillators are mainly designed by using inverters.

Now, you think about it, the inverter is a block which has inputs and output as 0 and 1, and this block is going to be used as an oscillator. So, let us first understand how these inverters in the ring work as an oscillator. So, first I will complete the circuit. So, all these inverters are connected to supply VDD and right now they are connected on the other side as ground, the feedback one is actually which makes the inverting operation or oscillation operation here.

So, what we have is this. So, let us name these nodes as A, B and C and the Out node of the inverter, third inverter, this Out node is D which is connected to A itself. I will write this inverter as inverter 1, 2 and 3. This is connected to VDD. So, you have an inverter like this which is connected to VDD and ground with inputs let us say A and B independently. This inverter is made up of NMOS and PMOS transistors.

So, you have like this, this is VDD, the gates are connected and the drains are also connected, these are A and B. This inverter has input to output characteristics as shown. So, if I just write this as input and output, this is input, this is output. So, input to output characteristics of the inverter is something like this. So, there exists a point in the inverter where you can use this

inverter as a gain amplifier whereas for inputs much lesser than the threshold voltages on either side, you have output as VDD or ground.

So, you look at the PMOS here and NMOS here. When input is quite low, at that time NMOS will be turned off and PMOS is turned on and you have for the inverter itself, the PMOS is on, NMOS is off. So, I am not drawing that and whatever capacitive load you have, you are actually charging that load to VDD.

For input lesser than the threshold voltage of NMOS, only PMOS will work and it is going to charge the output voltage to VDD, that is what you have here. When your input is greater than $VDD - |V_{tp}|$, at that time your PMOS will be turned off, NMOS is turned on and the output is actually equal to 0. These characteristics of the inverter, they are at DC input voltages, if you bias this inverter at a point where input and output are same for example, then you may have this as an operating point. If this is your operating point, then you can say that I am having the maximum gain.

So, when we are looking at gain, what are we looking at? We are looking at the slope of this curve. So, gain is, you can say, dV_{out} whatever your output voltage by input voltage. So, that gain is maximum at this node. So, this is a basic inverter operation. The other thing is that when you apply any input to the inverter, so, I will just draw the waveform. So, let us say, I apply some input to this inverter, this is my input.

So, for the given input A, the output of the inverter B is going to change. The output of the inverter will change after some delay and it will be like if the inverter input was 0 here, at that time, the output of the inverter will be VDD or logic 1 and then as your input starts going to change, your output will also change. So, when the input crosses the mid value, the output crosses the mid value at some point and this is the delay which you have from input to output.

So, in response to A, you get the output delayed. The same thing is going to happen when, so, let us say I just, when the input goes low, in response to this input, the output will go high after some time and typically that is going to happen roughly at this same delay. So, this delay between the zero crossing of the falling edge of the input and the rising edge of the output is t_d only or you can design it such that it is t_d.

So, what we can have is that the rising input at A to falling output B, the delay is t_d. The delay between the falling edge at A and the rising edge at B, this delay can also be same. When you connect the inverters in the configuration as shown here, what happens is that in response to

A, let us say, you begin this experiment, you break the loop here, this is just for our understanding and your A signal rises, your B will rise after some time and then you are going to have signal C.

So, C signal will respond to the signal at B and if C is going to respond at B, what you are going to see here is that signal C will go high after some time and if I am using the same inverter for all 1, 2 and 3, this delay will also be t_d. Now, in response to C, I am writing this as D but the D is actually same. So, what is D here? So, D and A are same.

So, you will have the signal delayed in response to C, you can say, I am having the delay here such that it happens like this. So, the delay between the rising edge on C and the falling edge on D is again t_d. Now this process, so now if you think about it, when I had rising edge on A, we get falling edge on B, when we have falling edge on B, we get rising edge on C, in response to rising edge on C, we get a falling edge on D or A again.

So, this distance or the separation between the rising and falling edge on A or D signal is actually 3 t_d. So, we broke the loop, we applied a rising edge on A, we get a falling edge on D after 3 t_d and then I connected the loop back again. So, what happened? I applied a falling edge on A and when I apply a falling edge on A, using the same logic, we will see that we are going to get rising edge on A after the same time 3 t_d because the delay from rising to falling edge, the delay of each inverter is t_d.

So, you are going to get the rising edge again after delay 3 t_d. So, just to look at it again, rising edge on A gave you falling edge on B after delay t_d, falling edge on B gave rising edge on C again after delay t_d and rising edge on C gave you falling edge on A or D after delay t_d. So, after 3 t_d delay, you get a falling edge on A signal and when you get a falling edge on A signal, this is going to repeat and you are again going to get rising edge on A after delay 3 t_d and this process continues.

Now, you think about it, if this process continues, you do not have to feed any other signal to this particular block, it will automatically keep on varying with the waveforms like this. So, what is the period of the waveform? Well, the period of the waveform is given by,

$$T = 6\ t_d$$

where, t_d is the rise-to-fall or fall-to-rise delay of each inverter.

So, you can have an oscillator, as you see that you are seeing periodic waveforms here, you can have an oscillator with 3 inverters connected in the manner shown here and the oscillation frequency is given by,

$$f_{osc} = \frac{1}{T} = \frac{1}{6\,t_d}$$

Now, the next question which you can have is that who decides what is t_d.

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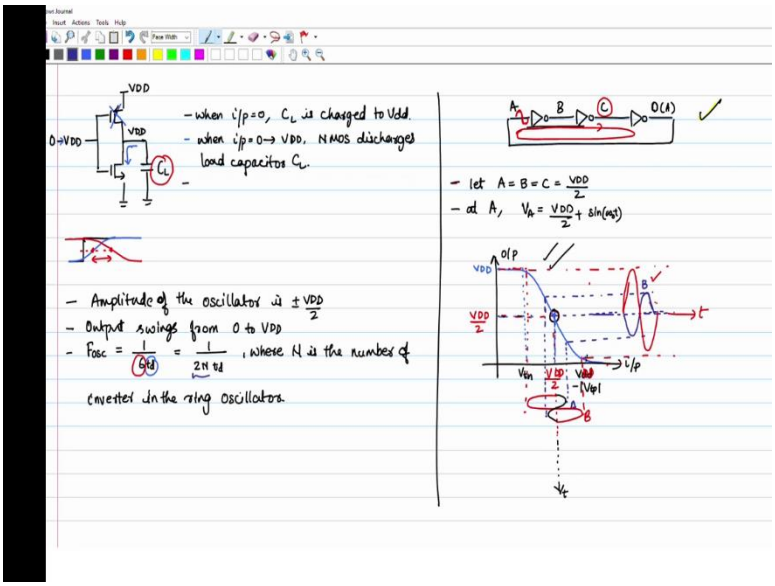

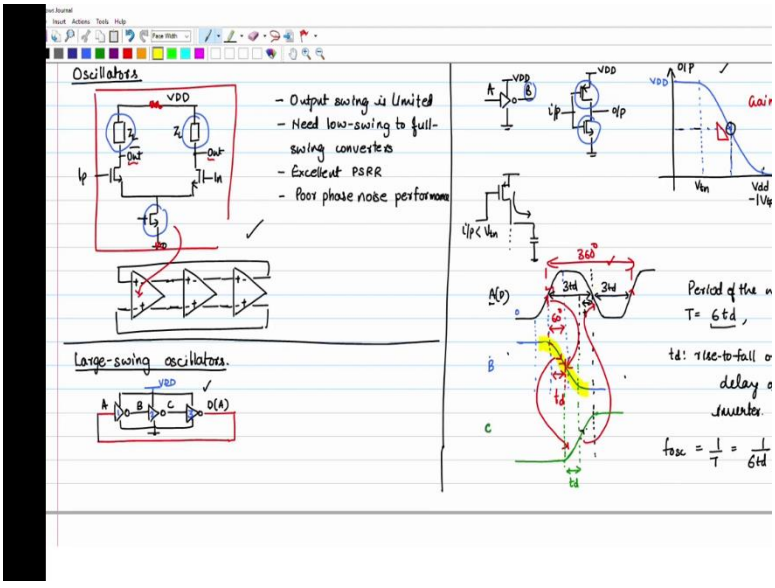

Because I am saying that you are having a delay t_d, then your question will be that what is the value of t_d or how we decide t_d? Well, that is a simple one to answer. Let us say you have an inverter and when you have an inverter and the input is either 1 or 0, so, let us say, input is 0,

this is VDD. If input is 0, the output voltage will be VDD only. Both the MOSFETs will come with some capacitor.

So, I am just drawing the effective capacitance at the output, effective capacitor at the output with value C_L. So, when input is 0, C_L is charged to VDD. When I make a transition at the input from 0 to VDD, if you make a transition with zero time, then also. When you make a transition from 0 to VDD, what happens is PMOS is turned off and NMOS starts drawing current from the output voltage.

When input makes a transition from 0 to VDD, NMOS discharges load capacitor C_L. It takes finite time to discharge the load capacitor C_L from VDD to 0 and surely from VDD to $\frac{VDD}{2}$ and that is the delay which we are talking about. So, when the input goes from 0 to VDD, the output goes from VDD to 0 in some finite time and that finite time is coming because you are discharging the capacitor which was earlier charged to VDD.

Now, in practice, you cannot give an input like this first. Your input is always going to have some kind of rise and fall time and when you have finite rise and fall time at the input of the inverter, PMOS will not turn off instantaneously, NMOS will not turn on instantaneously. So, there is some time in which PMOS will go from saturation to linear to cut-off or from linear to saturation to cut-off. So, it goes to all regions of operation during any rise or fall transition.

So, there is some finite time at the input. So, for the same reason, you have a finite time at the output and we look at the difference between $\frac{VDD}{2}$ as the delay because that is what is going to be repeated throughout the ring. So, what we have here is that based on whatever capacitor you have at the inverter, this capacitor is not right now any external capacitor, this capacitor is coming because of the load of the transistor itself. So, that is what you have.

So, in this way you can design an oscillator with the period $\frac{1}{6\,t_d}$ and we understand what controls the period, the charging and discharging rate. So, if we look at it, the amplitude of the oscillator or oscillator output, any node here can be used as output of the oscillator because each node is symmetric with respect to the other node, is the same, amplitude of the oscillator is $\pm\frac{VDD}{2}$, the output swings from 0 to VDD.

The frequency of the oscillator is given by,

$$f_{osc} = \frac{1}{6\,t_d}$$

where, t_d is the delay of each inverter. So, now one can say if I want to design an oscillator with a different frequency, what I need to do is I need to change t_d or I need to change the number of inverters in the ring.

So, here I can have,

$$f_{osc} = \frac{1}{6\,t_d} = \frac{1}{2Nt_d}$$

where, N is the number of inverters in the ring. This is called as a ring oscillator in general. Now, one can question that previously for these oscillators what I did was I told that you need to have a loop gain and angle should be 360° as per Barkhausen criterion, and this time when I introduced the large-swing oscillators, I did not talk anything about it.

So, are these two things different? Well, these two things are not different and that is the reason I introduced this kind of input to output characteristics of the oscillator. So, let us look at it from loop gain perspective and see what happens. So, you have a ring oscillator or you can say 3 inverters connected in this manner, same nodes A, B, C and D is as same as A.

So, if I have the input to output characteristics of the oscillator as shown to you here and just assume that there is one operating point for these inverters such that the input and output potential is the same. So, this is $\frac{VDD}{2}$ and this is also $\frac{VDD}{2}$. You can have an operating point like this but this is the point where you have the maximum gain for the oscillator.

So, to begin with, let potential A equal to B equal to C is $\frac{VDD}{2}$ and this is a perfect operating point if you can have such that the input and output potentials are same. In this case, you can say that there is no need for any oscillations. This is a stable operating point or a solution for these MOSFETs connected in the circuit or the inverters connected in the circuit.

Now, consider that there is noise at any given frequency and I am considering only at one particular frequency. So, I have a small sinusoidal waveform at point A which serves as an input. So, small value, it serves as an input. So, what you are going to have here is that the potential at A (V_A) is given by,

$$V_A = \frac{VDD}{2} + \sin(\omega_0 t).$$

Now, if you have that, your actual input at A can be like this with respect to time, this is your time axis. So, I am just drawing with respect to time. So, what you can have, in response to this

input which you are seeing in black here, you can have an output and we know that the output is amplified version of the input.

So, when we see an output as an amplified version of the input, when this is positive, you can say you have because the gain is large. Well, how did you get that? You get that by this. It is an amplified version, same amplitude so let me just make it for the same. It does not seem to be symmetric because my sine wave is not symmetric here but that is what you are going to get.

So, just from these input to output characteristics of the inverter, you see that the output gets amplified. So, this happens at A and this happens at B. When this happens at B, the C inverter, you can think about it that you are applying this signal B as an input here. So, what you can say is that the signal, this particular signal, is applied here with an amplified voltage at B and in response to B, you are going to get the output at C.

What is the output at C? It is going to be amplified. So, what you try to understand from here is that we have these 3 inverters in the chain, $\frac{VDD}{2}$ can act as an operating point such that there are no oscillations and both the inputs and outputs of each inverter, that is $\frac{VDD}{2}$, and then if there is any swing or because of noise or any other reason, there is some sine wave at a given frequency, then what is going to happen is that it is going to get amplified as I showed you here using the input to output characteristics.

Now, as you see the things start building up and when they build up, they are going to reach VDD and 0. It will keep on doing this, it may start from a very small amplitude but finally it will keep on building up and then it reaches 0 to $\frac{VDD}{2}$ and that is how you get your oscillation build up from none to full-swing oscillations.

So, when you have a single sine wave here, you can actually apply the Barkhausen criterion here for the given operating point. It is not that it is working with some other phenomenon, it is the same thing. So, what is the same thing? That the gain across the loop, it will start building up the oscillations when the gain across the loop and the phase which you are adding up, that phase is equal to 360°. Then finally this swing is more and it saturates to VDD and 0 and then you get the full-swing oscillations.

So, you cannot have the oscillation build up until and unless at a given frequency, you have the phase equal to 360°, that is the condition for the oscillations to build up. Now, if you look at it,

in time domain also, when I am looking at the phase difference, see this is a square wave characteristic, this is like a square wave with a finite rise and fall time.

So, I am just looking this as 360° from rising edge to rising edge. The separation between the rising edge at A and the falling edge at B is t_d or this angle, you can say, is how much? This angle is equal to 60° but this is 60° with the falling edge, the 60° which you are seeing, this separation, the separation is with respect to the falling edge. So, with respect to the phase, what you are going to see is that there is 120° separation from the input to the output. So, what we are having here is the phase shift between each of these clocks is 120° in steady state and that is what you will also get for this oscillator.

But one important thing is that we cannot apply our loop gain or Barkhausen criterion for the square waves because when the MOSFETs are off, the linear gain model does not prevail there. So, you do not have the linear gain model. You can apply the linear gain model only when you have linear gain. When your MOSFET goes into cut-off region, the linear gain characteristics which I am applying here cannot be applied but for the oscillations to build up, that is required.

So, once the oscillations build up, it reaches your 0 and $\frac{VDD}{2}$, you get the fixed-swing oscillations. Also, the oscillations will be sustained if and only if you have the delay like this. If somehow it happens that the delay is not maintained, then you will not have the oscillations. Now, another quick thing here is that I told that you can vary the number of inverters and you can get different output frequency.

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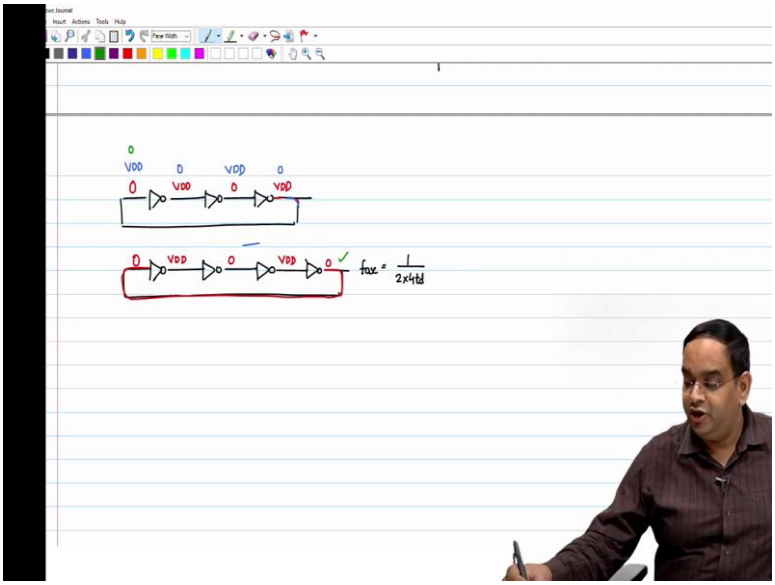

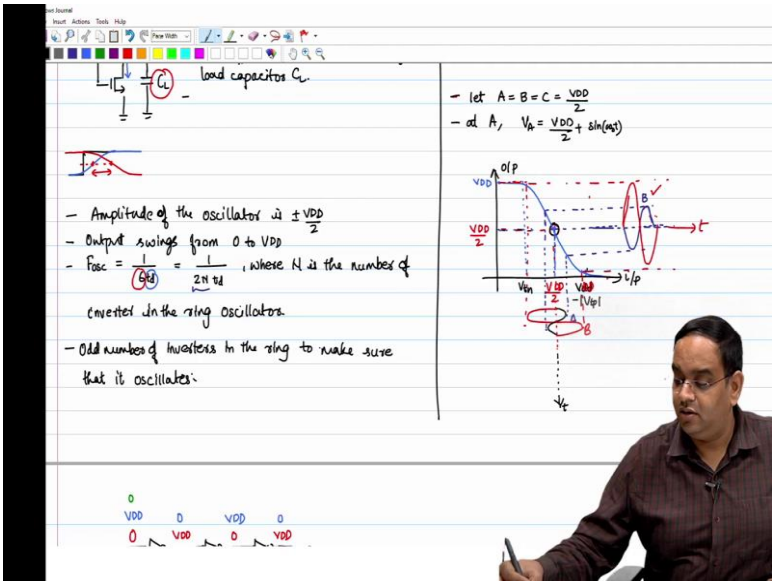

So, you can say, I can use any number of inverters and get the desired frequency. So, when I look at it, initially I had three inverters, now, I will say, I want to have four inverters. So, I will connect it in the loop and then I will get the frequency here, f_{osc}. If each inverter has delay t_d, this should be $2 \times 4t_d$, that is what the frequency of oscillation should be.

But the reality is that this particular block or this whole oscillator will not oscillate at all. The reason is when you are trying to build up the oscillations using the inverters and the method which we have seen here, what happens is you will reach steady state where the input of this is 0, this is VDD, this is 0, this is VDD and this is 0.

So, you see that you have another solution where you have in steady state, the input and outputs of the inverter are either 0 or VDD, they do not make any transition whereas in case of this odd number of inverters in the ring, if you have 0 here, you will get VDD, with respect to VDD, you get 0, then you get VDD again. So, you applied 0 here to begin with but what you get is VDD.

So, it will again trigger, this will be VDD, 0, VDD and 0. So, again this 0 comes back and you come back to 0. So, this keeps on happening in the ring oscillator with odd number of inverters whereas the same thing does not happen when you have even number of inverters in the ring.

So, if you are using a single-ended oscillator with even number of inverters, that will not behave as an oscillator at all. You should have odd number of inverters in the ring to make sure that it oscillates. Otherwise, you will see initially some transition, 0 and $\frac{VDD}{2}$ and finally it will saturate to 0 or $\frac{VDD}{2}$. Thank you.