Phase-Locked Loops
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Lecture – 38
Low-Swing Ring Oscillator: Part II

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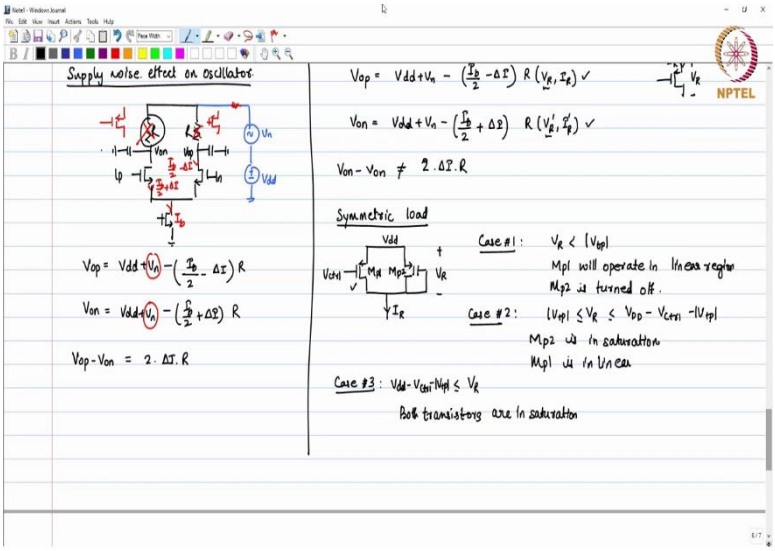

Hello, welcome to this session. In the previous session, we looked at how to change the output frequency in a simple ring oscillator where we use differential cells and we varied the resistance, we retain the output swing. Now, we are going to see what happens to this delay cell in the ring oscillator when you have supply noise.

So, in the presence of, let us understand supply noise effect on oscillator, the one which we have discussed before, the oscillator which we have discussed before. So, in our case, we had a simple cell like this as we see. Well, this was the first design which we used where we used poly or physical resistor here, not a voltage control. As soon as you have voltage control, things change.

So, we have input here and V_{op} and V_{on} and now let us consider that you are having a supply noise, this is Vdd and you have V_n here, supply noise. So, what happens is when you have supply noise which is this here, your V_{op} and V_{on} are going to change. At any given instant of time, if you have I_b current here and the current in one branch can be $\frac{I_b}{2} + \Delta I$ and in the other branch, it is going to be $\frac{I_b}{2} - \Delta I$.

So, the voltages which you are going to have at V_{op} and V_{on}, let me just write it, that is going to be,

$$V_{op} = Vdd + V_n - \left(\frac{I_b}{2} - \Delta I\right) R$$

$$V_{on} = Vdd + V_n - \left(\frac{I_b}{2} + \Delta I\right) R$$

This is the case when the resistance value remains fixed. So, if you look at the differential output swing, you do not have any effect of V_n on the output swing and if you do not have any effect of V_n on the oscillator output waveform, you have no effect on the noise or no effect on the jitter or the phase noise from the oscillator also.

So, here if you look at it, we have,

$$V_{op} - V_{on} = 2\ \Delta I\ R$$

It was the same before without the noise also. Now, when this resistor is replaced by a MOSFET, no matter which way you are biasing with V_{ctrl} or something. So, when you bias this particular MOSFET, then we have,

$$V_{op} = Vdd + V_n - \left(\frac{I_b}{2} - \Delta I\right) R\ (V_R, I_R)$$

The resistance is a function of the voltage and the current. So, I call this as V_R and I_R. What are these V_R and I_R? Well, if you take a MOSFET and you have a voltage difference at the source and drain node, this is V_R and the current which is flowing through the transistor is I_R. So, we have seen earlier that the equivalent resistance of the MOSFET has a dependence on the voltage difference across it, that was V_{SD}, and the current through it.

So now, we have,

$$V_{on} = Vdd + V_n - \left(\frac{I_b}{2} + \Delta I\right) R\ (V_R', I_R')$$

So now, V_{op} and V_{on}, what you see here that has $V_n - \left(\frac{I_b}{2} + \Delta I\right)$ and the resistance $R\ (V_R', I_R')$ because for the left and right side your voltage difference across the source and drain nodes is going to vary and since these two values are not equal, so, we get,

$$V_{op} - V_{on} \neq 2\ \Delta I\ R$$

We had $V_{op} - V_{on} = 2\,\Delta I\,R$ in the case when you were using passive resistors. So, this is a problem.

So, all the noise which you get, this particular noise gets converted to your supply noise which you will see that noise at the output and that is also going to affect the phase noise. So, to address that problem, Maneatis proposed a kind of a symmetric load and with the help of that symmetric load, we could actually get a supply noise rejection. So, let us first understand what this symmetric load is.

So, let me just write it as in place of simple voltage controlled MOSFET, we are going to use a symmetric load and that symmetric load is like this. You have two PMOS, one PMOS is controlled by a control voltage V_{ctrl} and the other PMOS is connected or you can say the drain and source are shorted. This is Vdd, I am just drawing the current, the total current drawn from this load is I_R, the potential difference between the Vdd and the output node is V_R.

Both the MOSFETs have the same size. Now, this MOSFET operates under different conditions. So, let me just write this as M_{p1} and M_{p2}. So, in case 1, you can say when V_R is quite low, that means when $V_R < |V_{tp}|$, at that time, the M_{p2} transistor will be turned off because $V_{SG} - |V_{tp}|$ for that transistor is, V_R is actually equal to V_{SG} of the M_{p2} transistor. So, if $V_{SG} < |V_{tp}|$, the transistor is not on and M_{p1} will only be on and M_{p1} will operate in linear region. This is one case, and here M_{p2} is turned off, we are not considering the sub-threshold conduction here.

Then, case 2 will be, this MOSFET operates in different cases, so first we understand that and then we will look at the current versus the voltage profile. When $|V_{tp}| \leq V_R \leq Vdd - V_{ctrl} - |V_{tp}|$. So, what will happen when V_R increases more than $|V_{tp}|$, the M_{p2} transistor is in saturation and M_{p1} is in linear region of operation.

Then, what is going to happen when case 3, when $Vdd - V_{ctrl} - |V_{tp}| \leq V_R$, both the transistors will operate in saturation region. So, you see, depending on the swing available at this node, the drain node, your transistors are in saturation region, your current is going to vary.

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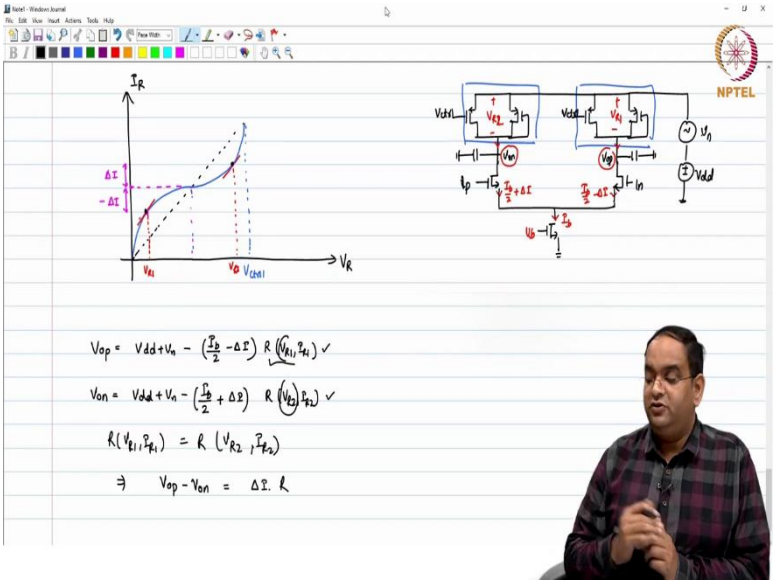

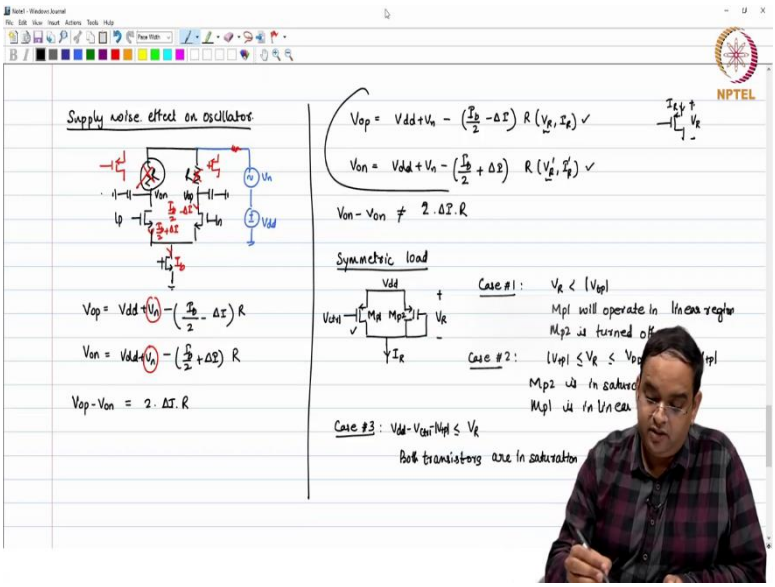

So, if I go and plot I_R versus V_R, I have given the region of operation, you can actually find out this value. So, this is going to be, depending on the control voltage what we have, you will see a characteristic like this and I am just writing let us say this is for V_{ctrl1}. So, I_R versus V_R characteristics are shown in this or they will turn out to be like this.

The interesting thing for these characteristics is that if you look from the midpoint, then if you go $-\Delta I$ down or you go $+\Delta I$ up, so, this is going ΔI up, then this is going ΔI down from this point, you pick up these points, the slope of I_R versus V_R or the resistance value which you know, so, the resistance is not only calculated as $\frac{V}{I}$. For a non-linear device, you are going to calculate resistance as derivative of that non-linear function.

So here, the resistance is the slope at this point and here the resistance is the slope at this point. You see that for the change in the current $+\Delta I$ and $-\Delta I$ and for the different voltages, V_{R1} and V_{R2}, the slope remains the same. Now, this is the interesting part. How? If I use this Maneatis cell load as an actual load in the oscillator cell, then my cell will be something like this.

So, here I am going to have NMOS load connected in this manner. You can find the control voltage in the same way as you found for the replica such that the output swing remains constant. We are using Maneatis cell with a specific purpose of reducing the supply noise effect on the output. So, I am not going through the biasing for fixed output swing right now.

So, I give this V_{ctrl} here and V_{ctrl} here, we have this I_p and I_n and you can have the capacitive load as desired, this is V_{op}, this is V_{on}. So, what we do, this is bias voltage V_b, and this is I_b. So, at any given time, you have $\frac{I_b}{2} + \Delta I$ and here you are going to have $\frac{I_b}{2} - \Delta I$. So, for these currents, you know that these voltages will be different and the equivalent resistance of each cell, this cell and this cell, it depends on the potential V_{R1} across them.

So, the example which we took, this potential, let us say is V_{R1} and this potential is V_{R2}, $-\Delta I$ I took, this is V_{R2} and this is V_{R1}, where you have $-\Delta I$, I took V_{R1}. So, with these potential differences, you see the slope is the same. Now, if the slope is the same, the resistance value is going to be the same. So, I just need to rewrite these equations when you have supply noise. This is Vdd, this is V_n.

So, what we have here is,

$$R\ (V_{R1}, I_{R1}) = R\ (V_{R2}, I_{R2})$$

This is because the resistance value is the slope as you see at these points and the slope is the same. So, since we have $R\ (V_{R1}, I_{R1}) = R\ (V_{R2}, I_{R2})$, this implies that we get,

$$V_{op} - V_{on} = \Delta I\ R$$

So, your supply noise is not affecting the resistance, it is actually getting cancelled out. When we are talking about the supply noise, we are talking about your Vdd, V_n changing your V_{R1} and V_{R2}. It affects both of them in the same manner. So, by using the symmetric load in the oscillator or this Maneatis cell in the oscillator, we can get a better suppression of the supply noise to the output. Thank you.