Phase-Locked Loops
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Lecture − 37
Low-Swing Ring Oscillator: Part I

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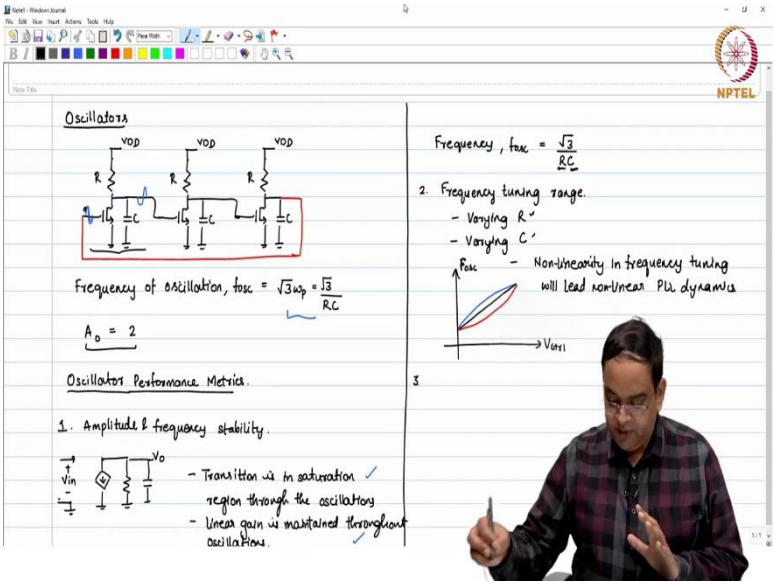

Hello everyone. Welcome to this session. We were discussing about the oscillators in the previous session and we looked at a simple common source amplifier based ring oscillator. So, you had R and C at the output load like this. I had this R and this is C connected to VDD and we had three of these connected like this and we also worked out the conditions under which such a circuit is going to have sustained oscillations.

So, what we did, we connected it like this and it is connected in ring in this manner. So, this particular oscillator, we worked out and the frequency of oscillation is given by,

$$f_{osc} = \sqrt{3}\omega_p = \frac{\sqrt{3}}{RC}$$

So, this was the frequency of oscillation and we also told you will have sustained oscillations if the dc gain of each stage was equal to 2.

So, given that the dc gain of each stage is equal to 2 and you will have sustained oscillations here. Now, with this simple oscillator if you look at it, what all things do we need in any given oscillator whether this oscillator meet our demands or not. So, the performance parameters, oscillator performance metrics, we have to define that, performance metrics whether this

oscillator is good or not, it will meet our demand or not, that is something which we need to figure out.

So, first thing is, in this particular oscillator, what is the amplitude of oscillation? Amplitude and frequency stability are the two things which you will measure for any given oscillator. So, here in this particular oscillator, we made sure that there is a certain small signal model of each block and the small signal model of each block was something like this where you have the current source effectively, the load resistor, the load capacitor and so on and this was the gate input.

So, if this is input V_{in}, we have this as V_{out}, this was the small signal model of the transistor. So, the small signal model of the transistor which we were using because the transistor is a non-linear device, so our assumption was that the transistor is in saturation region, this was our assumption, saturation region throughout the oscillations. So, even when you have some swing at the input and output nodes, the transistor remains in saturation region and the linear gain is maintained throughout oscillations.

Now you can ask a question that what will be the output swing. Well, the oscillation analysis using the Barkhausen criterion did not impose any kind of amplitude limit on this particular oscillator. So, you can say that you are going to have swing, the swing can be 1 mV also or the swing can be 100 mV also, till the time these two conditions are satisfied, transistor is in saturation region and our linear gain approximation is valid. If our linear gain approximation is not valid, we cannot write the gain of this and find the oscillation frequency like this.

So, overall we can say that the oscillator output amplitude is not fixed, it actually depends on what kind of signal you have initially and you can maintain the transistor using a linear gain model. When we talk about the frequency of this oscillator, this is given by,

$$f_{osc} = \frac{\sqrt{3}}{RC}$$

f_{osc} actually depends on the resistor and the capacitor. So, as long as we maintain these resistor and capacitor values, the frequency of the oscillator is fixed, it is not going to vary.

So, if you maintain R and C fixed and you maintain the dc gain of each stage as 2, the frequency will not vary but what the amplitude is going to be, that is not fixed because it depends on how much overdrive you have biased the transistor, what kind of signal swing you are having in the beginning when the oscillations build up.

Then the next parameter which we have to look for this oscillator is the tuning range of the oscillator, frequency tuning range, because we are going to use this oscillator in the PLL so we should be able to vary the frequency of the oscillator. So, here, well, speaking about this oscillator you can say, if I can vary R and C of the oscillator, I can vary the output frequency of the oscillator. So, varying R and varying C will give you the tuning range for the oscillator.

Now whether you are going to get a linear tuning range or a non-linear tuning range, it depends on how you are varying the resistor and the capacitor. So, what we are looking at is the following that with respect to your control, now this can be V_{ctrl} or I_{ctrl}, voltage or current control, ideally we want a linear relationship but you may see, depending on how you are controlling, you may see a non-linear or some other kind of relationship between the control voltage or current and the output frequency.

Now any non-linearity in frequency tuning will lead to non-linear PLL dynamics which is not desired. So, if you change your K_{VCO}, your loop gain bandwidth and other things will change. So, that is something which is not desirable. So, we will go with this amplitude and frequency tuning for this particular oscillator, how we can do it, in a while.

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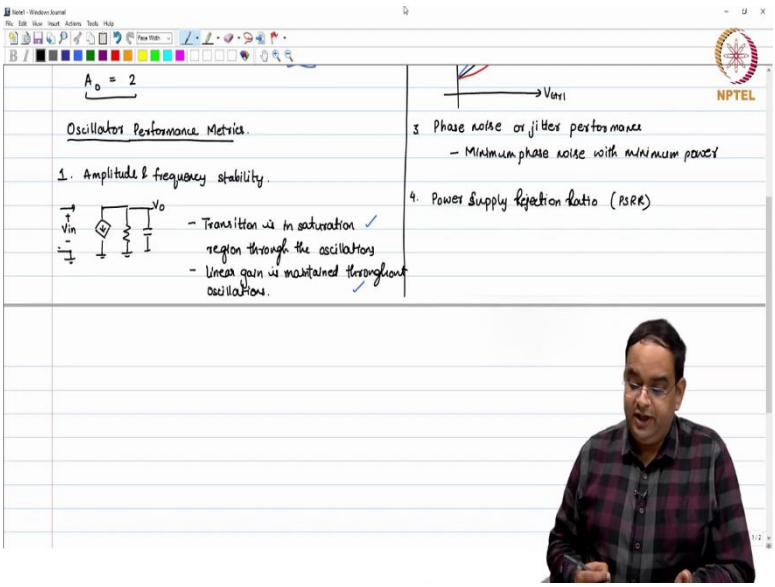

But the other metric which we are interested in is the phase noise or jitter output for the oscillator, phase noise or jitter performance. Ideally, we would like to have minimum phase noise with minimum power, that is the goal always but there will be some limits with what you can do in a given process. Then the other thing is power supply rejection ratio and this is measured as how you are affecting the VCO output frequency or VCO phase noise with respect

to the supply noise, this is called PSRR, let me just write it with all capital, Power Supply Rejection Ratio.

This is critical in ASICs where you are having multiple PLLs. So, if each PLL starts picking up the noise from the nearby signals, then the output of the PLL will be noisy not because of the thermal noise in the PLL, but because of the noise coupled on the supply from nearby signals. So, these are the performance metrics which we will look at during the design of the oscillator. So, let us come to this amplitude and frequency for the oscillator.

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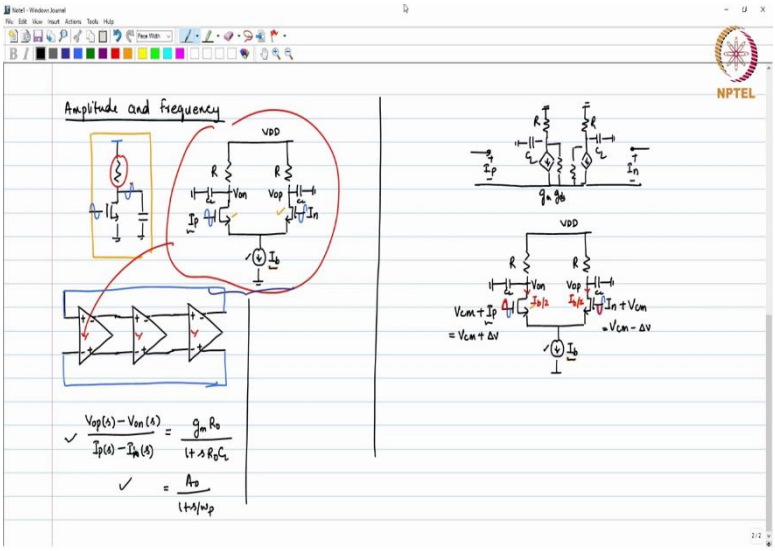

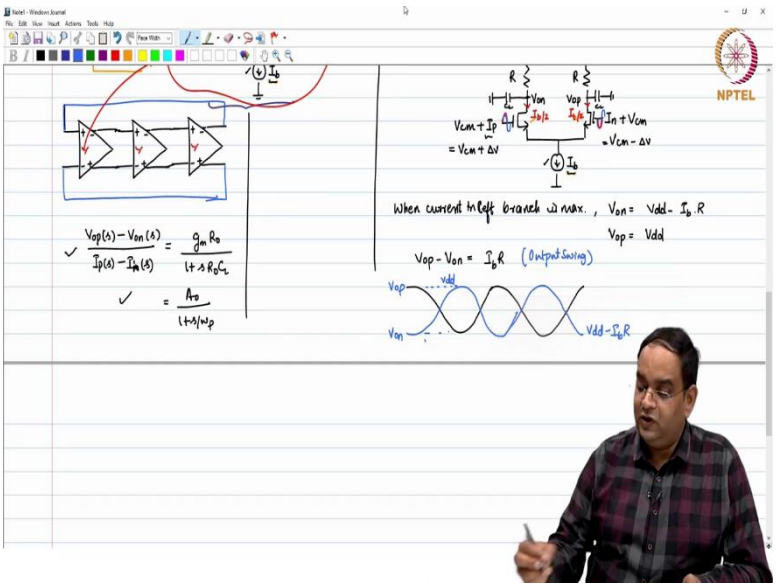

So, in the example which we have seen, our each cell is actually if you look at it when the input changes or you have any swing at the input, the corresponding output also varies and the current does not remain constant in this transistor or you can say the main transistor for this stage for

the delay from the input to the output and the swing which you are going to get is not fixed, as we have seen the transistor should remain in saturation region for linear gain model and the swing is going to be very limited which is not in your control.

So, if we would like to control the output swing, we would like to have a fixed current going through the resistor. So, fixed current because the swing which you are producing at the output when you have a maximum swing here, that time you are actually having maximum current going through the resistance, so if we can control the current in the RC load, then we can control the output swing.

So, as an example, let us look at a simple circuit like this where you have a differential pair as the input and with a fixed current I_b, this current is realized with a MOSFET but this current is fixed here, I_b. You have the load resistance R connected to the supply VDD and there is a capacitive load connected on both the sides. This is I_p and this is I_n, this is V_{op} and this is V_{on}.

Now, as a single delay cell in our oscillator, if we are going to use this, let us look at its operation. So, I am trying to show you with a single cell, this is normally an amplifier sign, so this block is there here, we have positive, negative, so this is actually positive, and this is negative. So, here I have this as a single cell and this cell is connected, in place of using a single-ended circuit, we use a differential circuit and it helps in limiting the output swing or defining the output swing as we desire.

So, let us look at it. So, now we connect these, so what you have is every sign which you are seeing is inversion, so I can very well connect it like this, it will make an oscillator. So, what I have done is I just created you can say first just a mirror image of this which you are seeing here and then fix the current source which is supplying the current to the cell.

Now, for each cell, if you look at I_p and I_n, and you have a fixed current I_b for this circuit, the gain of this circuit, this is like from differential input to differential output, is given by,

$$\frac{V_{op}(s) - V_{on}(s)}{I_p(s) - I_n(s)} = \frac{g_m R_o}{1 + sR_o C_L}$$

Here also both the transistors are in saturation region, so what happens here is the small signal model of the circuit which you are seeing on the top, this is, by the way, the gain of single cell.

So, for small signal model, you can connect it like this. The current source is ideal and you have, so, this node is not connected and you have load R here with capacitor connected to

ground. Now if there is any g_{ds} of the transistor, that g_{ds} will also come in, this is ground, this is ground, so this is R, C_L, R, C_L, you have g_m and g_{ds}, and corresponding I_p and I_n, you are going to have at the input.

So, what I have here is this is with respect to the source, so the source is connected here, this is I_p and similarly you have I_n. So, for the given small signal model, you will get a gain term like this. Now the way we have worked out the frequency of a common source amplifier connected in an oscillator configuration, in the same way we can work out this. So, this is given by,

$$\frac{V_{op}(s) - V_{on}(s)}{I_p(s) - I_n(s)} = \frac{A_o}{1 + \frac{s}{\omega_p}}$$

As we worked out previously, the frequency of oscillation will be equal to $\sqrt{3}\,\omega_p$.

Now we started this because we want to understand that how we are going to get the desired swing. So, now look at this circuit and when we are going to have a positive swing here and this is in a differential connection and a negative swing here, so this swing is applied at a given common mode voltage. So, you can very well say that I am going to have here, you can say the signal which you are having is $V_{cm} + I_p$, $I_n + V_{cm}$ here, and if the input is differential, then $V_{cm} + I_p$ can be $V_{cm} + \Delta V$ and this can be $V_{cm} - \Delta V$.

So, when $\Delta V = 0$, at that time the current which is flowing in each branch is actually $\frac{I_b}{2}$, and then when you have a positive swing here, the current in the left branch is more than the current in the right branch and at one particular time what will happen is when the swing is maximum and here the swing is minimum, all the current will get shifted to the left branch. So, you can say, at any given time, so when the current in the left branch is maximum, then you will have the value at V_{on} as minimum and V_{op} as maximum.

So, when current in left branch is maximum, then you have $V_{on} = VDD - I_b R$ and $V_{op} = VDD$ at that time because there is no current in the right branch. So, the swing, you are looking at differential swing, so differential swing is $V_{op} - V_{on} = I_b R$.

So, when you connect these cells in the feedback as shown, what you are going to see the signals during the oscillation phase or during the oscillation, you are going to see swings like this, and I can just, assume that these are sinusoids. The maximum value at any given time, so,

let us say, I call this V_{op} and V_{on}, the maximum value is VDD and the minimum value is $VDD - I_bR$. So, that is the output swing. So, if we want to control the output swing using such a differential cell, it actually gives you the swing which you want and you can also control the swing by controlling the current I_b.

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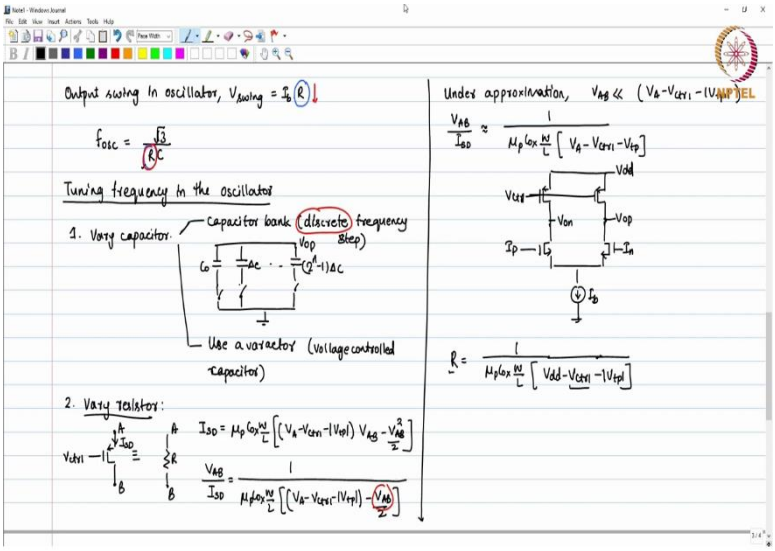

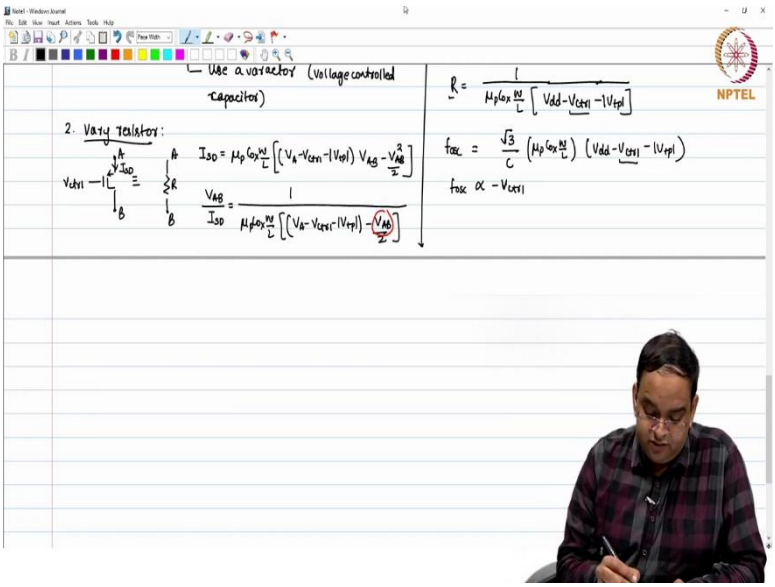

So now, what we have done is we have actually, output swing, I can write it like this that the output swing in our oscillator is given by,

$$V_{swing} = I_b R$$

We also know that the frequency of oscillation is given by,

$$f_{osc} = \frac{\sqrt{3}}{RC}$$

Now this is a problem that your output swing also depends on R and output frequency also depends on R.

So, let us say, you design the oscillator at only one particular frequency. At that time, depending on the resistor, you can always choose I_b such that you get the desired swing but when you would like to vary the frequency of the oscillator, in that particular case while varying the frequency of the oscillator using resistor, your output swing will also vary which is not a good thing, and on top of that what is happening is as you want to increase the frequency of the oscillator by reducing R, your output swing drops which is like at higher frequency, your output swing is lesser. The first thing is output swing should not vary with the frequency, and second thing is on top of that if output swing reduces with higher frequency, that makes the situation worse.

So, the thing which we need to figure out at first how are we going to change the frequency of the oscillator by varying resistor? How are we going to vary the resistor? So, if I just say to tune the tuning frequency in the oscillator, you have two options. So, let us look at both the options.

The first one is, I will just first have vary capacitor. Well, this particular technique is used to vary the output frequency but quite often the capacitor bank is used to vary the frequency and capacitor bank, capacitor bank means that you are having multiple capacitors connected with switches and you switch in these capacitors depending on the frequency which you want between your output nodes.

So, if I say, at each output node V_{op} and V_{on}, you had such kind of capacitor banks, you can switch the values. So, you can have C_0, ΔC and binary capacitor bank you can have something as $(2^n - 1)\Delta C$. The problem with this capacitor bank based approach is that the change in the frequency step is discrete.

So, when you are varying the frequency using the capacitor bank, you have discrete frequency step which is something which is not desirable, you want something continuous quite often, frequency step, and if you want to have a very fine resolution or frequency step, that capacitor which you can switch in will be very very small which actually becomes an implementation problem.

The other method is to use a varactor where you vary the capacitor with some voltage. So, you can do that but the range which is offered by varactors in case of frequency change is quite limited. So, both these options are available. This is, you can say, more of a voltage controlled capacitor. I am not saying you cannot do it but the range is normally limited, this can be done.

The second thing is you vary resistor. So, when you would like to vary the resistor, the one way as we have seen the way you have used, the capacitor bank, in a similar way you can use a resistor bank, but then also you will run into this discrete frequency step. So, what I would like to do is I would like to use a voltage controlled resistor and a MOSFET is a perfect voltage controlled resistor which we have seen.

So, given a MOSFET, it can actually mimic a resistor between the two nodes depending on the voltages. So, let us say, this is A and B, that is what you have, this is resistor which you want to mimic, I will use a control voltage to get the desired value. So, how do we find the MOSFET? There is a MOSFET for a given resistor, well, if you have a current I_{SD}, this is PMOS, flowing through a MOSFET, then I_{SD} is given by,

$$I_{SD} = \mu_p C_{ox} \frac{W}{L}\left[(V_A - V_{ctrl} - |V_{tp}|)V_{AB} - \frac{{V_{AB}}^2}{2}\right]$$

This is the current flowing through the MOSFET.

So, during operating point, you can say an equivalent resistance for this particular MOSFET is given by,

$$\frac{V_{AB}}{I_{SD}} = \frac{1}{\mu_p C_{ox} \frac{W}{L}\left[(V_A - V_{ctrl} - |V_{tp}|) - \frac{V_{AB}}{2}\right]}$$

So, you see that this resistance is actually depending on the V_{AB} value also, it is not an ideal resistance, it depends on V_{AB}. So, under the approximation that $V_{AB} \ll (V_A - V_{ctrl} - |V_{tp}|)$ which is also the condition for the MOSFET to operate in linear region, we can say,

$$\frac{V_{AB}}{I_{SD}} \approx \frac{1}{\mu_p C_{ox} \frac{W}{L}\left[V_A - V_{ctrl} - |V_{tp}|\right]}$$

Also, when this particular MOSFET is used in our current cell, and where was our current cell? Our current cell was, I am replacing the resistor with PMOS controlled by V_{ctrl} with input pair,

NMOS input pair, with a fixed bias current I_b. So, this is your I_p and I_n, V_{op}, V_{on}, and this is V_{ctrl}, here you have VDD.

So, for this case you have,

$$R = \frac{1}{\mu_p C_{ox} \frac{W}{L}\left[V_{DD} - V_{ctrl} - |V_{tp}|\right]}$$

So, what you see here is that I have a resistance which is controlled by the gate voltage V_{ctrl}. Well, the way you are seeing right now is it is inversely proportional to $-V_{ctrl}$, so if you increase V_{ctrl}, your denominator will reduce and resistance will increase. So, now the frequency of oscillation which was $\frac{\sqrt{3}}{RC}$, so, well, you will get,

$$f_{osc} = \frac{\sqrt{3}}{C}\mu_p C_{ox} \frac{W}{L}\left[V_{DD} - V_{ctrl} - |V_{tp}|\right]$$

So, by replacing your resistor with a MOSFET, you can actually control the output frequency. So, I can write it as,

$$f_{osc} \propto -V_{ctrl}$$

under the approximation that you need to have a limit on the control voltage so that you can use the transistor in linear region.

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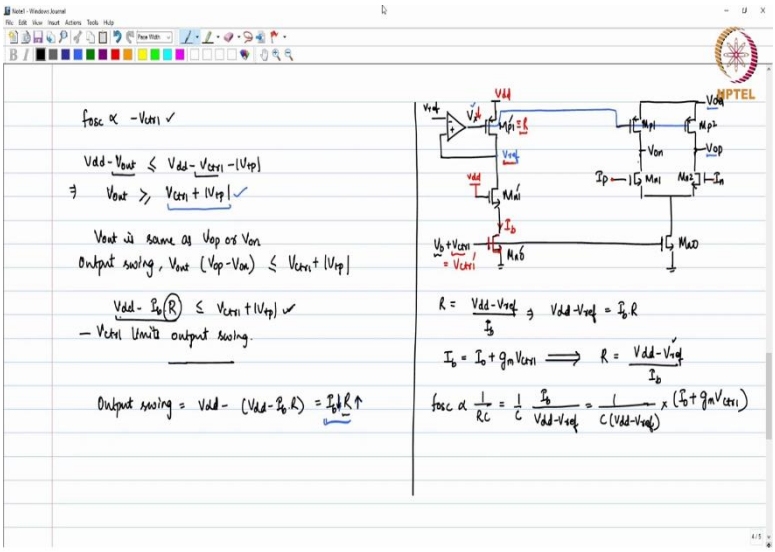

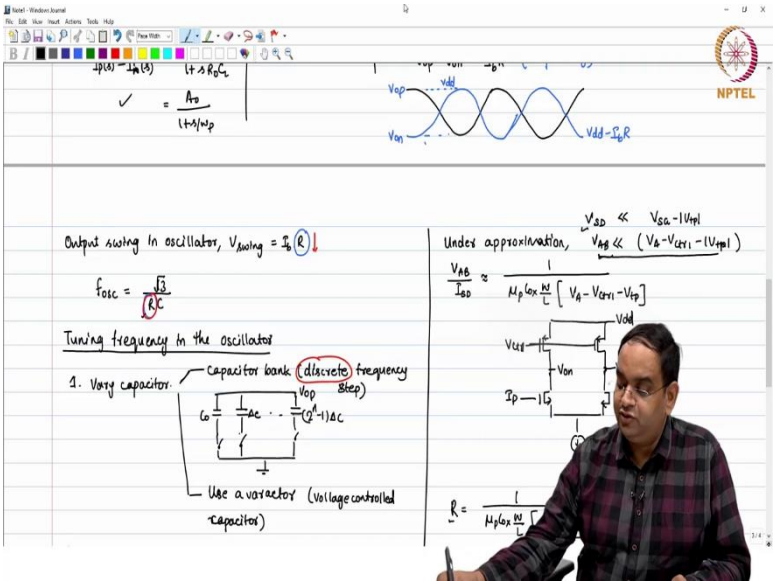

So, now let us see that what is that limit. So, the first thing is $f_{osc} \propto -V_{ctrl}$. This is a good thing that you can vary the control voltage and you can vary the output frequency. The other thing is that you have a limit and the limit says that for linear region,

$$VDD - V_{out} \leq VDD - V_{ctrl} - |V_{tp}|$$

So, when your gate overdrive is larger than your source to drain voltage, at that time you are going to have this. So, you get,

$$V_{out} \geq V_{ctrl} + |V_{tp}|$$

Now this is important that you see V_{out} is same as V_{op} or V_{on}. So, you come back here and you see that there is a lower limit on V_{op} and V_{on} as per our condition here and what happens when we have a swing?

One of the nodes goes to VDD and the other node swings down which means whatever is the lower limit on your V_{op} and V_{on}, that is going to limit your output swing. So, this particular voltage appears to be the limit for our output swing. So, I can just write output swing as,

$$V_{out} = V_{op} - V_{on} \leq V_{ctrl} + |V_{tp}|$$

So, your output swing cannot be anything greater than that.

There is a limit but surely that is depending on your bias voltage, you can always have that because we also know that this output swing is given by $VDD - I_b R_{on}$. It is not that you can have only one value of the bias voltage or you can have one value of the bias current but you

can have a range of bias current as desired. So, V_{ctrl} controls the output frequency, V_{ctrl} limits the output swing. So, if I just need to write it, V_{ctrl} also limits output swing.

Now come back to the problem that our output swing which was $I_b R$ and R becomes a function of frequency, so our swing is actually a function of frequency. That problem is not yet resolved because even if I take, this is just an upper limit but output swing is a function of R and output frequency is also a function of R. So, we will address this problem in a moment. So, if we look at it, our oscillator, we will look only at one particular cell of our oscillator.

So, what we have here is that V_{ctrl} controls the output resistor and thereby controlling the output frequency. So, what we need to do is if we want to have our output swing, output swing is $VDD - (VDD - I_b R) = I_b R$. This is what we have, so if our R varies for the frequency, we have to vary I_b in the opposite direction.

So, if R increases to reduce the frequency, then we should reduce I_b such that the output swing remains fixed. So, what we are going to do is that the control voltage, we want to fix the output swing, so, what we will do is that the control voltage which we want to have, is generated in such a manner that the current is as desired. So, this is our MOS transistor for the resistance. Let me just name this also. So, this is M_{n1}, this is M_{n2}, M_{p1} and M_{p2}.

So, here if I want to keep a fixed output swing, what I am going to do is I will give this as a reference voltage. This is, let us say, V_x. So, what we are going to do is that this load resistor, we are going to decide the load resistor, control load resistor gate voltage in such a way that the current through the load resistor and the load resistance value itself, that product remains fixed. That is what we want to do that if the resistance increases, I_b reduces such that $I_b R$ remains same.

So, think about it that you just took a copy of this PMOS transistor here and you generated the gate voltage in such a way that if I have, just as an example, if I have let us say I_b current here, then this voltage because this PMOS is in feedback, this I_b current, this voltage will always be equal to V_{ref}. If I increase I_b current, then what will happen? If I increase I_b current, V_x potential will drop but V_{ref} will become same. So, what I am doing is if I_b increases, I actually reduce the effective resistance value of this PMOS. That is how we can get the gate voltage of the MOSFET which is used as a resistor. So, we will use this particular logic with the replica of the cell.

So, the top transistor is a replica of M_{p1}, so I will write M_{p1}', this transistor is a replica of M_{n1}, so M_{n1}', and then you have a current source. So, in place of the current source, I am replacing with the current source transistor with bias V_b and other thing is when will all the current shift to one of the branches, when either of these potentials in our case will go to VDD.

So, I am going to connect this to VDD. Now, if there is a current I_b here, for I_b current, I will get the equivalent resistance value for this transistor M_p such that this voltage remains V_{ref}. So, I can also write here that effective resistance value for this is given by,

$$R = \frac{VDD - V_{ref}}{I_b}$$

Or if you want to say it the other way, then, we have,

$$VDD - V_{ref} = I_b R$$

So, what we are going to do, we are going to pass this V_X voltage, the V_X voltage which you are seeing here, this voltage is passed as a gate voltage to our load resistors in the actual cell, to all the cells we will give that, and here you can have the same NMOS transistor to control the bias current.

So, you can do this. Now, you can ask a question, well, what I have done is I have actually fixed the resistance value or I decide now the resistance value in this delay cell in my oscillator such that the bias current times the resistance remains fixed so my amplitude or output swing is fixed but how am I going to control this frequency. Well, frequency control you can do by changing this from bias voltage as you can say bias voltage plus some V_{ctrl}.

This is fixed part you can say and this is varying part. So, overall if you want to write it, you can say, this is like $V_{ctrl}{}'$. So, by varying the gate voltage here, I am going to vary the current in this and as I vary the current in this, the resistance will vary and as the resistance varies, then my output frequency will also vary.

So, let us just look at that relation. So, I will write,

$$I_b = I_0 + g_m V_{ctrl}$$

This implies that resistance is given by,

$$R = \frac{VDD - V_{ref}}{I_b}$$

V_{ref} is external voltage which you gave, VDD is fixed, V_{ref} is fixed. The frequency of oscillation is given by,

$$f_{osc} \propto \frac{1}{RC} = \frac{1}{C}\frac{I_b}{VDD - V_{ref}} = \frac{1}{C(VDD - V_{ref})} \times (I_0 + g_m V_{ctrl})$$

So, it is not a problem whether f_{osc} is proportional to $-V_{ctrl}$ or V_{ctrl}. That is only going to change the sign but here the thing is that all these terms which you are seeing here, $\frac{1}{C}$, VDD, V_{ref}, I_0, all these terms are constant. There is only one variable term for the frequency.

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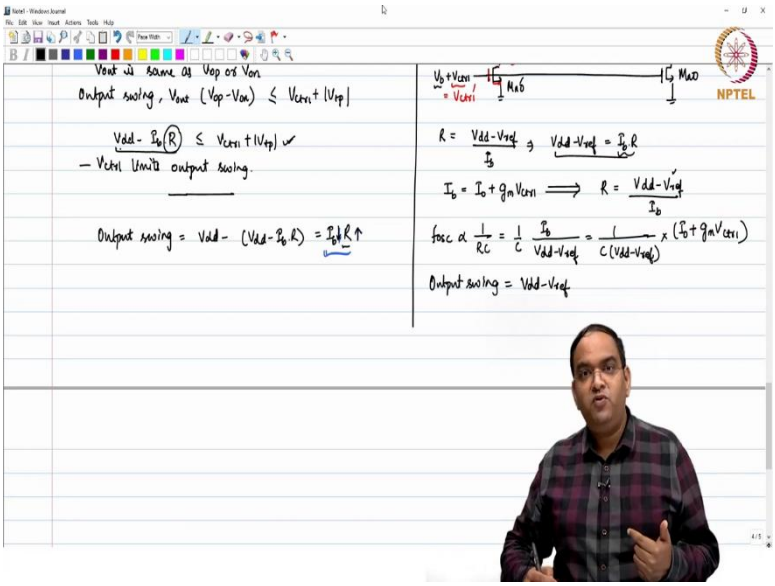

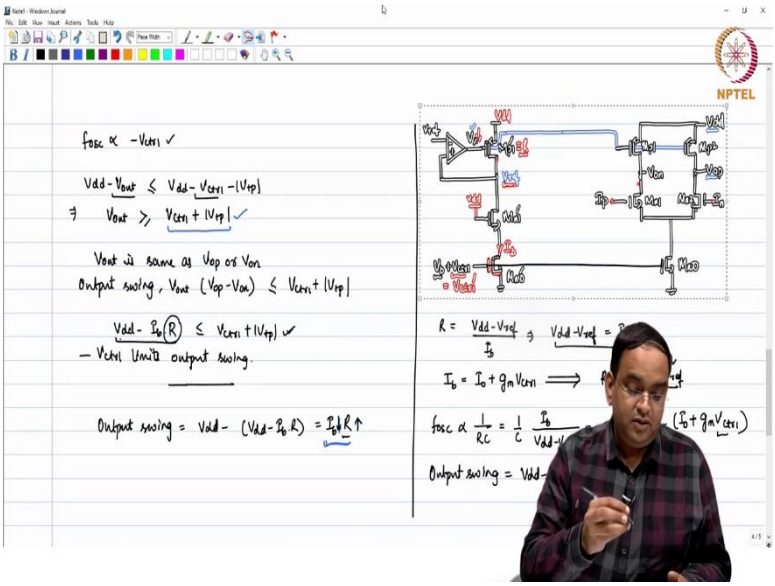

The output swing is given by,

$$V_{swing} = I_b R$$

$I_b R$ is fixed and equal to $VDD - V_{ref}$. So, now you have an oscillator whose output swing does not vary with the output frequency and you can vary the output frequency by applying a control voltage here. Now, well, when you are going to design with the transistors like this, you will see that this transistor M_{n0}, the non-linearity of this transistor will affect your frequency gain with respect to the control voltage.

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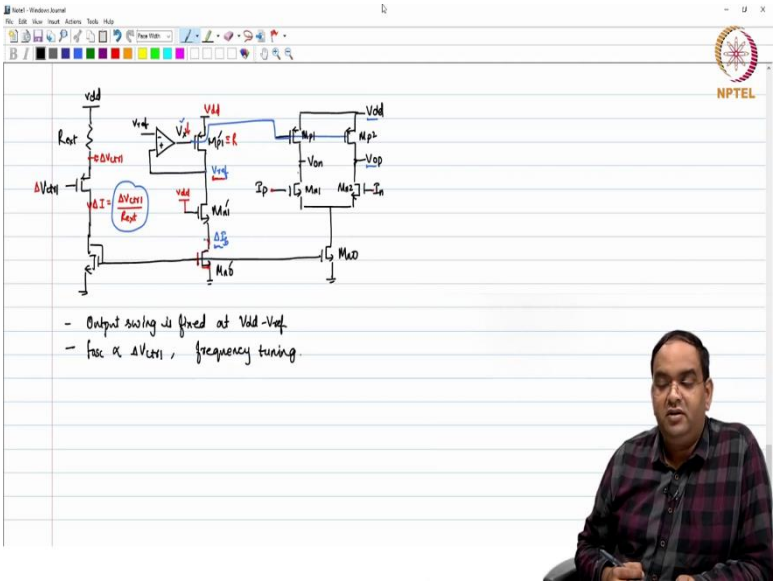

So, if that is the case, what you can do is the following, you want to have the change in the current linearly related to the control voltage rather than using g_m because g_m will depend on the control voltage itself, that is the non-linearity which we are talking about. So, if that is the case, what we can do is we can linearize our current gain from V_{ctrl} using source degeneration and how we do it, well, we can have an extra poly resistor or an extra resistor here. Let us call this as R_{ext} for a while and you have a PMOS and you can have a PMOS with a diode connected NMOS at the bottom.

So, now here you give V_{ctrl}. So, what happens is when you change V_{ctrl} with ΔV_{ctrl} here because it is a source follower with respect to PMOS, so, you get roughly ΔV_{ctrl}, approximately ΔV_{ctrl} change at the output node. With respect to that, the change in the current ΔI is going to be $\frac{\Delta V_{ctrl}}{R_{ext}}$ and this changed current value gets replicated in the changed bias current here, ΔI_b, and for the changed bias current, you have a change in the resistance value and you change the output frequency.

So, this is still connected, this connection still remains the same. So, what we have achieved in our above configuration is output swing is fixed at $VDD - V_{ref}$ and output frequency is directly

proportional to V_{ctrl} as we have or you can call this as ΔV_{ctrl}, and you can have frequency, this is nothing but output frequency proportional to ΔV_{ctrl} is frequency tuning. So, depending on how much control voltage you are using or what control voltage do you use, based on that you can change the output frequency. Thank you.