Phase-Locked Loops
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Lecture – 35
Noise Simulations for CP-PLL Blocks

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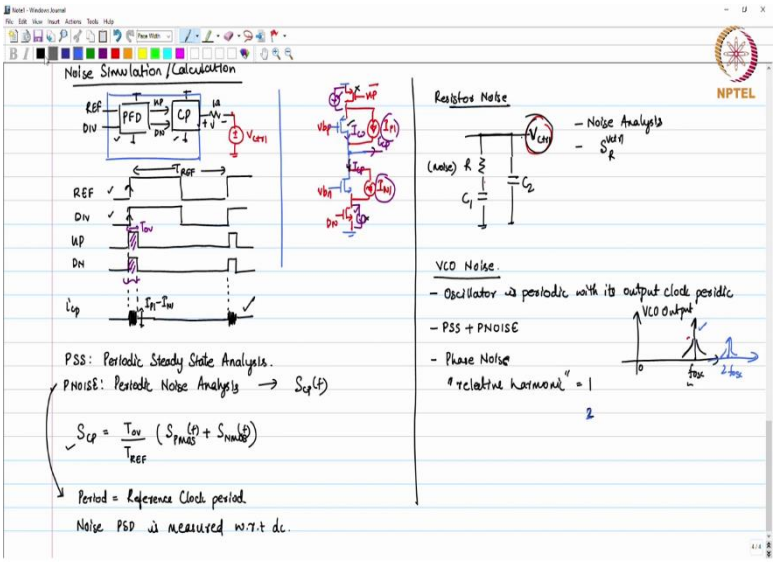

Hello, welcome to this session. In the previous session, we looked at the noise optimization for different noise sources in the PLL. In this session, we are going to find out the noise of different sources either by calculation or by simulation. So, in our PLL block, we have PFD and charge-pump. So, let me just write this is noise simulation or calculation depending on which is easier to do. So, we have PFD plus charge-pump and we know that the output of the charge-pump is current i_{cp}. This is your reference clock and then you have divided clock.

So, first thing to understand is the following. Well, both of them are connected to VDD and ground. That this PFD plus charge-pump block together, it is clocked at reference, reference is a fixed clock. So, this is like we have seen this earlier, it is like a periodic system, it is sampled at reference frequency. Then in the locked state of the PLL, if you are using a Type-II PLL, then ideally your reference and your divided clock will be aligned, it will be perfectly aligned with zero phase offset.

If that happens, then the UP and DN pulses which you are seeing here, these UP and DN pulses will have zero error and they will be ON only during the overlap time for this reference and divided clock. So, UP and DN will have the pulses like this, this is locked state when there is zero phase error and which it will be if there are no other non-idealities in the system.

Now, what happens is that in the charge-pump, the model which we have chosen so far is that you have a current source, forget about how these UP and DN are going to be interfaced in the end, but you have current sources, both top and bottom and these are the switches and these current sources are also realized using MOSFETs by the way. So, you will have a MOS current source like this, another MOS current source like this, and these are the current sources.

And the switches we have here, we will use MOS kind of switches. So, you have MOS switches here and you have MOS switches here. This is a very simplified model of the charge-pump. Now, this is $\overline{UP}$ and this is DN, these are your bias potentials v_{bp} and v_{bn}. Now, consider the case when $\overline{UP}$, here UP is high for this much time and DN is high for this much time which means during this time T_{ov} or T_{RST}, I will call, this is T_{ov} here.

So, during this T_{ov} time, what is going to happen, this switch, this switch is ON, this is also ON and the desired current will flow from top to bottom. Ideally, this is same I_{CP} and no current comes out of the charge-pump. But when you have a MOSFET, it comes with its noise current also. We have seen some kind of modeling. So, with respect to the charge-pump, you get the noise current and each MOSFET will have its own noise current. So, I can call this as I_{P1}, this is I_{N1}. By the way, your switches will also have equivalent noise current like this.

The noise current density is same for the same current but at any given instant of time, the noise current, the exact value of I_{P1} will be different from I_{N1}. So, if I consider the noise for the switches, let us not, it will become complicated, let us not consider the noise for the switches but noise only for the current sources.

So, you have I_{P1} coming from top and I_{N1} going to the bottom, so, the difference will flow as noise. So, the difference current I_{P1}- I_{N1}, what is the current value? Because this is random, so I am just creating some kind of disturbance here. This current at any given time is going to be I_{P1}- I_{N1}. So, this noise current will flow. What we need to do is we need to find the noise spectral density for this current.

So, the method which we widely adopt is you simulate your PFD plus charge-pump together, you feed the same pulses, reference and divided, so that there is zero phase error. This is your reference clock period and the simulation will be done with the help of PSS analysis which is Periodic Steady State analysis.

So, what it does is because we know this system is clocked at reference, it is periodic with respect to reference. So, when you have a sampled system, the noise conversion will happen

from different harmonics of the sampling clock to your output. So, when you apply any change to the system, because it is periodic, so, you will have frequency transformations there. So, this is periodic steady state analysis, this is a simulation which you will do, periodic steady state analysis and then you can do PNOISE analysis, which is a noise analysis for periodic system, so this is Periodic Noise Analysis.

When you do such analysis, what will you find? You do such analysis and you find the output current. How will you find the output current? If I know that during regular operation of the PLL, there is some desired voltage which I would like to have at the output at control voltage. So, I will just give that as a control voltage source so that my charge-pump is terminated with the same voltage as it will be terminated in the PLL and I can find i_{cp}.

Sometimes you may not be able to find i_{cp} directly. So, what you can do is you can insert a resistor here, resistor of 1Ω, let us say, and the resistor is noiseless and you measure the voltage across this resistor. So, if you measure the voltage across 1Ω resistor, the current, you know $V = IR$. So, whatever voltage you have, that is actually the noise current, you can change the units later. So, this is the way we can simulate for the combined noise of PFD and charge-pump.

Interestingly, you can also calculate after doing a lot of math, you can find that the noise spectral density of the charge-pump which is the spectral density of this waveform is given by,

$$S_{CP} = \frac{T_{ov}}{T_{REF}}\left(S_{PMOS}(f) + S_{NMOS}(f)\right)$$

So, you can verify your simulations after doing PSS and PNOISE which gives us i_{cp} noise or from here charge-pump noise. You can verify these things with your mathematical calculations. So, that is going to give you PFD plus charge-pump noise.

Similarly, if you want to find the divider noise, again you take help of PSS and PNOISE analysis and find the divider noise. One important thing here is when you are doing PNOISE analysis, it is done at the reference frequency. So, you have to provide what is the periodicity or beat period in the system, that period is your reference period for the analysis, Reference Clock Period, that is what you can tell the simulator.

Then the other thing is when you are doing the PNOISE analysis, it will also be asked during the process of the simulation that do you want to measure the noise with respect to dc, with respect to reference or with respect to second harmonic of reference or third harmonic or so on.

So, there it is like noise PSD Power Spectral Density is measured with respect to dc. You have options to measure with respect to the fundamental of the beat frequency which is your reference frequency or second harmonic or third harmonic or so on, but you are measuring with respect to dc, that is what we need here. So, this is normally you can, depending on which simulator you are using, you can define it as absolute or relative. So, here it is absolute, we need with respect to dc.

Now, the resistor noise is very simple because that is $4kTR$. You do not have to do any simulation for that, but if you still want, you can simulate for the resistor noise. So, for resistor noise, what we have been doing is, earlier, you have the resistor, you will look at these capacitors C_1 and C_2, you can do the noise analysis only for this. These are passive components, so, the voltage here does not matter. You will find what is V, voltage at this node.

Let me name it as the same node, so, V_{ctrl}. You find V_{ctrl}. If the resistor is noisy, you do noise analysis and noise analysis will give you the output, this voltage. So, this is the filtered value of your noise control voltage, you will get that directly. So, this is due to resistor but at V_{ctrl} node, you can find that out. And then you can use this with correct transfer function because right now if I am finding the noise at this node, then the transfer function is not the same if I am modeling it here. So, please keep that in mind.

Then you have the other important noise source which is VCO. Well, VCO is going to be our next topic of discussion, but the only thing which is important here is VCO or an oscillator, it is periodic, oscillator is periodic with its output period. You cannot say that this is periodic with the reference frequency because a standalone oscillator is periodic with its output clock period.

So, since it is periodic in nature, you will again do PSS plus PNOISE analysis and when you are doing PSS plus PNOISE analysis, just remember that the VCO is oscillating at certain frequency, f_{osc}, this is the spectrum of the VCO output, the noise which we are looking is like this, this is the noise which we are interested in.

So, you look for the output phase noise, you will have options to find the phase noise and that phase noise is found in PNOISE analysis, one harmonic to the beat frequency, relative harmonic = 1. This is important here because when we are simulating for the oscillator in periodic using PSS analysis, it is periodic with the oscillation period and the noise which we are looking at is the noise here, this noise.

It will be given to you whether you want to have upper sideband, lower sideband or something else. I think that we will understand better when we are with the simulator but the important part here is that the noise which we are looking at is relative to the output frequency. We are not looking from dc to higher frequency, we are looking from relative to this frequency. It is φ_{out}, it is measured with respect to the output period. We have been using that, right now we are just translating that to simulations.

So, for that, you will be asked that what noise you want, whether it is absolute, absolute means 0 to higher, from dc to higher frequency, or relative. When you say relative harmonic 1, that means with respect to f_{osc}, if by chance you happen to give relative harmonic 2, it is not going to be this, it is going to be with your second harmonic. That is not what we are interested in, we are interested in the noise at the fundamental.

So, in this way, you can simulate for the VCO noise. So, PFD plus charge-pump combined output noise at the charge-pump output, resistor noise is coming with the help of a filter and then you have VCO noise. Divider noise also you can measure in the same way, it is also a periodic system. So, you will get that. So, in this way, you can calculate the noise spectral density of different noise sources and later you use it with the noise transfer function for bandwidth optimization for the desired amount of jitter. Thank you.