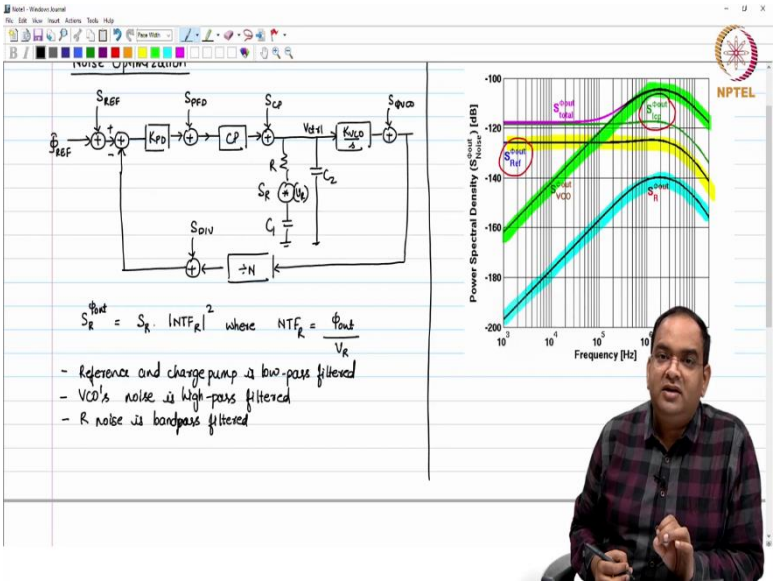
Phase-Locked Loops
Dr. Saurabh Saxena
Department of Electrical Engineering
Indian Institute of Technology Madras

Lecture – 34
Noise Analysis in CP-PLL: Part III

(Refer Slide Time: 00:15)



Hello everyone. Welcome to this session. In the previous session, we looked at how to calculate the noise at the output of the PLL. So, today, in this session, we will look at the noise optimization with respect to bandwidth of the PLL. So, before I start with the noise optimization, let us just have a quick recap of the noise in the PLL. So, I will just draw the small signal block diagram for the different noise sources which we have seen earlier.

So, here you have φ_{REF}, then the noise gets added up for the reference and you have feedback at the input, then you have PFD plus charge-pump. So, I have treated PFD noise separate and charge-pump noise separate. You can take it together also. So, this is S_{PFD} and then you have charge-pump whose output is current. So, the noise which is added at the output of the charge-pump is current noise actually, so this is S_{CP}. Here, S is referring to the noise spectral density.

Then you have the resistor with a noise source V_n^R and noise spectral density S_R. So, let me just write noise spectral density as S_R followed by a capacitor C_1 and then you have capacitor C_2, this is R followed by VCO with gain $\frac{K_{VCO}}{s}$. The noise added by the VCO is in terms of phase which is φ_{VCO} and this is V_{ctrl} voltage node and you feed this signal back to the frequency divider.

So, you have the $\div N$ here, you add the noise, the output of the divider in terms of phase and this feeds back. So, this was the small signal model of the noise in the PLL and we were analyzing this noise with the noise transfer functions for the PLL. So, let us just bring the plot where we were looking at the output noise spectral density with respect to the input noise spectral density.

So, this is the noise plot which we were looking at the output of the PLL. So, what we are plotting here is just to recall, we have,

$$S_R^{\varphi_{OUT}} = S_R \times |NTF_R|^2$$

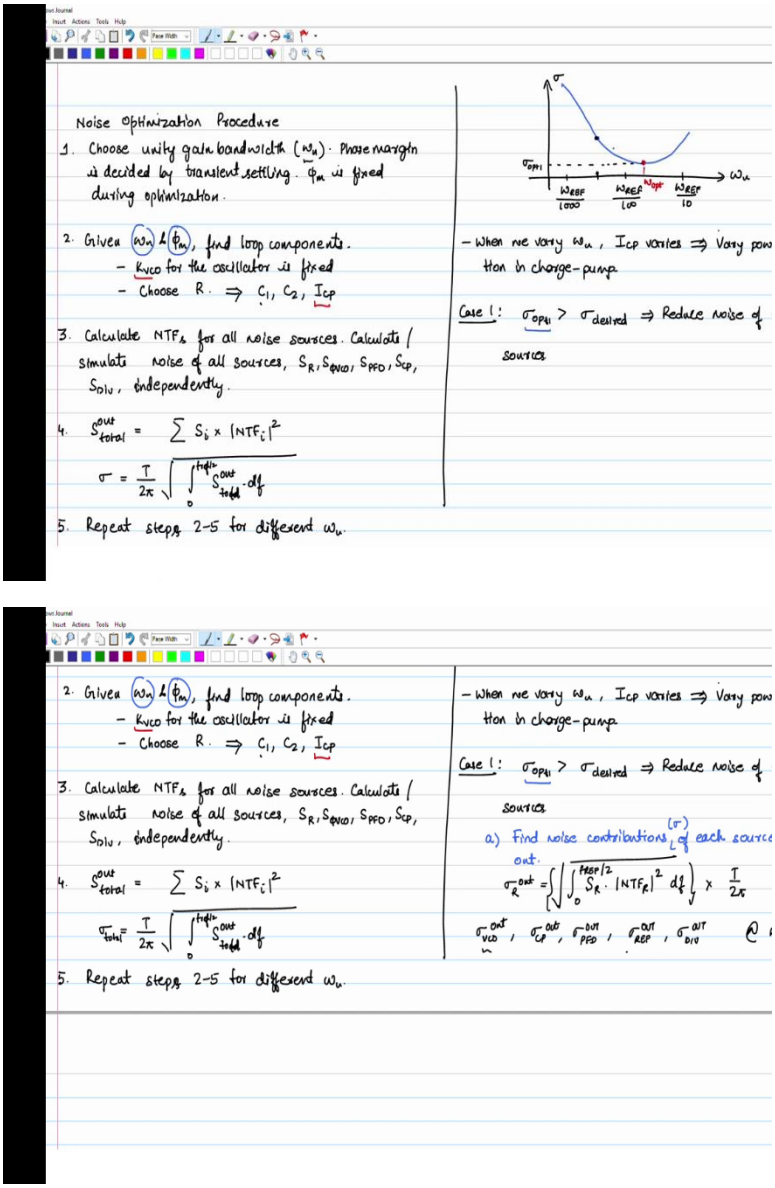
where, $NTF_R = \frac{\varphi_{OUT}}{V_n^R}$ and this V_n^R is the equivalent noise voltage for the resistor. So, we are plotting the output noise spectral densities. The important thing which we would like to highlight is the following that your $S_{REF}^{\varphi_{OUT}}$ and $S_{CP}^{\varphi_{OUT}}$ are actually low pass filtered. So, reference noise and charge-pump noise are low pass filtered. Why do I say low pass filtered? Well, you see the transfer function which we are having is flat from dc and then it drops, so this is low pass filtered.

Second, you look at the VCO noise. So, the VCO noise is actually high pass filtered and if you look at it, it is like this and what you are seeing at the higher frequencies is because of the noise profile itself. So, VCO noise is high pass filtered and then you have resistance noise. The input noise for the resistance is actually flat and the output noise what you see is low value at lower frequency and low value at the higher frequency and in between it peaks. So, the resistor noise is a bandpass filtered.

So, now you think about it that if I have multiple noise sources in the system and all the noise sources are not filtered by the same filter. It is like if all the noise sources were getting filtered by a low pass filter, then we can very well say that it is better to choose a lower bandwidth for the low pass filter to minimize the output noise.

Similarly, if all the noise sources in the PLL block were filtered by high pass filter, then it would be better that we choose a larger bandwidth for the high pass filter, so that we filter out the output noise. Now, here there are some noise sources which are low pass filtered, some noise sources which are high pass filtered. So, without calculating or without finding either by simulation or by calculation the noise for a given bandwidth, you cannot say whether that particular bandwidth which you are choosing is optimizing the noise or not.

(Refer Slide Time: 07:00)



So, for that particular reason, what you need to do is the following. So, the noise optimization procedure starts like this. So, let me just write it, this is noise optimization procedure. So, to begin with, you choose some bandwidth, choose unity gain bandwidth which you would like for the PLL, ω_u, and let us say that phase margin which you want is decided by transient settling so that is already a number which you have picked up. You need to find which is the optimum ω_u, phase margin is decided by transient settling and that is already given, you can assume that, either given or you have already chosen. So, phase margin is fixed during the optimization.

So, when I pick up ω_u, so for given ω_u and φ_m, find loop components with the same procedure which we saw earlier that the phase plot at the unity gain frequency should be maximally flat, that is derivative of phase is equal to zero. So, using that, we will find the loop components.

Now, when we find the loop components, few things we have assumed or we chose and few things will be given for the design. So, what will be given for the design? K_{VCO} for the oscillator is fixed. So, this whole optimization procedure is at system level and circuit level iteratively.

So, we design an oscillator, we find the oscillator phase noise, independent oscillator phase noise and the K_{VCO} for the oscillator is fixed, you have to choose R in these calculations because we have seen that for the loop gain and the phase margin we want, you have to make a choice on R. Only when you choose R and K_{VCO} is given, then only you will find C_1, C_2 and I_{CP} such that you get the chosen ω_u and phase margin for the loop components and you know that the resistor is a noisy block. So, once you make a choice on R and you find that the overall noise does not meet your requirements, then you have to go back and change for R.

So, let us say we chose R here, we calculate C_1, C_2 and I_{CP}. Once your C_1, C_2 and I_{CP} are found out, then what are you going to do? Calculate noise transfer functions for all the noise sources. And you find noise of all sources independently, there are two options either you calculate or you simulate. So, you can do both the things. We will see what we are going to do but whichever way it is, you calculate or simulate noise of all sources independently.

So, what are we doing? When we are saying we calculate or simulate noise of all sources independently, we are actually calculating or we are finding S_R, $S_{\varphi_{VCO}}$, S_{PFD}, S_{CP}, S_{Div} and so on. These have to be found out.

Once you know the noise and the NTFs, you know that you can calculate the total output noise which is given by,

$$S_{Total}^{\varphi_{OUT}} = \sum S_i \times |NTF_i|^2$$

where, i denotes the i^{th} source.

So, whatever the noise components, you find this out and you then calculate the jitter which is given by,

$$\sigma_{total} = \frac{T}{2\pi}\sqrt{\int_0^{\frac{f_{ref}}{2}} S_{total}^{\varphi_{OUT}} df}$$

where, T is the output clock period. The integration goes from 0 to $\frac{f_{ref}}{2}$ in our calculations because it is a sampled system, so most of the time our simulations are going to be valid till $\frac{f_{ref}}{2}$ or our modeling is going to be valid till $\frac{f_{ref}}{2}$.

So, now you started with one particular ω_u and phase margin and what you got is the jitter value. So, you pick up that jitter and you plot it. So, I am going to plot jitter versus ω_u. So, I picked up one particular frequency ω_u and I got a certain value of jitter, you need to repeat this exercise, repeat steps 2 to 5 for different ω_u.

Now, this depends on what ω_u you prefer or which is going to give you noise optimization, ω_u. So, you keep, normally you can vary from, this is just an example, you can vary from $\frac{\omega_{ref}}{10}$ because till that point our modeling is valid and maybe you can go upto $\frac{\omega_{ref}}{100}$ or $\frac{\omega_{ref}}{1000}$, that just depends. So, we are doing all these things at system level. So, you keep on doing this, $\frac{\omega_{ref}}{10}$ to $\frac{\omega_{ref}}{100}$. So, let us say, I pick up one value, this is $\frac{\omega_{ref}}{100}$.

So, when I am going to find and I am repeating this exercise, each of these unity gain frequencies is going to give me some amount of jitter. What you are going to find that this particular plot may look like this, it can be anything. So, the only thing is, it may have some peak point or it may not have that optimum point. So, the way I have shown you the plot, you see that there exists a point where the noise is optimum.

So, in this particular case, as soon as we chose K_{VCO} and the phase noise of the oscillator, the power consumption in the oscillator is fixed. We got a certain I_{CP}, the power consumption in the charge-pump is also fixed and you are designing it for a PLL where your reference frequency and output frequencies are fixed, so the power consumption in all other blocks is also fixed.

The only thing is that when we vary ω_u, when we vary ω_u without making any changes to the reference or the output frequency, the only other block in which the power consumption will vary is I_{CP} varies and which in turn actually varies the power consumption in the charge-pump. So, only that power consumption will vary, rest all will remain same.

So, when we do this, we find certain ω_{opt}. Now the question arises whether the value of the jitter which you have, let us say, σ_{opt1}, whether this σ_{opt1} is lesser than your jitter requirements or it is larger than the jitter requirements.

So, depending on what we have. So, let us say, case one where $\sigma_{opt1} > \sigma_{desired}$ from the PLL, it can happen because without calculating everything, you do not know what jitter value you are going to have. So, if $\sigma_{opt1} > \sigma_{desired}$, then for the desired jitter value, you have to reduce the noise of components.

Now, if let us say, $\sigma_{opt1} = \sigma_{desired}$, then you can say equal or within the range very close that you can say that this is fine within the tolerable limits, you can go ahead and just confirm the values of C_1, C_2 and I_{CP} at σ_{opt} and your PLL design at system level is over. You can just plug in the components now and your PLL should work. But in case when $\sigma_{opt1} > \sigma_{desired}$, it is beyond the margin of error which you can tolerate for the desired output frequency, then what you have to do is, you have to go back and reduce the noise of the sources. If this happens, you have to reduce noise of the different sources.

Now, how will you reduce the noise of different sources? That is the question. Now, this PFD, charge-pump, PFD is working at the fixed reference rate. One thing is the noise contribution by the PFD is normally very less but it works at the fixed reference rate, you will not change the noise by designing it again. The only way it can be that you increase the sizes of transistors, you consume more current there but before we take a call that which particular component or which particular noise is dominating, do one thing here, find noise contributions of each source to the output.

For the noise contribution, I am looking for σ which particular component contributes more to the output. So, what we have found earlier is σ_{total}, what I am asking you to do is the following: you find σ^{out} due to resistor. So, if I just call this as σ_R^{out}, this is going to be,

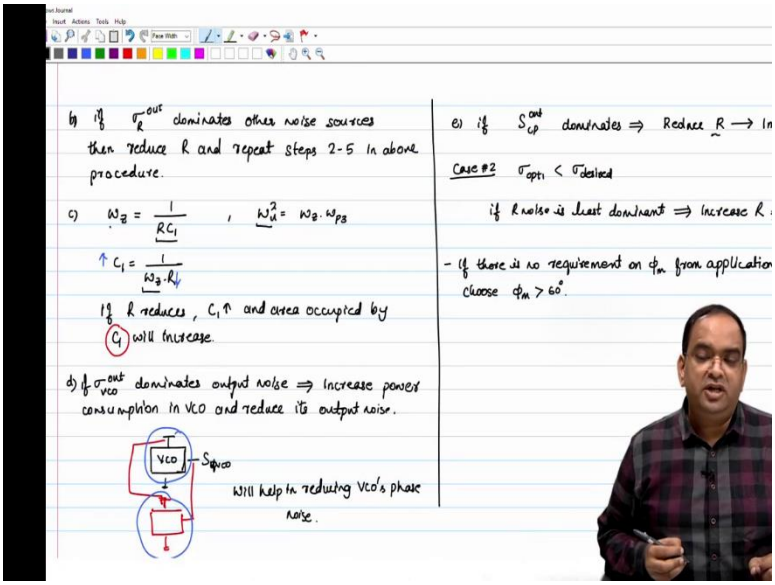
$$\sigma_R^{out} = \frac{T}{2\pi}\sqrt{\int_0^{\frac{f_{ref}}{2}} S_R.|NTF_R|^2 df}$$

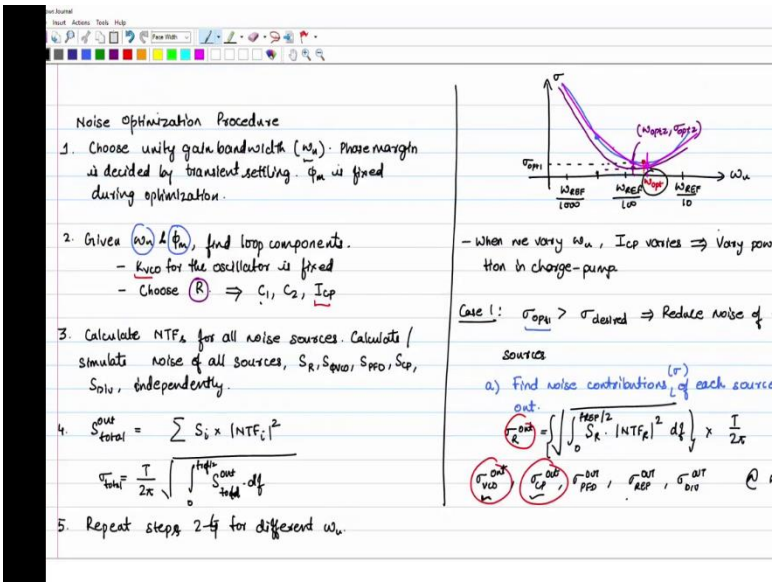
So, this is the jitter contribution by the resistor to the output. Similarly, I am going to find for all the components σ_{VCO}^{out}, σ_R^{out}already there, σ_{CP}^{out}, σ_{PFD}^{out}, σ_{REF}^{out} and σ_{Div}^{out}. And where I am going

to find for what ω_u? All these contributions I am going to find for ω_{opt} because that is the minimum jitter which I have in the system after choosing the noise from independent sources. So, I need to find out which of these components actually is contributing the most.

See, if you want to reduce the noise of any component, then you should know whether that noise is dominant or not. If it turns out that let us say the resistor noise is dominating because we chose the value of resistor randomly to begin with, just start designing, so, 1k 2k whatever you like, you can choose that and if it happens that the resistor noise is dominating, if you choose a large value of the resistor, resistor noise is going to dominate. If resistor noise dominates, then there is no point in addressing the noise in the VCO. So, we are going to find all these jitter contributions independently at $\omega_u = \omega_{opt1}$.

(Refer Slide Time: 22:53)





So, what we are going to do is once we find that, then we should look for these. If σ_R^{out} dominates other noise sources, then reduce R and repeat steps 2 to 5 in the above procedure. So, what it is going to do is if your resistor noise is dominating the output noise and you go ahead and you choose a different value of R, that means you are going to get different value of C_1 and C_2 and I_{CP}, you again go and plot the curve, it may happen that because you reduced the value of the resistor, so, resistor noise reduces.

So, maybe you get something kind of this, quite possible. What bandwidth? It again depends, so you get another value, which is σ_{opt2}, I can call this. σ_{opt2} and at different frequency which is ω_{opt2}. So, the coordinates will be $(\omega_{opt2}, \sigma_{opt2})$. If it meets your requirement, well and good.

It is like this, if it meets your requirement and it is below what you require, then you can think you can increase the resistor value and you may still be able to meet the requirements. If it is above, if $\sigma_{opt2} > \sigma_{desired}$, then you go ahead again and reduce the value of the resistor more and find the output noise. So, this is with respect to the resistor.

Now, the question you can always ask is that if the resistor noise is so important, it can dominate at any point of time, then why don't I use a low value of the resistor itself so that I make it noiseless. There is a trade-off between the value of the resistor and the area for the capacitor C_1. So, we have seen earlier that in the loop gain expression, $\omega_z = \frac{1}{RC_1}$ and $\omega_u^2 = \omega_z . \omega_{p3}$. We calculated all these values and it turns out to be that if for the desired phase margin, you have a fixed $\frac{C_1}{C_2}$ and you have a relationship between ω_u and ω_z in terms of $\frac{C_1}{C_2}$ which is independent of R.

So, as soon as we get ω_z and we need to find the exact value of C_1, the value of R matters. So, here, $C_1 = \frac{1}{\omega_z . R}$. So, what I am trying to tell you here is that for given ω_u and phase margin, your ω_z is fixed. So, if ω_z is fixed and you reduce the value of R, the value of C_1 will go up and if the value of C_1 goes up, then what happens is, if R reduces, C_1 will increase and area occupied by C_1 will increase which is a problem, problem in the sense how much area you are going to occupy on chip.

So, well, an IC is like a real estate, you keep on increasing the area, your cost will keep on increasing. So, there is a limit. We cannot just always start with the lower value of resistor to make it noise non-dominant or it is like should be always not noticeable. Well, there is a limit because of the area which we can afford for C_1. So, if your resistor noise dominates, you can

keep on changing the resistor value to a lower value iteratively such that you meet your requirements and you do not sacrifice the area more than required for the capacitor value, capacitor C_1. So, this is one case.

Now, the case which we have discussed is only with respect to R. Now, if you find that let us say other options because you can have multiple options here. If σ_{VCO}^{out} dominates, what to do? If σ_{VCO}^{out} dominates output noise and you still do not meet the requirements. In that case, well, the plot which I showed you earlier in this case actually, VCO noise dominates.

So, if VCO noise dominates, then the only option which you have is because you cannot change the reference frequency because that is fixed, and you cannot change the output frequency because the output frequency is something which you want and at ω_{opt} and σ_{opt}, it does not meet your requirement, then the only way is if this happens, increase power consumption in VCO and reduce its output noise. That is the only way. This is, well, given that the oscillator which you are using is one of the best designed oscillators. It is not a lousy oscillator for which you still have margin for improvement of noise.

So, to begin with, we designed an oscillator which is good and the only way to reduce the output noise of the oscillator what you will see is, the only way is you have to increase the power consumption and reduce the noise. So, you do that and you get the phase noise of the oscillator again, you go back again to your jitter versus σ plot, again do it, you may find that you meet your requirements. If you meet your requirements, well and good. If you do not meet your requirements, then you have to again increase the power consumption in the oscillator and reduce the output noise. So, that is something which we need to do when VCO noise dominates.

Now, in this case, I will tell you one trick which is often used. So, let us say, you have a VCO block and it gives you some output noise, phase noise which is something which we have been talking about. So, if I want to reduce the VCO noise, one of the easiest ways is that you take two copies of such oscillator and connect them node to node. Connect them node to node means each component of the original design and the oscillator is doubled.

So, if you do that, then what happens is you can think that each of these oscillators were oscillating independently earlier at the desired frequency and they will have the same noise. So, if I club them together, the oscillation frequency will not change, the power consumption will double and the phase noise will reduce by 3 dB. We will see the noise in the oscillator, the

relationship between the noise in the oscillator and the power consumption later but this is in general true that when you double the power consumption, your phase noise improves by 3 dB.

So, this will help in reducing VCO phase noise. So, I will do this if VCO noise dominates and then I can again calculate the jitter versus σ plot and if it is within the limits, good, if it is not, then I have to redo it. Then the next case is, let us say, if your charge-pump output noise dominates. What to do? If charge-pump output noise dominates, then the only option which you have before you is that you increase the charge-pump current, but if you increase the charge-pump current itself, then your unity gain bandwidth and everything will be different.

So, in that case, what you do is if charge-pump noise dominates, then you first reduce R. This will increase charge-pump current, this will increase I_{CP} and if it increases I_{CP}, charge-pump noise will reduce. So, well, as you reduce R, you have to recalculate all C_1, C_2 and everything. The charge-pump current is surely going to be larger and the charge-pump noise will be lesser. So, based on which noise is dominating your output noise, if you are not meeting the requirements, you can target that and you get the new jitter versus bandwidth plot such that you meet all the requirements.

So, finally, you may have, for example, if I do all such stuff, it may turn out that I get a plot something like this and this is the optimum bandwidth which I can pick, whichever is the optimum bandwidth for the desired jitter, you go and pick that particular value and then you will find all components C_1, C_2, I_{CP}, you plug in these components in your circuit design and hopefully the magic will happen and it will work.

Now, the case which we have listed here is when your jitter is more than the desired. Now, case 2 is when $\sigma_{opt1} < \sigma_{desired}$. So, what would you like to do? Would you like to just say I need let us say 2 picosecond of RMS jitter, I am getting 500 femtosecond of RMS jitter, well, it is within the margin, so, I would not do anything. Well, that will not be a good option because it is a trade-off in the design. If your jitter is lower, then by default you can think about it that your power consumption in the design is larger.

So, it is like I need 2 picoseconds, I am getting 500 femtoseconds. So, I am spending power for 500 femtoseconds but my requirement is not 500 femtoseconds, it is only 2 picoseconds. So, if I try to get 2 picoseconds of jitter, then I can reduce my power consumption. So, in that way, you can go ahead and find out, the way we have find out σ_{VCO} and all those things, you find here that which of these noise sources is least dominant.

So, reference is coming from outside, you have divider, you have PFD, charge-pump and so on. So, once you find which is least dominant, mostly it will be either R or VCO or charge-pump plus PFD. So, you find which one is least dominant and based on that you reduce the power consumption in the design.

So, let us say, if resistor noise is least dominant, if R noise is least dominant, then in that particular case, what do you do is you increase R. If you increase R, what will happen is I_{CP} will reduce. Since I_{CP}will reduce, C_1 will also reduce and if by reducing I_{CP}, your power consumption will actually reduce in the PLL and you can approach the $\sigma_{desired}$. You are actually increasing noise at the expense of lesser power consumption.

So, for a power optimized design for the desired jitter value, you have to do this iteratively till the time you meet your jitter requirements with minimum amount of power consumption. So, when it is lesser, you do this. When it is greater, we have discussed the steps. Finally, before you decide on the unity gain bandwidth and the jitter, you should check with these plots such that you get the best possible design for the PLL.

Now, an important part here is regarding the phase margin. I told that comes from the transient simulations. If you do not have any requirement from the transient simulation, it is better to keep the phase margin above 60° across process corners, then you will see I will start with phase margin of let us say 70°.

So, if you start with phase margin of 70°, your C_1 will be quite large. So, it depends on the application, I will just write, if there is no requirement on phase margin from the application side, choose phase margin typically, this is just a rule of thumb which I am applying here, phase margin greater than 60° and then design your PLL.

Now, greater than 60°, you can say between 60° to 90°, there is a lot of range. Well, 60° to 90°, there is a lot of range but there will be some variation in phase margin across process corner. So, make sure that it is greater than 60° across process corner and then you will also see that based on the phase margin, the noise contribution also changes a bit. The ratio of $\frac{C_1}{C_2}$ will vary based on the phase margin which will change the noise transfer functions. So, you can calculate that.

So, once I know the other noise sources, I can make phase margin also as a variable if there is no requirements, maybe between 60° to 70°, 75° and see which is giving me a better output

noise. So, there will always be a trade-off, if you want a larger phase margin, your capacitor area will be large. So, that is something which you need to always keep in mind. Thank you.