Phase-Locked Loops
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Lecture – 32
Noise Analysis in CP-PLL: Part I

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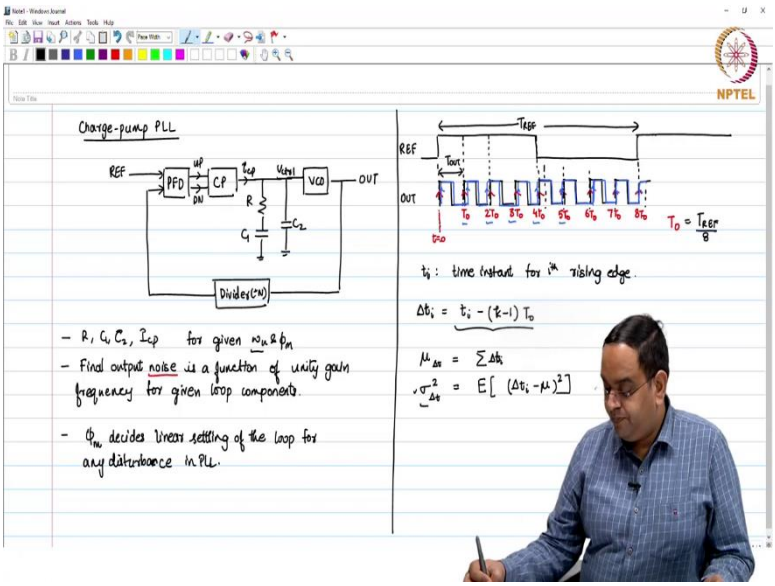

Hello everyone. Welcome to this session on noise in PLLs. So, earlier we actually found out the loop components of the PLL for a given unity gain frequency and bandwidth. So, let me just draw the PLL block diagram which we have been using. So, this is about charge-pump PLL and the block diagram which we have been using had a PFD followed by charge-pump. So, UP and DN signals here and this goes to the loop filter, the output of the loop filter controls the oscillator frequency and the oscillator output is fed to a clock frequency divider which divides the input frequency, divider I will write $\div N$ and it feeds back into the PFD. This has been our main PLL block or you can say a clock multiplier. So, here you have reference and here you have output, this is i_{cp} and this voltage is V_{ctrl}.

So, we actually found out the loop components R, C_1, C_2, I_{CP} earlier for given unity gain bandwidth, ω_u, and phase margin. A question arises that who decides ω_u and phase margin. So, if we want to have this PLL with minimum noise, the noise is actually a function of ω_u. So, I will first write final output noise, right now we do not know what is the meaning of noise, but give me a minute, final output noise is a function of unity gain frequency for given loop components.

So, if you choose a certain unity gain frequency, you can get R, C_1, C_2, I_{CP}. For those R, C_1, C_2, I_{CP} and your loop components, you will get some noise. If you vary the unity gain frequency, your output noise will vary. So, what guides our decision about unity gain frequency is the final output noise. So, we need to understand what this noise is here.

The phase margin also has a role to play and the phase margin actually decides the linear settling of the loop for any disturbance in the PLL loop. So, both of them will be decided based on the settling which we require and based on the noise limits which we have. So, let us try to understand the noise part first.

So, in case of these PLLs, we use a reference clock and we get an output clock. So, an ideal output clock, let us just say first our reference clock is like this and this is just an example. So, we feed in a clean reference clock whose period is fixed, ideally fixed. This is the kind of the reference clock which we feed in, and if we have our output clock which is 8 times the reference frequency. So, I will just plot that, if it happens to be 8 times the reference frequency, then our output clock will be like this. This will be our output clock and this clock is going to be repeated.

I just chose the same so that there is no problem. It appears that the size which I have taken is slightly away but that is okay, we can adjust that. This is hand drawn, so, it can be easily adjusted. So, these are our 4 clock cycles and then you can say all these 4, so, let me just make a slight change and let us do this, this is our T_{REF} and this is our output clock ideally. If you think about it, if this is my ideal clock, then our VCO period $T_{OUT} = \frac{T_{REF}}{8}$.

So, if I look at the time stamp of the rising edge of this output clock, then what I am going to get is these time instants will start with $t = 0$. This will be $t = T_{OUT}$, let us use o so that we can write it easily. This is going to be $2T_o$, this is $3T_o$, $4T_o$, $5T_o$, $6T_o$, $7T_o$, $8T_o$ and so on.

So, these are ideal time stamps of the rising edge of the clock. But what happens is that this rising edge of the output clock actually does not appear always at fixed time intervals. It may appear sometime after and by how much magnitude it will appear after, that is also random, sometimes it may appear before. So, you are going to see variation between the ideal and the real clock.

It can be any value. If it is in phase lock, then it will surely be limited, but it can take any value. Sometimes it may even fall upon the ideal time stamp. So, all these blue rising edges which I

am marking here, these are the rising edges of the real clock. Let me just draw on top of that the full clock. So, you may have something like this. It is perfectly normal that these things happen. By how much magnitude, that is still a random value here.

So, the difference between the actual rising edge and the ideal rising edge is something which we calculate. So let me just mark this t_i is the time instant for ith rising edge and the ideal rising edge you already know here. So, Δt_i is defined as follows:

$$\Delta t_i = t_i - (k-1)T_o$$

This is because your ideal time stamp is $k-1$ is 0, then T_o, $2T_o$, $3T_o$ and so on.

So, this is the variation in the actual rising edge and the ideal rising edge and this value Δt_i is actually random in nature and it depends on the noise in the system. What we require in our PLL is that this Δt_i should be as low as possible. Ideally, it should be 0, then you get a perfect clock. That is what you will get. So, we measure the performance of our PLL in terms of this Δt_i that how much variation do we have.

So, this is the variation in time domain. Then you define all the other parameters for this Δt_i. The mean value of Δt is defined as,

$$\mu_{\Delta t} = \sum \Delta t_i$$

If your system is locked, then mean value is going to be equal to 0. You also define the variance and the standard deviation for Δt. The variance for Δt is defined as,

$$\sigma_{\Delta t}^2 = \mathrm{E}[(\Delta t_i - \mu)^2]$$

This is the variance which you will have.

So, if we do not know the probability distribution function, what we do is you can you have a large number of samples, from those large number of samples, you calculate the standard deviation or the variance, $\sigma_{\Delta t}$ is the standard deviation and $\sigma_{\Delta t}^2$ is the variance.

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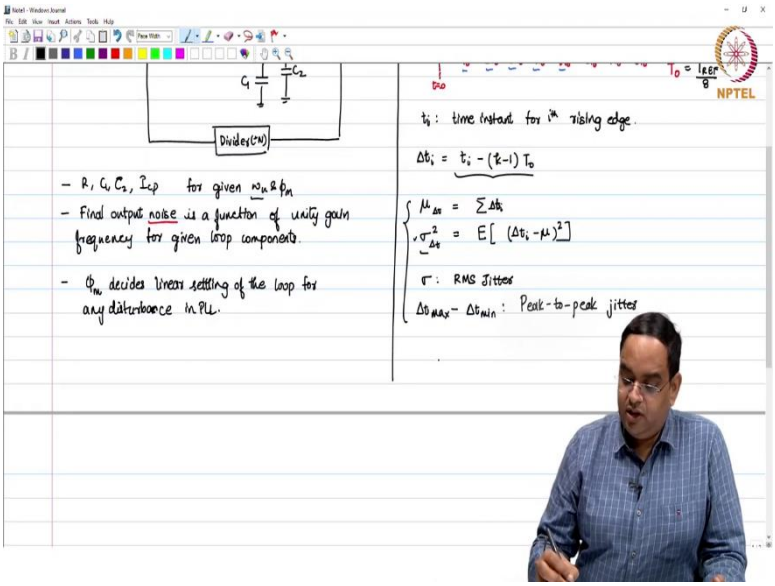

So, this value sigma is called as RMS Jitter. Then, $\Delta t_{max} - \Delta t_{min}$, it can have both positive and negative value, it leads to peak-to-peak variation or peak-to-peak jitter. So now, you see that because of noise in the system, we have the variation of the rising edge of the clock or the periodicity of the rising edge is susceptible to noise, and that variation is characterized by mean, standard deviation and peak-to-peak value and this is termed as jitter. So, jitter is the variation between the ideal rising edge and the actual rising edge of the clock. You can define it with the falling edge also but that is going to be the same.

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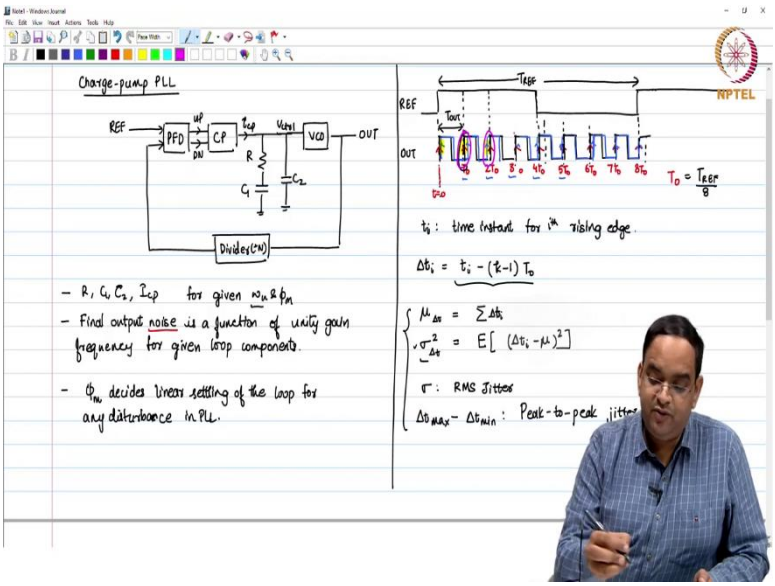

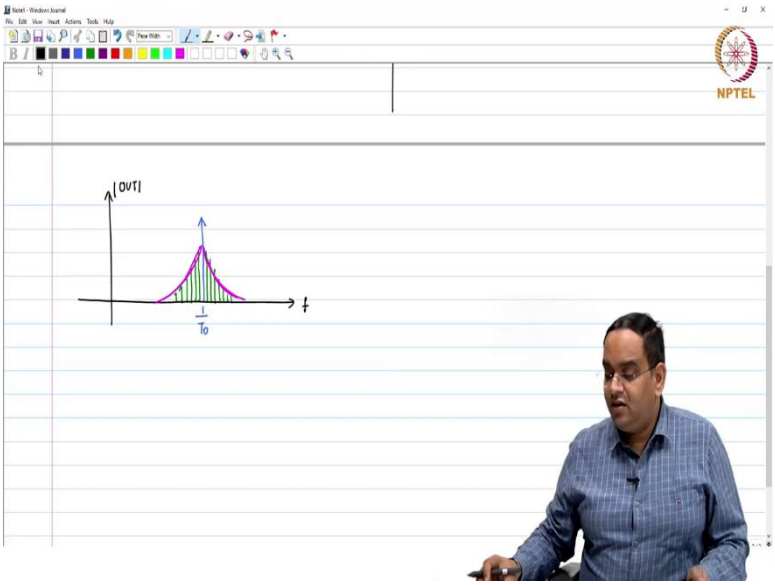

Now, this is what we see in the time domain. In phase domain, if you look at the spectrum of such a clock which has deviation, then what you will see in voltage spectrum? So, what I am going to do is I am looking at the voltage spectrum of the output with respect to the frequency. So, what you are going to see is you will see the tone at $\frac{1}{T_o}$ and then you see multiple tones around the output frequency. They are not like discrete tones, and you have the components at all the frequencies in general. So, this is what you will see. Effectively what we see is something like this characteristic for a noisy clock.

This characteristic for the noisy clock is coming because of the disturbances which we have just talked about. So, when we are taking the voltage spectrum, you are taking the output signal in time domain, and you are looking at the frequency spectrum of that output signal which is going to show you all the other tones which you observe.

If you want to understand further, you can think about it that these disturbances which you are seeing here, these disturbances, they are not very high frequency disturbances, they are relatively low frequency disturbances with respect to your clock and that is what you see as a kind of a skirt around the main tone. So, that is how you see the voltage spectrum.

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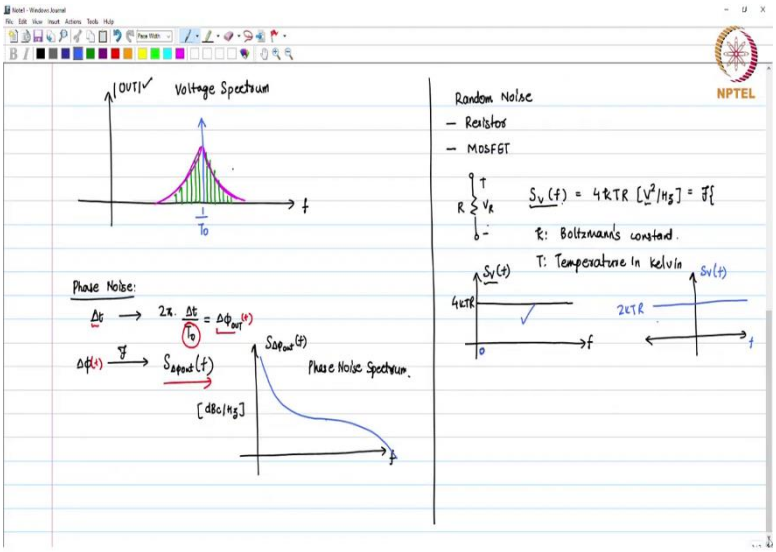

Then, there is another term which is defined as phase noise. So, what is this phase noise? We understand that your Δt variation in the rising edge or in the clock transition leads to phase error as defined by us earlier, which is $\frac{\Delta t}{T_o}$. Phase is always defined with respect to a clock period. We are looking at this Δt error at the output clock. We are defining the phase noise also with respect to the output clock.

So, this Δt leads to phase error $\Delta\varphi$. From $\Delta\varphi$, if you look at the frequency spectrum of $\Delta\varphi$, either you do Fourier or you do Laplace, the frequency spectrum of $\Delta\varphi$ is, I will just write it as, this is $\Delta\varphi_{OUT}$. So, this is $\Delta\varphi_{OUT}$, the frequency spectrum of $\Delta\varphi_{OUT}$ is normally used to specify the phase noise for a clock.

So, the spectrum $\Delta\varphi$ Fourier transform, if you look at that, this $\Delta\varphi$ Fourier transform, first thing is it is defined with respect to the output clock. So, $S_{\Delta\varphi_{OUT}}(f)$ with respect to f in case of PLLs, by the way, it may turn out to be something like this. It depends what it is but forget about the actual nature of the phase noise, the only thing which you remember is that the frequency spectrum is not constant and it is defined in units of dBc/Hz.

So, remember that phase noise is defined with respect to the clock. So, right now I am defining phase noise with respect to the output clock and with respect to that output clock, how is it calculated? You calculate $\Delta\varphi_{OUT}$ with respect to time domain and then from $\Delta\varphi(t)$, you use a Fourier transform to get the frequency spectrum.

By the way, both these things are related. This is by the way, a voltage spectrum. This is not the phase spectrum and this is your phase noise spectrum. So, the two are different, but these two are related, and then you will have different constants and gain factors when you relate both of these spectrums. So, the first thing is what we are interested in a clock is, at the end of the day, we are interested in this jitter value. What is this jitter $\sigma_{\Delta t}$ and what is the peak-to-peak jitter? The mean value we know when you are going to lock to a reference clock, mean value will be equal to 0 if you are using Type-II PLL.

So, that is what we have here with respect to the phase noise. Now, the question is who adds to this phase noise? Well, what we have said so far is that there is disturbance, the disturbance creates this noise. So, the two main elements which add random noise to our PLL are resistor and transistor. So, resistor contributes to the random noise and MOSFET or BJT whichever you are using, that also contributes to noise at the output. So, if you look at a simple resistor for the random noise, if this is a resistor R and you happen to measure the voltage across this resistor. It is not connected to any voltage, you will find that this voltage is varying. You are not connecting anything to the resistor, you just put your potentiometer, because of the noise in the resistor, you will measure some random voltage and the power spectral density of that voltage which you measure across the resistor is defined as,

$$S_v(f) = 4kTR \ \text{V}^2/\text{Hz}$$

where, k is the Boltzmann's constant, T is the temperature in Kelvin, and R is the resistance value.

So, the power spectral density of the noise measured across a resistor is actually flat. So, by the way, when I talk about $S_v(f)$, what I am actually doing is I am calculating the Fourier transform of your voltage, this is the power value. So, Fourier transform of your voltage measured across the resistor and in power terms, that is what we are measuring. So, $S_v(f)$ has units of V^2 and not V. If you just take the frequency spectrum of voltage, then you will see that you will have only Volts.

So, the way you measure it, you measure the Fourier spectrum of the autocorrelation of the voltage across the resistor because this is a random value. So that is what you measure. Now, what we do is that here this power spectral density is actually flat in nature. With the one-sided, it is $4kTR$, so, one-sided means from 0 to infinity. If you consider this noise as two-sided, it is a real signal. So, you know, if you have a real signal, you will have a symmetric Fourier

transform. Well, that symmetric Fourier transform will $S_v(f)$, this is both sided and this value will be $2kTR$. So, if you are considering noise of the resistor and you are always integrating only, you are looking at the noise only from 0 to f, then this is the correct one to use so that all the noise contribution is taken into account.

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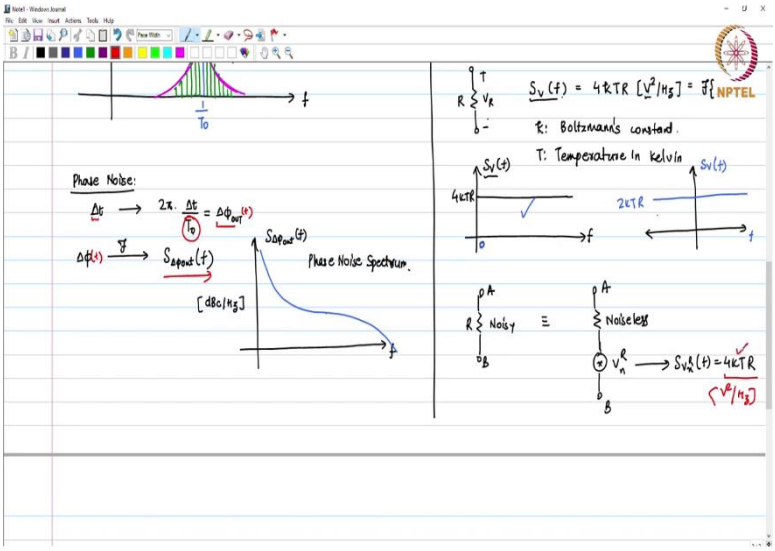

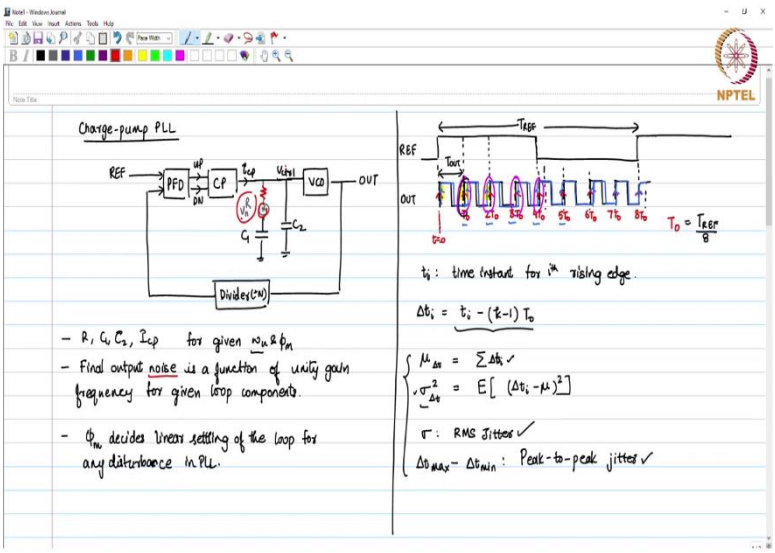

Now, you just think about it, a resistor appears to be noisy. So, what I can do is the following. I can, at any given time, I can mimic a noisy resistor, R, between two potentials A and B, this noisy resistor, to an equivalent of a noiseless resistor with a voltage source in series with it, A and B and I say this resistor is noiseless and there is a voltage V_n^R. This is V_n^R voltage source which we have here, there is no polarity to it because this is random signal whose power

spectral density $S_{V_n^R}(f) = 4kTR$. So, this is how we will model the noisy resistor with a noiseless resistor and a voltage source in series whose power spectral density of that voltage or the frequency spectrum of that noise power is $4kTR$ V^2/Hz.

So, this voltage which you are having is not a fixed voltage, its frequency spectrum has this spectral density. So now, even before we go and actually do the noise analysis for the PLL, we can just think about it that this resistor which was earlier noisy, I can have a noisy voltage in series with it.

So, let me just show you. You have a resistor which was earlier noisy, now noiseless and a voltage in series with it with noise voltage V_n^R. So, this noise voltage, now you think I have this resistor is noisy, there is an extra voltage here. So, this noise voltage is going to change the control voltage and if you change the control voltage, you will change the oscillator frequency and the output phase. So, that is what is going to happen.

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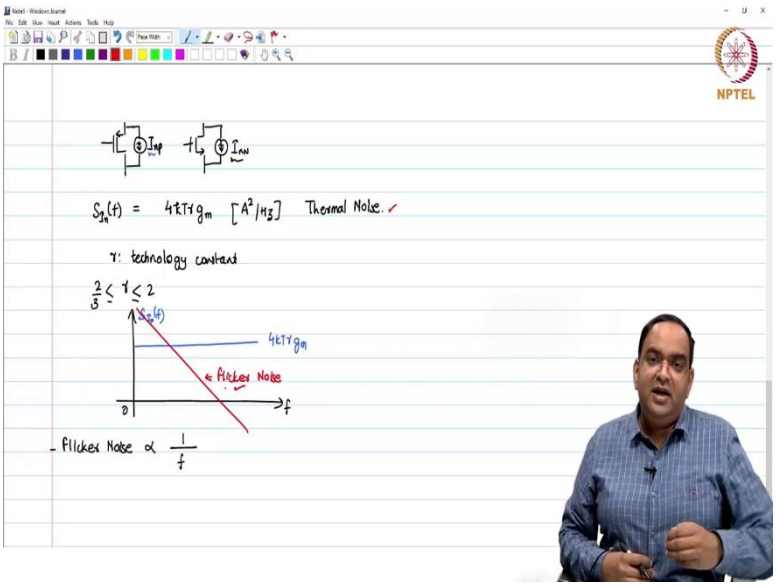

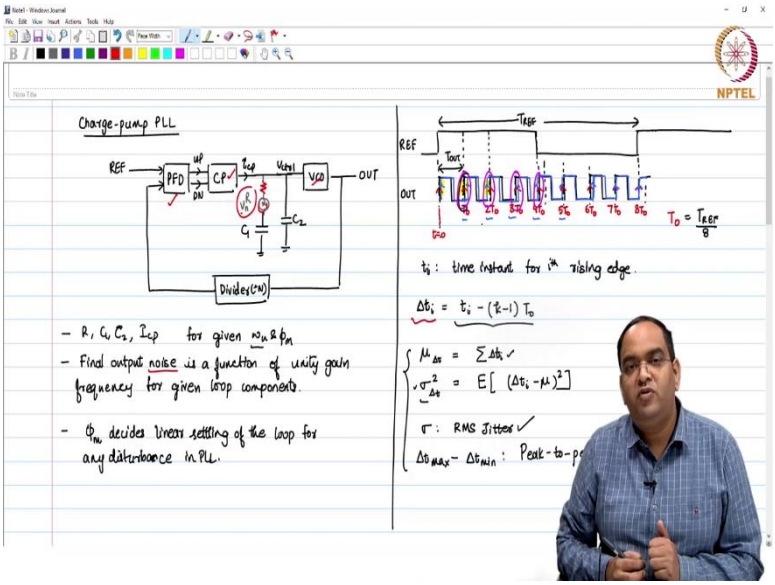

Similarly, as you see with respect to the resistor, you have noise coming from the MOSFET also. So, each MOSFET whether it is NMOS or it is PMOS or it is BJT which is NPN or PNP, noisy BJT or MOSFET can be replaced by a noiseless MOSFET and a noise current in parallel to the MOSFET. So, this is noise current I_{nP} and I_{nN} for PMOS and NMOS respectively. The frequency spectrum you can say or the spectral density $S_{I_n}(f) = 4kT\gamma g_m$ A^2/Hz, where k is the Boltzmann's constant, T is the temperature in Kelvin, γ is technology constant and $\frac{2}{3} \leq \gamma \leq 2$ depending on the transistor length and other parameters. So, if you look at the power spectral density of the noise current in frequency one-sided, that is going to be $4kT\gamma g_m$.

This $I_n(f)$ is the thermal noise because of the thermal noise of the transistor. So, the one which I am talking about right now is thermal noise. Now, in addition to the thermal noise, you also have flicker noise in transistors and the flicker noise is inversely proportional to the frequency of operation.

So, flicker noise in general will be something like this. So, you have two noise sources, you can say, two kinds of noise associated with the transistors, one is thermal noise as shown here, and the other is the flicker noise as shown here. So, both are random in nature, what value they will have at any given instant of time is not known precisely, you can only say that the noise current at this instant of time can be this value with this much of probability.

So, the transistor is used to design by the way, all your PFD, charge-pump, VCO and all the other blocks and it adds noise to the system. When it adds noise to the system, you actually have perturbations, you add to the Δt_i which actually leads to the final output jitter. So, now

you think about it, we designed a PLL using transistor, capacitors and resistors, by the way capacitors have no noise associated with them, even in the regular technology which we use. So, resistors and transistors are the noise sources. So, they create disturbance and they create these perturbations and the output clock jitter.

Now, the important part here is that these noise voltages and currents are so small that we can use our small signal analysis to find out how these noise sources affect the output noise. So, that is the way we are going to take forward to do the noise analysis in charge-pump PLLs. Thank you.