Phase-Locked Loops
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Lecture – 30
Sources of Non-Linearities in CP-PLL: PART I

Hello everyone. Welcome to this session. Earlier we have looked at the step-wise procedure for the design of a charge-pump PLL and a charge-pump clock multiplier.

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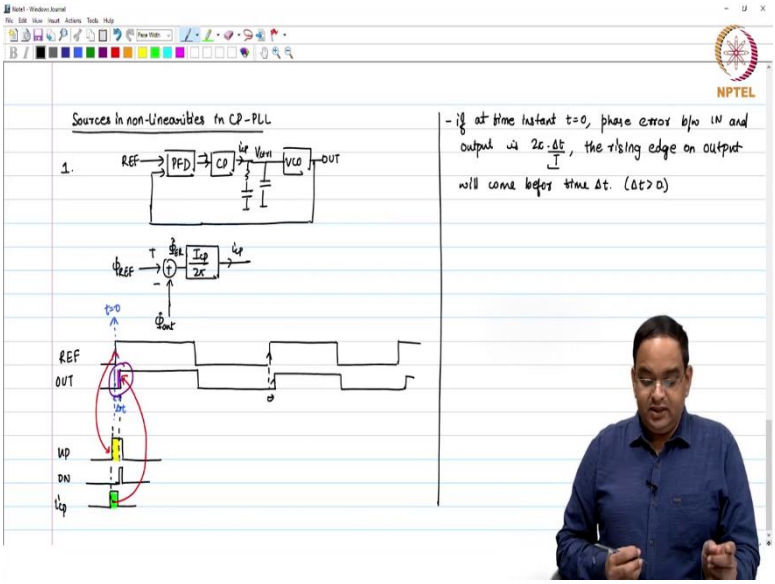

Now, we are going to look at the sources of non-linearities in the charge-pump PLL which we are ignoring while finding all the parameters for the PLL, sources of non-linearities in charge-pump PLL. It appears that unless these non-linearities are large, we can easily ignore them.

So, first thing is the following, what we have assumed in the charge-pump PLL is a linear gain model for PFD, for PFD plus charge-pump both, so, what does it mean? So, let me just draw the block diagram quickly and say, well, we have this PFD, we give it to charge-pump, loop filter and followed by VCO, this is what we do.

What we have assumed in our analysis earlier was the following. So, this has been the reference, this has been the output and the model of this we have used as phase error detector with plus minus followed by combined gain of PFD plus charge-pump is $\frac{I_{CP}}{2\pi}$ and that goes to the loop filter and so on.

So here, if I have any phase error between the input and the output phase which is φ_{ER}. This φ_{ER} gets modulated by the charge-pump and you get a corresponding I_{CP} gain. This is what we have assumed which in turn means that let me just plot our PFD response. So, just think about it that we are having this as a reference pulse and the other one as an output pulse.

So, let us say, in locked state the phase error is very less or the two rising edges are very close which in turn means that these rising edges are very close means the phase error is very small. So, this is the reference and this is the output. So, consider your time instant at this dashed line as $t = 0$. So, at this time instant, you get a rising edge on reference and after Δt time, you get a rising edge on the output.

What happens as soon as you get the rising edge on the reference? The UP pulse goes high and it remains high till the time the OUT pulse goes high. So, when OUT pulse goes high, we have seen that it will be having some overlap period and this will go down and this also goes down. So, this is what happens in the actual PFD.

Now, if you think about it that as soon as the rising edge on reference comes, if it comes before the rising edge on OUT pulse, that means you are going to have a positive phase error. So, this is the phase error. Because the UP pulse goes high, so, you get i_{cp} at the output, a non-zero i_{cp} at the output. Because you get a non-zero i_{cp} at the output, you go and change the control voltage of the VCO, you go and change the control voltage of the VCO which is going to change the rising edge on the output pulse.

So, a rising edge on reference triggers an UP pulse which gives you the current. So, I will draw the current also that will be helpful for us to understand. It gives a positive current, that current may remain only for this time, but you get this current and this current itself you have to highlight it because this is important here, this current itself goes and changes the control voltage and the rising edge on the V pulse.

So, if at time instant t, let me just write it, if at time instant $t = 0$, the phase error between input and output is $2\pi\frac{\Delta t}{T}$, this is what I am talking about without considering that charge-pump current comes and it changes the control voltage. If this is the phase error at time instant t, it does not remain the same.

If you think that the rising edge at the output will come at the phase error which you observe at time instant $t = 0$. It is actually not going to be the same because the charge-pump has come into action and it has changed the control voltage and so it has actually perturbed this edge.

You may get this edge before what you may think at time instant $t = 0$. So, I can write, if at time instant $t = 0$, phase error between input and output is $2\pi \frac{\Delta t}{T}$. The rising edge on output will come before Δt time. Here, by the way, $\Delta t > 0$. Just consider the opposite case.

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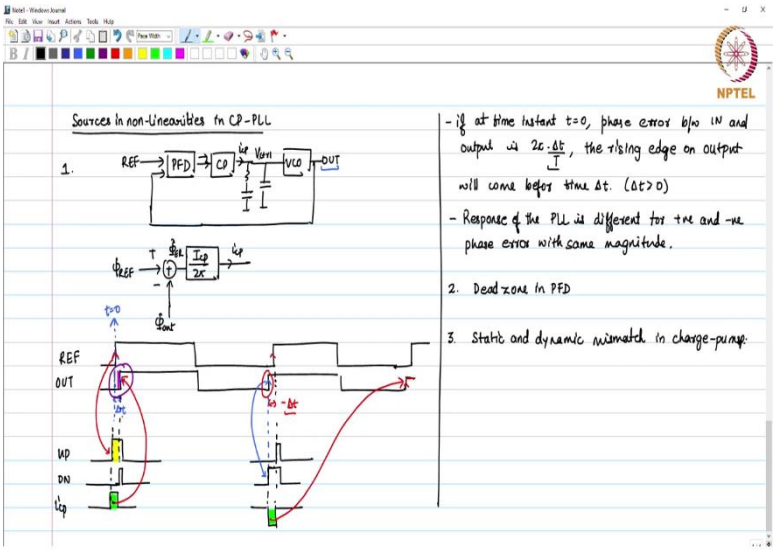

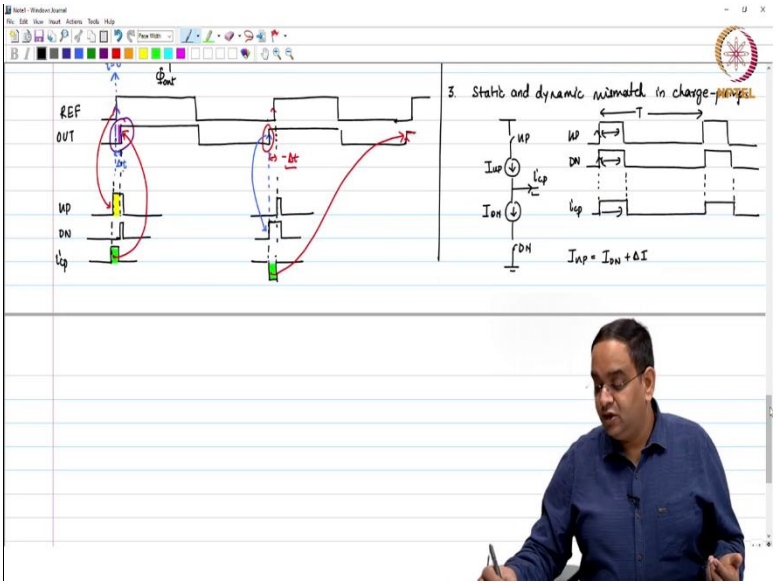

So, what is this opposite case? The opposite case is when you have, I am just showing you in the same waveform. Let us say when the rising edge on V comes first and then you have the rising edge on R. They are all frequency locked, so, do not worry about that. So, first I get the rising edge on V. If I get the rising edge on V, then my DN pulse will go high first and UP pulse will go high later when you are going to get a rising edge on OUT and this will happen.

Now, in this case, rising edge on V has triggered a rising edge on DN which in turn has actually triggered the current also, no doubt, current is negative. It has triggered the current. So, current reduces the control voltage, this is the current, it reduces the control voltage, when it reduces the control voltage, it is going to shift the rising edge at the output and the rising edge at the output, this particular current is going to change the next rising edge at the output. Because rising edge at the PFD inputs has already happened here.

So, if I keep the same phase error, here it was Δt, here I say the phase error is by the way $-\Delta t$. So, what you see here is, for positive Δt, I am changing the output rising edge in the same clock cycle whereas in case of negative phase error, the rising edge of the output is changed for the next clock cycle. The reference remains fixed, we are not changing the reference at all in this PLL.

So, the response of the PLL is different for positive and negative phase error with same magnitude. If you have positive Δt, it responds differently as compared to the negative phase error. Well, this is the non-linearity which you will see during settling. When the PLL is in the locked state and the phase error is very small, this non-linearity is negligible.

But depending on the implementation or depending on the phase error which you have, it may happen that you will observe this difference. And this non-linearity will then change the loop gain. Then the second non-linearity which we have seen is dead zone in PFD. Well, this is something which we have also addressed by having a buffer delay in the feedback path.

If you have some finite dead zone where your PLL does not respond, then in that particular case, it is a non-linear system. Now, the other non-linearities which you have observed quite often is or you will observe is the static and dynamic mismatch in your charge-pump.

So, what are these? Let me elaborate. What we have assumed is that we have a switch and this is a charge-pump current source. These are ideal current sources and as we close the switch, a current i_{cp} flows depending on our charge-pump current and these switches are controlled by UP and DN. Assuming that it is a perfect conversion of the pulse width to the current, whatever we have assumed is correct. But what happens in practice is that you will not have your UP and DN currents same.

So, if you do not have your UP and DN currents same, so, let us consider the locked state. In the locked state, I am just drawing the UP and DN overlap pulses. There is no phase error for example, if that is the case, then if this is UP pulse, then our DN pulse is also going to be the

same. Then, during the UP pulse, we know that the current which comes out, i_{cp} current is going to be I_{UP} and on the downside, it is I_{DN}.

If $I_{UP} = I_{DN}$, then no current flows from this charge-pump. But if $I_{UP} \neq I_{DN}$ or if I say $I_{UP} = I_{DN} + \Delta I$. If this happens, then what will happen in our actual PLL is that you will have $+\Delta I$ current flowing out at every reference clock period. Even when you think it should lock to zero phase error, it will not, this is what will happen.

Now, we have seen earlier that any difference in the current which is pumped into the loop filter every reference period is going to create a reference spur. So, this mismatch between I_{UP} and I_{DN} current actually leads to the non-linearity in the PLL and the PLL does not lock to a zero phase error because if you think that you have a zero phase error, then UP and DN pulses will be high like this. But in that particular case, you will always dump charge on the capacitor. So, your control voltage will increase.

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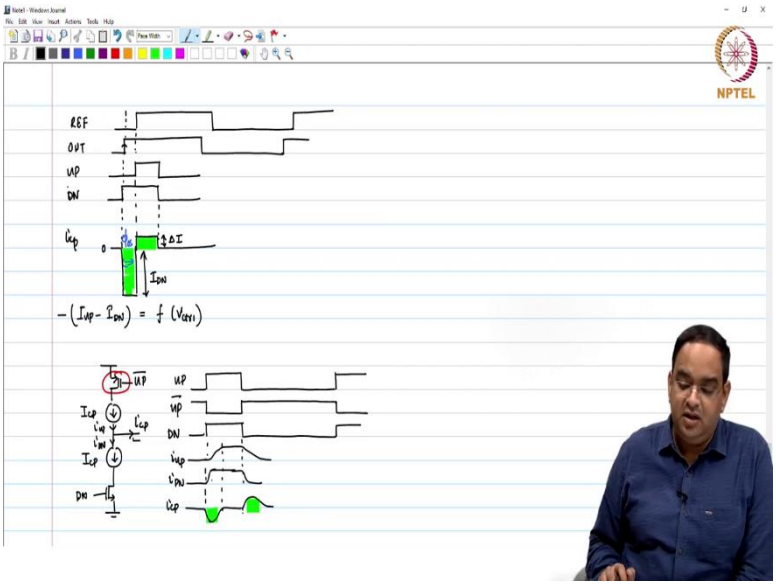

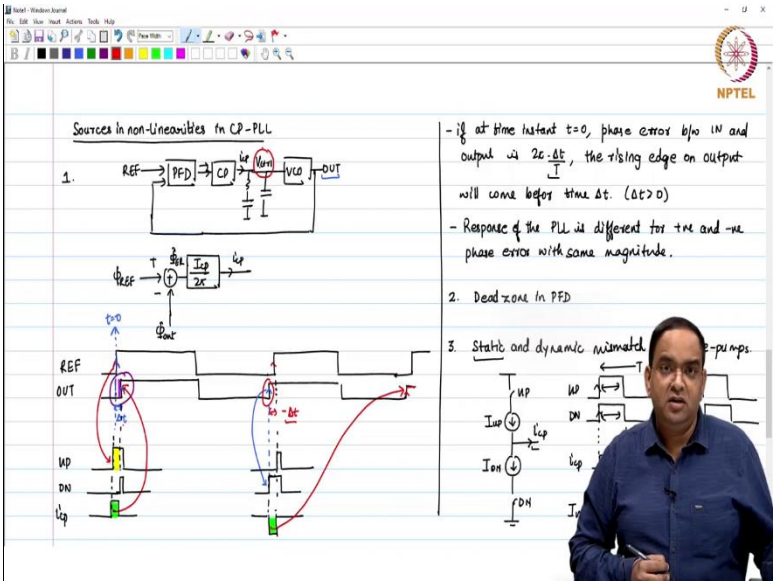

So, what happens is in the presence of the mismatch between the UP and DN current sources, input or your reference and output pulses are shifted in such a way. So, if $I_{UP} > I_{DN}$, then you will have a negative phase error such that the overall charge which is dumped onto the capacitor is zero in one reference clock period.

So, what is going to happen is that you are going to lock to a phase offset. I am assuming that I am having $I_{UP} > I_{DN}$ which in turn will lead to the following thing that I_{UP} will come here with the overlap, the overlap period is exaggerated here, that is fine and DN is like this.

So, DN is going to be like this. So, we know when DN comes first, in that particular case, $i_{cp} = -I_{DN}$, I am just doing it like this, from 0 level this is going to be $-I_{DN}$ and when you have UP and DN both the pulses high, at that time you are going to get this Δ.

So, this was the mismatch between the UP and DN current sources and this is actually DN current. So, the PLL is going to lock to a phase offset and, what is the phase offset by the way, this is the phase offset, this is φ_{os} in phase domain. So, it is going to lock to a phase offset in such a way that the total area under this curve is equal to zero.

So, if you have any mismatch between the charge-pump current sources which is actually a source of non-linearity in your PLL, you lock to phase offset but not to an offset of zero phase. Now, we talked about one thing that you have mismatch between I_{UP} and I_{DN}, well, this is actually static mismatch. What also happens in practice is that the mismatch varies depending on the control voltage. So, if you want to lock your PLL to different output frequencies, you will have the control voltage varying over a certain range.

So, what you see here is that $I_{UP} - I_{DN}$ or the difference between the top and bottom current is actually a function of, I would not write proportional, it depends on how you are having, is a function of control voltage. Now, this becomes more problematic in the loop gain. Because if this is a function of the control voltage, then your offset is going to vary depending on the frequency at which you are locking, your gain will also vary.

So, this is another non-linearity. When we are going to design these circuits, we will try to take care of these non-linearities as much as possible. Another non-linearity which is associated with the charge-pump is with the response time of the UP and DN switches. So here, what we have assumed is that these are ideal switches, as soon as we say that the switch is closed, the switch gets closed and current flows, but in practice it is little different.

And how is it different? Well, this switch is normally implemented using PMOS and this switch is implemented using an NMOS. So, this is $\overline{UP}$ and this is DN. So, when I give a signal of UP like this, let us say, in the locked state this is the signal which you want. If this is UP signal, then $\overline{UP}$ is going to be like this, this is $\overline{UP}$ and DN signal is going to be in this manner.

Now, the response time of your PMOS switch is going to be different from the response time of your NMOS which in turn makes us, let us say, the current values are equal in this case just as an example, and I am plotting this i_{UP} and i_{DN}. So, what happens is this i_{UP}, when your UP signal goes high here, this i_{UP} current has some response time and it will have a response like this. It is PMOS, so it may have a slower response and it will do like this. This is i_{UP}, i_{DN} is a little faster. So, it may do something like this.

So, if you look at i_{cp} which is nothing but $i_{UP} - i_{DN}$. During this time, well, it is 0. But during the transition time, what you are going to see is there is going to be some kind of current like this and then these two areas are going to be the same. So, just think that the area under these two curves is the same.

So, because of the mismatch in the response time of your NMOS and PMOS, you have the charge-pump actually adds current to the loop filter which is again a non-linearity. So, one thing is that all these charge-pump related issues whether it is the difference between the I_{UP} and I_{DN} which is the static difference or because of the dynamic difference based on the control voltage or because of different response time of NMOS and PMOS, they add ripple on the control voltage.

They add ripple to the control voltage thereby adding the reference spur. They also alter the linear gain of the PFD plus charge-pump. If these are within limits, you can still approximate the gain of the charge-pump plus loop filter as linear but in any case they are going to add spurs at the output. This is one of the non-linearities which is associated.

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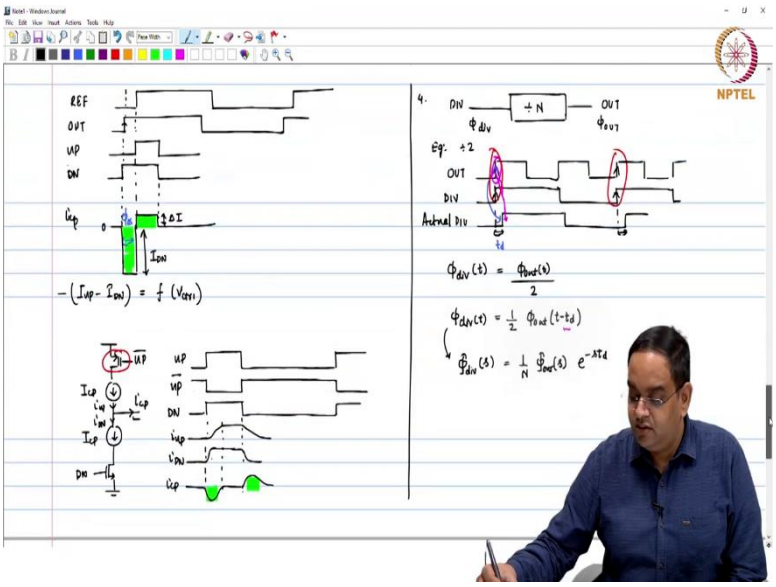

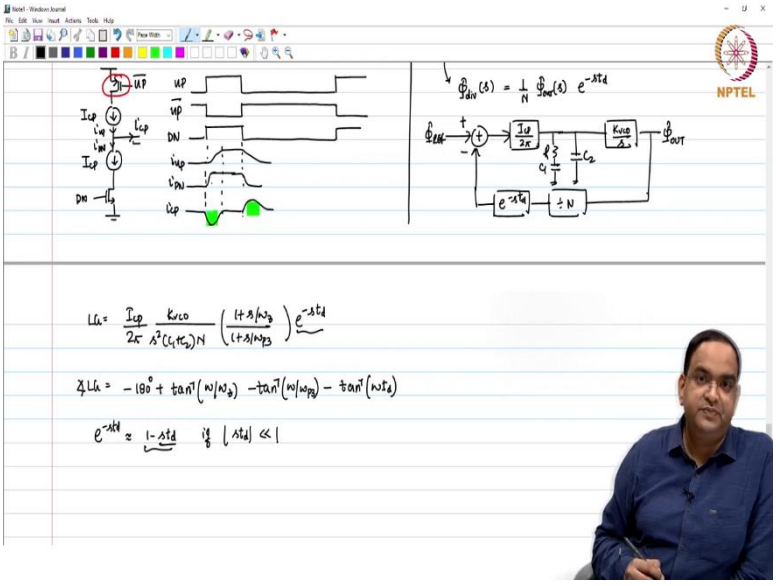

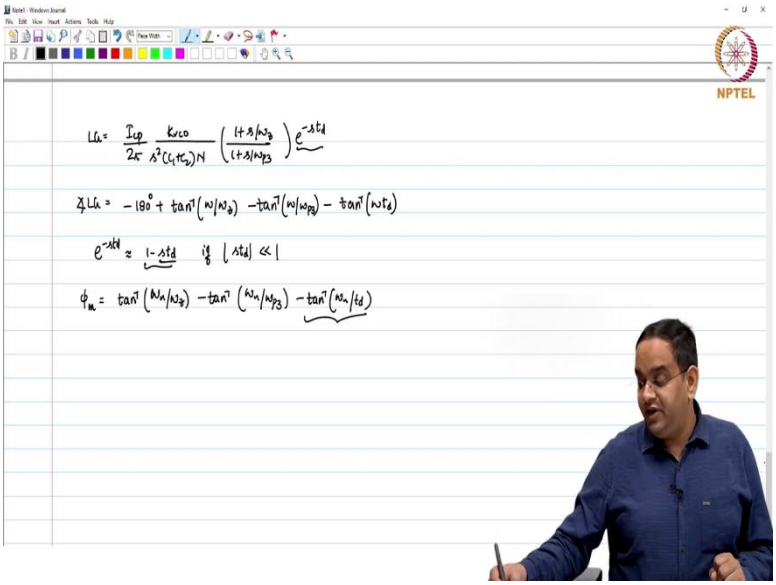

Another non-linearity which is associated with the charge-pump is the delay in the loop. Now, what is this delay in the loop? Well, you look at the frequency divider. So, the frequency divider which we have in our clock multiplier which is $\div N$ clock divider. So, I have output frequency here, and I have the divided frequency here. So, when I have output frequency and divided frequency, let us just assume, for example, in this case I am using $\div 2$. So, if my output frequency is something like this. Ideally, the way I have been using is that I write that,

$$\varphi_{div}(t) = \frac{\varphi_{out}(t)}{2}$$

The assumption which I am having is that as soon as I get a rising edge, we start getting the divided clock and my divided clock is something like this. These edges are aligned. If these edges are aligned, you do not get the divided clock at delayed at all, you get the divided clock exactly at the same instant as the rising edges align, but in practice what happens to the divided clock is that the divided clock is slightly delayed, this is slightly delayed.

So, when the divided clock here is not coming at the same edge, but it is coming at certain delay t_d, I cannot write that $\varphi_{div}(t) = \frac{\varphi_{out}(t)}{2}$, this is not the case. Because what is happening is the divided edge is coming later. So, you can very well say that the phase at the output is divided but that phase is actually delayed, so it is $\varphi_{div}(t) = \frac{\varphi_{out}(t-t_d)}{2}$.

If you make a change on the output clock, then that change is going to be reflected in the divided clock after t_d delay. You make a small change in the output phase, that small change in the output phase is going to be delayed by a certain amount.

Now, if this happens, then what happens to the transfer function? Then, we get,

$$\varphi_{div}(s) = \frac{1}{N}\,\varphi_{out}(s)e^{-st_d}$$

The delay may be very small, but it is a delay and this is something which we have not taken into account.

Now, with the divider with a certain delay in the PLL, our PLL transfer function is going to be different. So, what will be the new PLL transfer function? So, we have,

$$LG = \frac{I_{CP}}{2\pi}\frac{K_{VCO}}{s^2(C_1 + C_2)N}\left(\frac{1 + {}^{s}/_{\omega_z}}{1 + {}^{s}/_{\omega_{p3}}}\right)e^{-st_d}$$

Now, e^{-st_d} does not change the loop gain magnitude, it changes the phase. So, the new phase is going to be,

$$\angle LG = -180° + \tan^{-1}\left({}^{\omega}/_{\omega_z}\right) - \tan^{-1}\left({}^{\omega}/_{\omega_{p3}}\right) - \tan^{-1}(\omega t_d)$$

Now, what happens to the phase corresponding to e^{-st_d}? Well, you can directly take into account by making a little approximation and that approximation is actually done as follows:

$$e^{-st_d} \approx 1 - st_d \;\text{ if } |st_d| \ll 1$$

If the delay is much lesser than the reference clock frequency, then we can do this. So, if this is an approximation of e^{-st_d}, then you see that it is like a right half plane zero and a right half plane zero will reduce the phase, this is going to be ωt_d. If you would not have taken this delay into account and then you experience the delay later, your phase margin is going to be degraded and that phase margin is then going to be,

$$\varphi_m = \tan^{-1}\left({}^{\omega_u}/_{\omega_z}\right) - \tan^{-1}\left({}^{\omega_u}/_{\omega_{p3}}\right) - \tan^{-1}(\omega_u t_d)$$

So, this is the degradation in the phase margin which you will see because of the additional delay in the PLL. If for some reason, you introduce any other delay in PLL loop, you just be aware of the consequence that any delay is going to add a right half plane zero, and it will reduce the phase margin. So, this concludes the main non-linearities which we experience in charge-pumps. Thank you.