Phase-Locked Loops
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Lecture − 3
Basic Operation of a Phase Locked Loop

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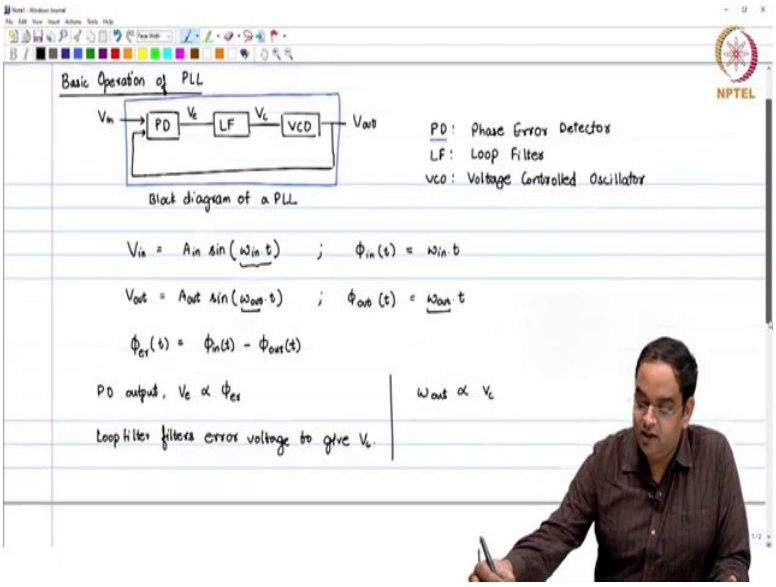

In this session, we will look at the basic operation of PLL. So, we will start. So, we are going to look at basic operation of phase-locked loop. So, previously we have looked at PLL as a block which generates frequencies as we desire. So, here I will first draw the block diagram of a phase-locked loop.

So, you have a block called phase detector, it has two inputs. And the output of the phase detector goes to a loop filter, this is loop filter. The output of the loop filter goes to a voltage controlled oscillator, for now. The output of the voltage controlled oscillator comes back as a feedback to the phase detector. Here, the input signal is V_{in} which feeds to PD and the output of the PLL is V_{out}. So, this is the block diagram of a PLL, you can say in general. Here, PD stands for Phase Error Detector. We will see what the phase error detector does. LF stands for Loop Filter and VCO stands for Voltage Controlled Oscillator.

So, if this is a PLL, it should generate some periodic signal at the output. And this particular PLL has input also as a periodic signal. So, here, V_{in} is a sinusoidal input given as follows:

$$V_{in} = A_{in} \sin(\omega_{in} t)$$

where, ω_{in} is the frequency of the input signal.

The sinusoidal output is given as follows:

$$V_{out} = A_{out} \sin(\omega_{out} t)$$

where, ω_{out} is the frequency of the output signal.

So, let me just put this as one single block. We feed sinusoidal signal at the input, V_{in}, and we get a sinusoidal output, V_{out}. For now, we will restrict ourselves to sinusoidal signals at the input and the output. Now, based on the discussion which we had in the last session, this parameter, $\omega_{in} t$, is nothing but the phase of the input signal. So, I can write the following:

$$\varphi_{in}(t) = \omega_{in} t$$
$$\varphi_{out}(t) = \omega_{out} t$$

where, ω_{in} is the input frequency, and ω_{out} is the output frequency.

So, this block, the phase error detector, somehow, we do not know how but somehow for now, the phase error detector computes the error between the input and the output phase. So, I define a term called phase error (φ_{er}). Phase error at any given instant of time is input phase minus output phase.

$$\varphi_{er}(t) = \varphi_{in}(t) - \varphi_{out}(t)$$

So, phase error detector computes the error between the input and the output phase and it gives a voltage. The output of the phase error detector is voltage, not some other variable. So, it gives the voltage proportional to the phase error. So, you can say that the phase error detector output which is error voltage, is proportional to the phase error, i.e., $V_e \propto \varphi_{er}$. Now, this is interesting. As you can see that the two input signals to the phase error detector are both sinusoidal voltage waveforms.

But, the phase error detector does not operate on the voltages, it operates on the phase error. And it gives the voltage which is proportional to the phase error. Now, this error voltage is filtered using a loop filter and it gives you a control voltage V_c. So, the loop filter filters error voltage to give V_c. This control voltage is used to control the frequency of the voltage controlled oscillator.

So, what does the voltage controlled oscillator do? The output frequency for the voltage controlled oscillator (ω_{out}) is proportional to the control voltage, i.e., $\omega_{out} \propto V_c$. And when you change the frequency of the oscillator in proportion to the control voltage, you will actually

change the phase at the output of the voltage controlled oscillator. So, we will look at it in detail one by one.

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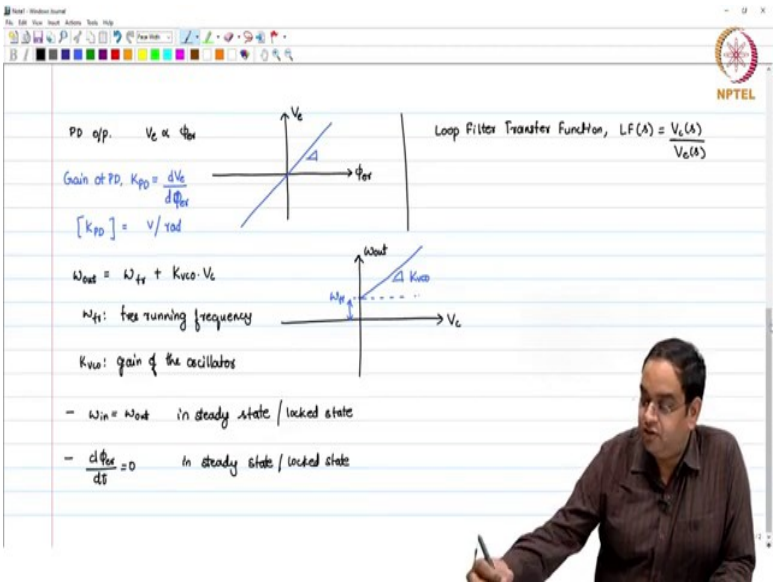

So, first one was phase error detector. So, as I said, phase error detector gives you error voltage. It gives you voltage proportional to the phase error. So, you can think about it that the PD output, $V_e \propto \varphi_{er}$. So, because this is directly proportional, there is a straight line characteristic between V_e and φ_{er}. So, the straight line characteristic between the phase error and error voltage will be something like this. The slope of this curve is the gain of PD (K_{PD}) and is defined as follows:

$$K_{PD} = \frac{dV_e}{d\varphi_{er}}$$

So, when you have a certain phase error at the input of the PD, you get an error voltage proportional to the phase error. The gain of this phase error detector is K_{PD} which is defined as the derivative of error voltage with respect to the phase error. The unit of K_{PD} is V/rad. So, once you get the PD output which is a voltage in proportion to the phase error, you filter this. And you filter this particular voltage with the loop filter using a transfer function, loop filter has a certain transfer function.

So, I can write like this Loop Filter Transfer Function ($LF(s)$) as follows:

$$LF(s) = \frac{V_c(s)}{V_e(s)}$$

where, s is signifying the Laplace Transform. So, whatever voltage you get here at the input of the loop filter, you filter it and you get the voltage. Now, you have the VCO. So, as I told, VCO output frequency is proportional to the control voltage. In general,

$$\omega_{out} = \omega_{fr} + K_{VCO}V_c$$

So, every term has a meaning here. ω_{fr} is the free running frequency of the oscillator, and K_{VCO} is the gain of the oscillator. Now, if you would like to look at this in plot form, what you have here is, with respect to the control voltage, ω_{out} has characteristics like this. This you can say, is the free running frequency, ω_{fr}. The slope of this particular curve is K_{VCO}.

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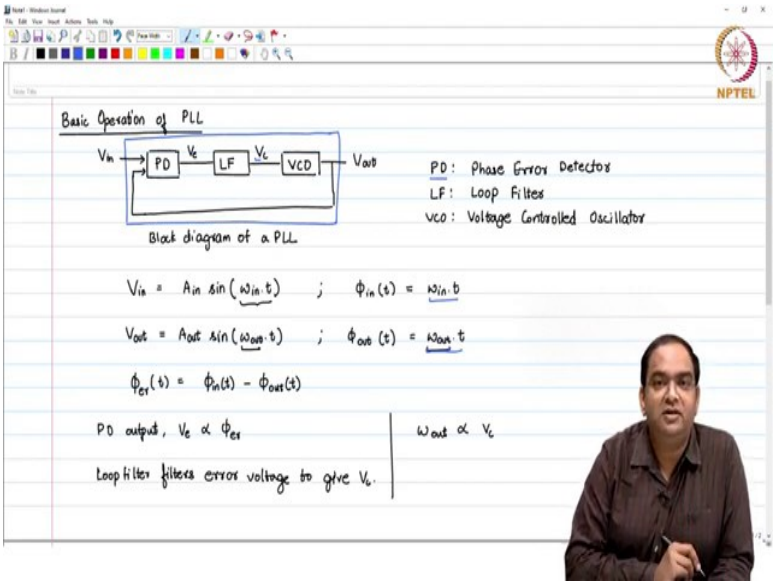

So, after knowing this, if you come back to this block, you see that you have the input as a sinusoidal signal. The oscillator is a block which generates sinusoidal output. If there is any error between the input phase and the output phase, then, the phase error detector generates the error voltage at its output, which is proportional to the phase error. The error voltage gets filtered using a loop filter which generates another voltage which changes the frequency of the voltage controlled oscillator. And as you change the frequency of the oscillator, you change the phase of the oscillator. So, when you change the phase of the oscillator, your error voltage will actually reduce and input phase and output phase will come closer.

In this particular PLL block, what happens in steady state or you can say in locked state when things have settled? The following things will happen:

$$\omega_{in} = \omega_{out} \text{ in steady state/locked state}$$

$$\frac{d\varphi_{er}}{dt} = 0 \text{ in steady state/locked state}$$

This is the condition for steady state or you can call this as locked state of PLL.

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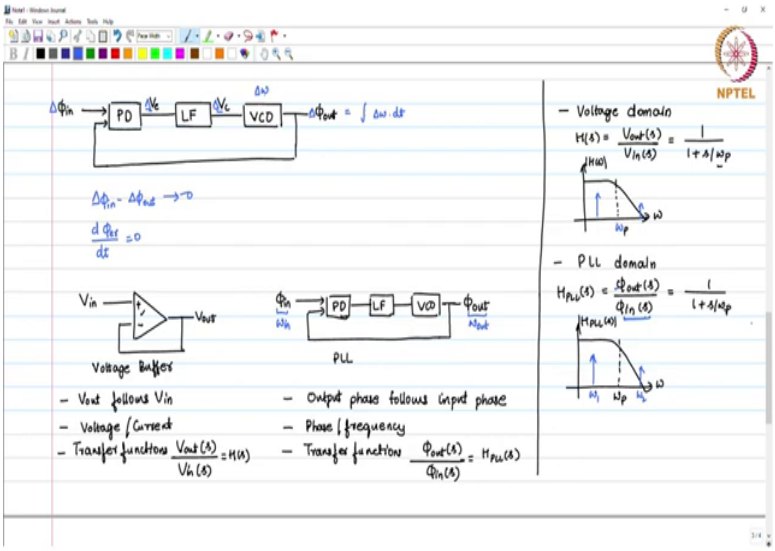

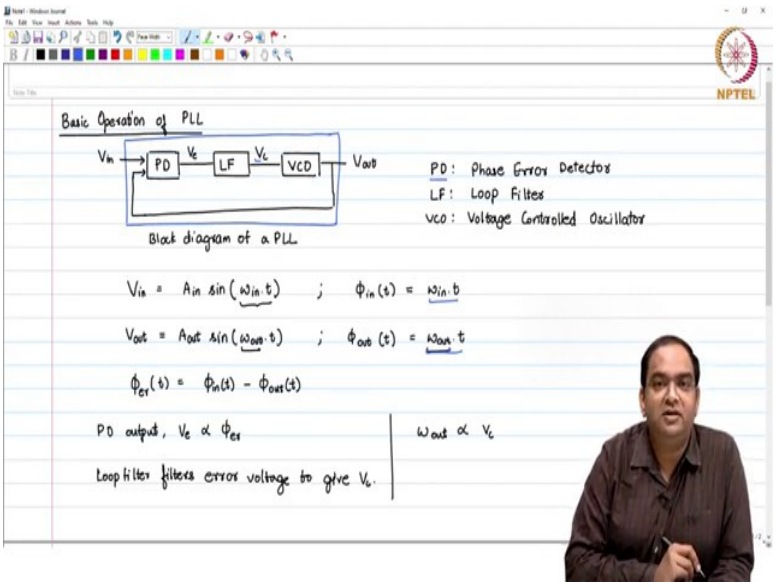

So, we will take an example to understand in a little more detail. So, given this block diagram, you give the input signal, you have a certain phase. So, I will just take an example here. So, as we know that we are operating on the input and the output phase, I will write only the phase variables as φ_{in} and φ_{out}. We know that the actual signals are voltages, but the loop is operating only on the phase signals. So, if I am going to change the phase, $\Delta\varphi_{in}$, just an example, if I increase the phase or I apply any change at the input, I will get a change in the

error voltage. This change in the error voltage will be reflected at the output of the loop filter as a control voltage and this control voltage changes the frequency of the oscillator by $\Delta\omega$. And the output phase is going to change by the integral of this change in the frequency. You will get a change in the output phase such that $\Delta\varphi_{in} - \Delta\varphi_{out} \rightarrow 0$.

In steady state, either

$$\Delta\varphi_{in} - \Delta\varphi_{out} \rightarrow 0$$

or the rate of change of this phase error becomes 0 as given below.

$$\frac{d\varphi_{er}}{dt} = 0$$

So, the phase error will not change with respect to time if the PLL is locked. Now, this is little interesting, that I have a block where my actual signals are voltages, but the different blocks in this PLL are operating not on the voltage or current signals, but they are actually operating on different variables like phase or frequency.

And it is not easy to extract the phase or frequency of the signal using different circuit elements which we know. But, we have to design in such a way that they operate on phase and frequency. Now, if you look at the PLL block which we have seen, this seems to be operating in a similar manner as a voltage follower or a buffer. So, for example, you are used to seeing a simple voltage buffer. I will just show you. This is a regular voltage buffer which you have used where you have an input voltage and an output voltage. So, this is a voltage buffer or a voltage follower.

Just like a voltage buffer, you have this PLL block, where you have the phase detector, loop filter and VCO. And in this particular PLL block, it is not the output voltage which follows the input voltage but it is the input phase which controls this block and output phase follows the input phase. So, if you would like to draw the similarities between your voltage buffer and your PLL. Here, V_{out} follows V_{in} whereas in this case, your output phase follows input phase. It is important to understand that the phase and frequency which you are seeing in the PLL, these variables are similar to the voltage and current variables in the amplifiers and other blocks which you have learnt and which you use now and then. So, in this case, our variables in general, are voltage and current. Here, the input and output variables which we are interested in, are phase and frequency.

The way you have analyzed or you would like to analyze this particular amplifier and the voltage buffer using transfer functions like $\frac{V_{out}(s)}{V_{in}(s)}$, in a similar way, you will analyze the input and output phase using the same kind of Laplace Transform, Bode plots and others for transfer function like this. So, here the transfer function which we will be interested in is like $\frac{\varphi_{out}(s)}{\varphi_{in}(s)}$. So, this is the similarity between a simple voltage buffer and the PLL block. Now, you may find little confusion that when we look at the transfer function, $H(s)$, in voltage domain, there we see that this $H(s)$ has frequency and phase information for the voltage transfer function. Now, we are talking about the transfer function for the phase $H_{PLL}(s) = \frac{\varphi_{out}(s)}{\varphi_{in}(s)}$. Here, φ_{out} and φ_{in} are phases.

So, just to help you understand, I will take an example here. I will just pick up one low pass transfer function. So, in voltage domain, we can write $H(s)$ as follows:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1 + \frac{s}{\omega_p}}$$

It is a low pass transfer function with a pole at ω_p. You can draw this transfer function like this, where you have a frequency ω_p. So, this is the transfer function which I plot. So, when you have this transfer function with respect to input voltage and output voltage, what does it mean? It means that if my input signal is within the signal bandwidth of ω_p, it will pass through. If I have a signal outside the signal bandwidth ω_p, it will actually get rejected. In other words, you can say that if you apply any change at the input which is within the bandwidth of this transfer function, that will come at the output whereas if you apply any input outside the bandwidth, that will be rejected by the filter.

So, we have looked at the voltage transfer function in voltage domain. In the same way, if I look at the same transfer function in phase domain or PLL domain, we have the following:

$$H_{PLL}(s) = \frac{\varphi_{out}(s)}{\varphi_{in}(s)} = \frac{1}{1 + \frac{s}{\omega_p}}$$

So, here, the transfer function which I am plotting is for input phase and output phase, not for input voltage and output voltage. This is something which you should be clear about. So, I have this $H_{PLL}(s)$. If I apply any change in the input phase at $\omega_1 < \omega_p$, I will see that change in the output phase. If I apply any change in the input phase beyond the bandwidth of the filter, then

that change will be rejected and I will not see it or I will see a very attenuated frequency at ω_2 at the output of the PLL.

So, please do not get confused between the frequency and phase of a transfer function with the frequency and phase used in the PLL block. In the PLL block, frequency and phase are the variables. You can have ω_{in} and ω_{out} also. So, this is where we have a similarity between the voltage domain and the phase domain. And whatever analysis we learn for the voltage in the voltage domain circuits, the same analysis will apply in the phase domain also.