Phase-Locked Loops
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Lecture – 29
Design Procedure for Charge Pump Clock Multiplier

Hello everyone. Welcome to this session. We were discussing the step-wise procedure for the design of a charge-pump PLL.

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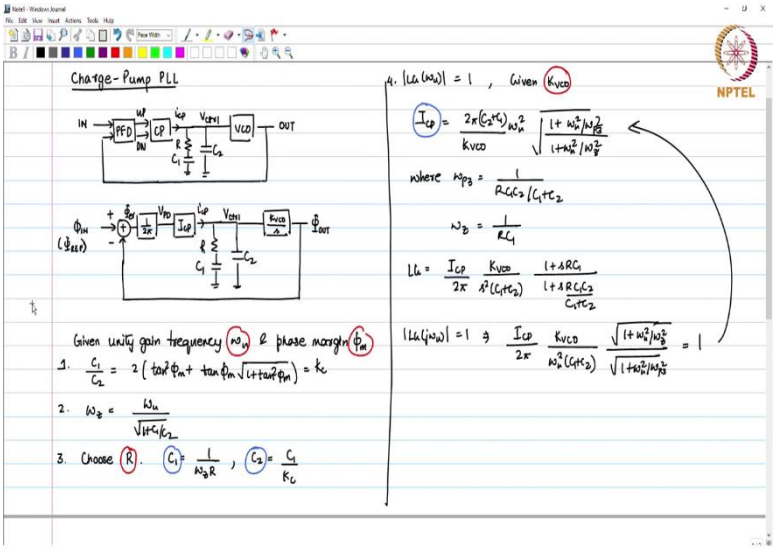

So, in the last session, we looked at the steps for designing a PLL given the unity gain frequency and the phase margin. So, our PLL was this with phase frequency detector and for the given phase frequency detector, the output of the phase frequency detector was fed to the charge-pump using UP and DN pulses.

The charge-pump output was given to a loop filter with a resistor R, C_1 capacitor and C_2 capacitor and the output of the loop filter was given to the voltage controlled oscillator and in this particular case, we had our output frequency feeding back to the input. So, this is our input, this is our output. The output of the charge-pump is current, small i_{cp}, the voltage was V_{ctrl}.

The small signal model of this particular PLL was this where you subtract the phase error in the PFD and the gain of the PFD was $\frac{1}{2\pi}$ followed by the charge-pump whose gain was I_{CP}, I_{CP} went through the loop filter with R C_1 and C_2 here and the gain of the VCO was $\frac{K_{VCO}}{s}$ for the phase.

So, I want to show the difference between this PLL and the PLL where you have frequency multiplication. Actually, the procedure remains the same for the design of the PLL, finding all other components. The only thing which changes is the loop gain. So here, we considered as φ_{IN} and φ_{OUT}, this is often also written as φ_{REF}, if this is the reference frequency.

So, you get phase error here and then output of the phase error detector, you can say this is V_{PD} and this is small i_{cp}, this is V_{ctrl}. So, what we said in the procedure was that you need to be given, this is important, given unity gain frequency ω_u and phase margin φ_m. The steps included first the calculation of $\frac{C_1}{C_2}$ ratio depending on your phase margin.

So, we did that and this turned out to be,

$$\frac{C_1}{C_2} = 2\left(\tan^2\varphi_m + \tan\varphi_m\sqrt{1+\tan^2\varphi_m}\right) = K_c$$

where, φ_m is the phase margin. The second step was given our $\frac{C_1}{C_2}$ ratio, we can find ω_z which was given by,

$$\omega_z = \frac{\omega_u}{\sqrt{1+\frac{C_1}{C_2}}}$$

The third step was given ω_z, choose R, now you can say how will you choose R? Well, that is going to depend on the noise which will be the topic of discussion in the coming sessions.

So, choose resistor R, this will give you the following:

$$C_1 = \frac{1}{\omega_z R}$$

Once you know C_1, your C_2 is also known because this constant $\frac{C_1}{C_2}$ is already known. So, C_2 is given by,

$$C_2 = \frac{C_1}{K_c}$$

Then using the fact that at the unity gain frequency, the modulus of loop gain is equal to 1, $|LG(\omega_u)| = 1$, this is the condition for the fourth variable which we would like to have, given this is equal to 1 and given K_{VCO} also. K_{VCO} is a parameter which you will get while designing the oscillator.

So, K_{VCO} is known. So, in the loop gain, K_{VCO} is known and other parameters are known. So, then we get,

$$I_{CP} = \frac{2\pi(C_2 + C_1)}{K_{VCO}} \omega_u^2 \sqrt{\frac{1 + {\omega_u^2}/{\omega_{p3}^2}}{1 + {\omega_u^2}/{\omega_z^2}}}$$

where,

$$\omega_{p3} = \frac{1}{\frac{RC_1C_2}{C_1 + C_2}}$$

$$\omega_z = \frac{1}{RC_1}$$

If you wonder how you get this equation, well, this is just reminding you that the loop gain of the PLL is given by,

$$LG(s) = \frac{I_{CP}}{2\pi} \frac{(1 + sRC_1)}{\left(1 + \frac{sRC_1C_2}{C_1 + C_2}\right)} \frac{K_{VCO}}{s^2(C_1 + C_2)}$$

So, what we are doing is, we are making that $|LG(j\omega_u)| = 1$. So, when you do that here, first I wrote the final equation, but now just to help you that how you will find it. We have the following:

$$|LG(j\omega_u)| = 1$$

$$\Rightarrow \frac{I_{CP}}{2\pi} \frac{K_{VCO}}{\omega_u^2(C_1 + C_2)} \frac{\sqrt{1 + {\omega_u^2}/{\omega_z^2}}}{\sqrt{1 + {\omega_u^2}/{\omega_{p3}^2}}} = 1$$

So, this will give you I_{CP}. So, you think about it, unity gain frequency and phase margin are the two numbers which you will start with. You will choose R or you can say you also know R.

By the way, R is a variable, R can vary, it does not have to depend on ω_u and phase margin. You can choose R and K_{VCO} is another parameter which you will get during the process of the design. What you found is C_1, C_2, I_{CP}. So, based on these, you will get the loop gain for the

desired unity gain frequency and phase margin. Now, if this PLL changes from PLL to clock multiplier when you are changing the frequency, how does the analysis change?

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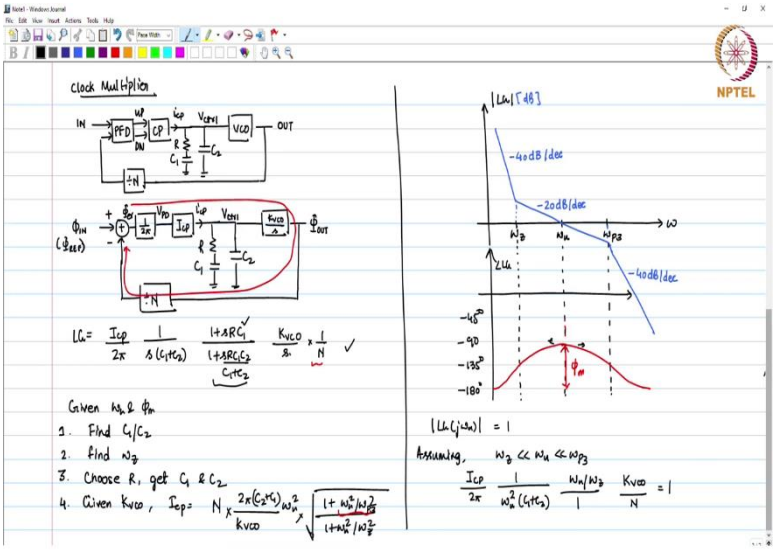

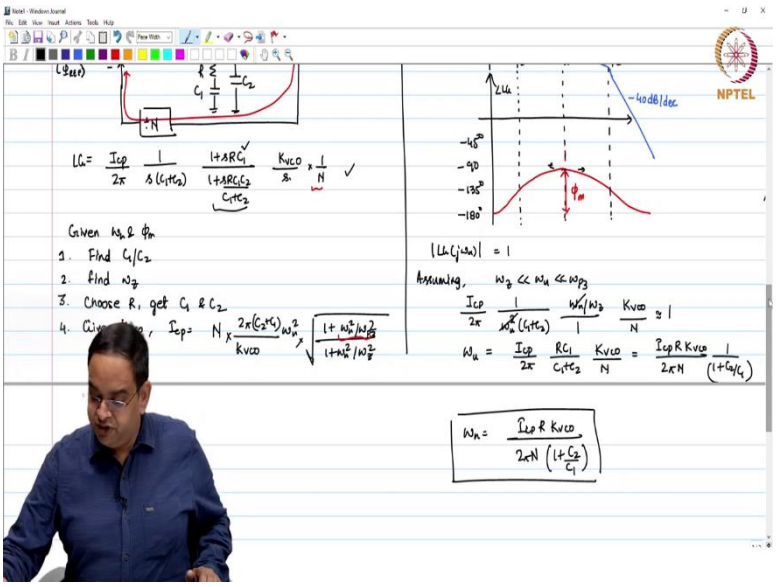

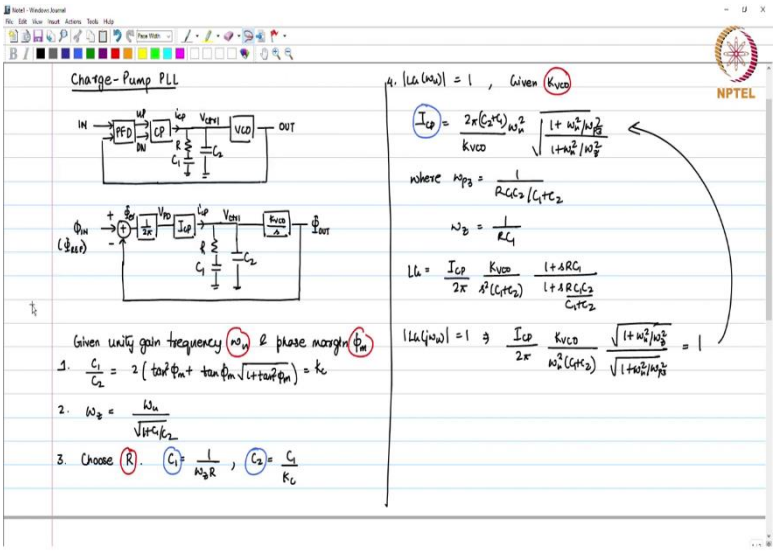

Well, it is very simple. I do not have to do anything here, just make one simple change. So, in place of the OUT connecting to the input, here I have a $\div N$ frequency divider. And when I have a frequency divider in the PLL block, I am going to have a phase divider in the small signal block.

So, the new loop gain is going to be,

$$LG(s) = \frac{I_{CP}}{2\pi}\frac{1}{s(C_1+C_2)}\frac{(1+sRC_1)}{\left(1+\frac{sRC_1C_2}{C_1+C_2}\right)}\frac{K_{VCO}}{s}\times\frac{1}{N}$$

So, you measured the loop gain by going around the loop and coming back. So, this is your loop gain. So, the loop gain has an additional factor of $\frac{1}{N}$.

Same procedure, no changes. Given ω_u and phase margin, you will find $\frac{C_1}{C_2}$. Second, once you know $\frac{C_1}{C_2}$, you find ω_z, that is what you did. Third step, you choose R and get C_1 and C_2. Fourth, given K_{VCO}, you get I_{CP}. The only difference here now in your I_{CP}, you are going to have in this transfer function you will have N also.

So, what we get here is just do it like this into this is N times. So, you get the correct expression as,

$$I_{CP} = N\times\frac{2\pi(C_2+C_1)}{K_{VCO}}\omega_u^2\sqrt{\frac{1+\omega_u^2/\omega_{p3}^2}{1+\omega_u^2/\omega_z^2}}$$

So, whether it is a clock multiplier or it is simple you can say a frequency buffer where the output frequency is same as the input frequency, the design procedure remains the same. In the second case, as you see the output frequency is N times the input frequency. So, if I design in this particular manner and I choose certain variables, what thing I am assuring you is the following. You found all the parameters, you feed those parameters back into the loop gain expression and draw the Bode plot for |LG|.

So, one thing is if your phase margin is going to be positive, your ω_u will be in between your ω_z and ω_{p3}, ω_u may be somewhere here. It is actually the geometric mean of ω_z and ω_{p3}. I am drawing this thing in log scale right now. So, I am going to see the characteristics like this. So, here you will see -40 dB/dec. Here you will see -20 dB/dec and this is going to be again -40 dB/dec.

Corresponding to the magnitude plot, you look at the phase plot. Let me just plot it till here, $\measuredangle LG$. So, at the zero frequency, you will have a phase addition of 45°. You are going to start from -180°. So, this is -180°, it will be -135° here and then whatever phase margin you desire, you will get this phase margin with maximally flat at unity gain frequency.

This is what you will get, this is maximally flat and your phase margin is φ_m, whatever you desire. So, our aim was to choose the parameters C_1, C_2 and R, and the placement of ω_z and ω_u in such a way that you get your phase response as maximally flat at the unity gain frequency. In that way, any small changes in the values of R and C_1, C_2, if C_1 and C_2 both change by the same value, your phase margin does not change. If your R and C change by a small amount, you can say if your unity gain frequency changes by a small amount, then your phase margin will not degrade that much.

Now, just a simple calculation from this expression, we get,

$$|LG(j\omega_u)| = 1$$

Assuming that $\omega_z \ll \omega_u \ll \omega_{p3}$, so, if I keep this assumption, then I can simplify this and I can neglect this part. So, if I do that and I want to calculate what my unity gain frequency is, then you will see my this is going to be,

$$\frac{I_{CP}}{2\pi}\frac{1}{\omega_u^2(C_1+C_2)}\frac{\omega_u}{\omega_z}\frac{K_{VCO}}{N} \approx 1$$

$$\omega_u = \frac{I_{CP}}{2\pi}\frac{RC_1}{C_1 + C_2}\frac{K_{VCO}}{N} = \frac{I_{CP}RK_{VCO}}{2\pi N}\frac{1}{\left(1 + \frac{C_2}{C_1}\right)}$$

So, to a simple approximation, you can say that ω_u, the unity gain frequency is given by,

$$\omega_u = \frac{I_{CP}RK_{VCO}}{2\pi N\left(1 + \frac{C_2}{C_1}\right)}$$

So, you can calculate the unity gain frequency and what you see here is that your unity gain frequency is proportional to R.

So, just think about it, if R varies slightly from the desired value, the unity gain frequency will vary, but $\frac{C_1}{C_2}$ remains the same. So, the phase margin will remain same. There is quite less deviation there. So, this is the standard procedure to design a simple charge-pump PLL or a charge-pump clock multiplier. Thank you.