Phase-Locked Loops
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Lecture – 27
Problems in Charge Pump PLL – Reference Spur

So, we were looking at the problems in the charge-pump PLL which we have introduced just a few sessions back. So, let us look at another problem in the charge-pump. And another problem in the charge-pump is associated with the charge-pump and loop filter action together.

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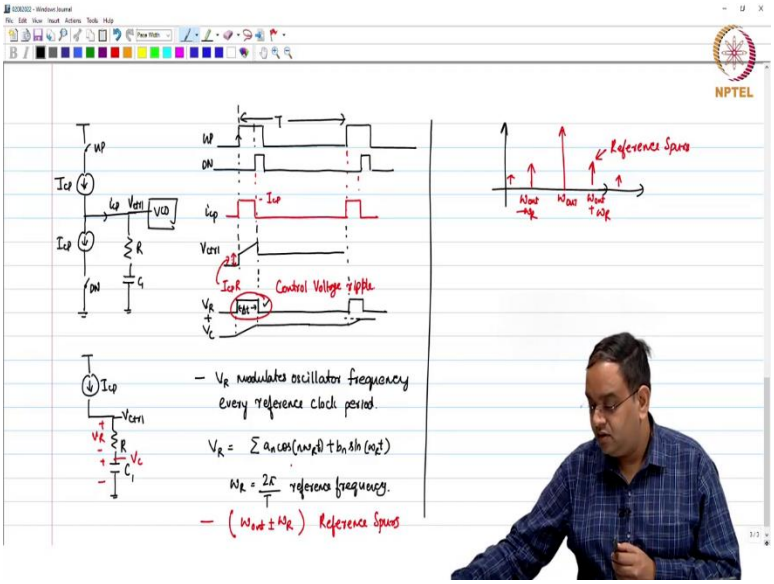

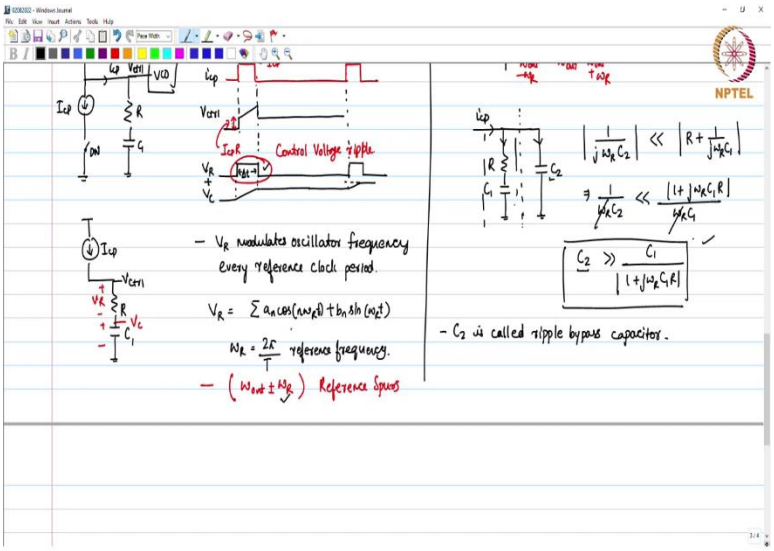

So, let me just redraw the charge-pump plus loop filter. So, you have this I_{CP} followed by the loop filter response. So, this is UP and DN, let us not worry about UP and DN now, I_{CP} and this is i_{cp} going in the system. Now, what happens is we have seen this multiple times that let us say the UP and DN pulses are such that you have some kind of phase error.

So, I am going to draw the UP pulse like this. It is periodic in nature, you can think about it and this is UP, and DN will also be a similar square pulse with a lesser width. Whether UP is larger or DN is larger, that depends on the phase error. So, in response to these UP and DN pulses, these UP and DN pulses, you have i_{cp}, small i_{cp}, the current which flows through the loop filter is shown here.

Now, when this particular i_{cp} current is pumped into the loop filter, earlier we drew the control voltage, this voltage is by the way control voltage. The control voltage happens to be like this, a jump, integration and jump like this and then comes back. If you think about it, what I am trying to do is, suddenly, you can think that suddenly you have i_{cp} current flowing through a resistor and capacitor. So, whatever value of the voltage, if this particular voltage before this rising edge may not be equal to zero, it will be some voltage. So, as soon as you start pumping the current i_{cp}, the capacitor voltage cannot change instantaneously. So, what you see here is a jump in the voltage and this jump is equal to $I_{CP}R$, the jump here is $I_{CP}R$ and then the current keeps on integrating over the capacitor, and the voltage keeps on increasing linearly.

So, if I call this as V_C, V_C is initially 0 and then it keeps on increasing. So, V_C and V_R, the voltage across the capacitor and resistor respectively can be drawn here. So, I will say that there is a voltage like this. So, you have a voltage like this. This is V_R voltage across the resistor and voltage across the capacitor is something like this. The voltage across the capacitor changes slowly, and $V_{ctrl} = V_R + V_C$.

So, what is the problem with this? Well, the problem is that the control voltage which is connected to the oscillator is changing every reference frequency and for multiple reasons. You have this oscillator here, this is your control voltage. So, the control voltage of the oscillator changes every reference frequency for multiple reasons whether you have phase error, some problems in the charge-pump and other things, those things will happen.

So, because of this change in the control voltage at the reference frequency, you modulate the frequency of the oscillator with V_R like pulse waveform. So, I will say V_R modulates oscillator frequency every reference clock period, this is my reference clock period.

Now, well, the waveform which you are seeing is more or less square waveform or square waveform with duty cycle and this is whatever Δt error you are going to have in steady state, it depends, the pulse width depends on that. So, this V_R can be written in terms of the Fourier series as follows:

$$V_R = \sum a_n \cos(n\omega_R t) + b_n \sin(n\omega_R t)$$

where, $\omega_R = \frac{2\pi}{T}$ is the reference frequency in rad/sec.

So, now you can write the Fourier series for this V_R waveform, it is modulating your oscillator's frequency and if you pick up even the first one, where n=1, then you see that you are modulating oscillator's voltage at ω_R which is finally leading to $\omega_{out} \pm \omega_R$. These components will come and the components at $\omega_{out} \pm \omega_R$ are normally termed as reference spurs.

So, if you look at the spectrum of the oscillator in a given PLL, you will find that you have ω_{out} and you have other components also and one of the dominant components is $\omega_{out} + \omega_R$, another is $\omega_{out} - \omega_R$. So, the problem of reference spur exists because there is an instant change in the control voltage of the oscillator. It is more prominent and it is not only that you are going to have $\omega_{out} \pm \omega_R$, depending on your output frequency, you are going to see other higher order harmonics also such as $\pm 2\omega_R$ and so on.

So now, we realize that this is the problem because of this control voltage variation which we also term as control voltage ripple. It is a ripple at the control voltage. Because of the control voltage ripple, we modulate the output frequency of the oscillator and we have unwanted components in the form of reference spurs. If we know the problem, then it is really good, we can find a solution.

So now, what we need to do is this. We cannot avoid the phase error information coming from the PFD plus charge-pump every reference frequency, that is not avoidable. So, what we need to do is the following. Let us say that I am going to get this current i_{cp} coming from the charge-pump in the loop filter.

And if I have this loop filter, I know that what will happen is there will be a jump. So, if I do not want that this should have a jump, what I can do is I can provide another low impedance path to the i_{cp} current which is coming at every reference frequency. So, that low impedance path can be provided by a capacitor with value C_2.

So, just for hand-waving analysis, let me put it that way, I have i_{cp}, it sees two paths, one with C_2 and other with R C_1. If I make sure that the impedance provided by C_2 at ω_R frequency or your reference frequency is much smaller than the impedance provided by R and C_1, then it will help in reducing the ripple on the control voltage. So, we have,

$$\left|\frac{1}{j\omega_R C_2}\right| \ll \left|R + \frac{1}{j\omega_R C_1}\right|$$

$$\left|\frac{1}{C_2}\right| \ll \left|\frac{1 + j\omega_R C_1 R}{C_1}\right|$$

$$C_2 \gg \frac{C_1}{|1 + j\omega_R C_1 R|}$$

where, ω_R refers to the reference frequency.

So, if you look at it, I need to provide, just from this, earlier we have seen that we chose C_1 and R such that we had proper phase margin and other things. Now, I have to choose C_2 which is larger than some particular component value and depending on the C_2 capacitor, I can bypass the ripple voltage. So, this C_2 is often termed as ripple bypass capacitor because we introduce it as a ripple suppressant.

Now, if we have C_2 as a ripple bypass capacitor, this analysis is just a hand-waving that the impedance provided by the two, but the combined impedance here of R C_1 plus C_2 actually introduces another pole in the loop filter which increases the order of the PLL and it questions the stability of the PLL.

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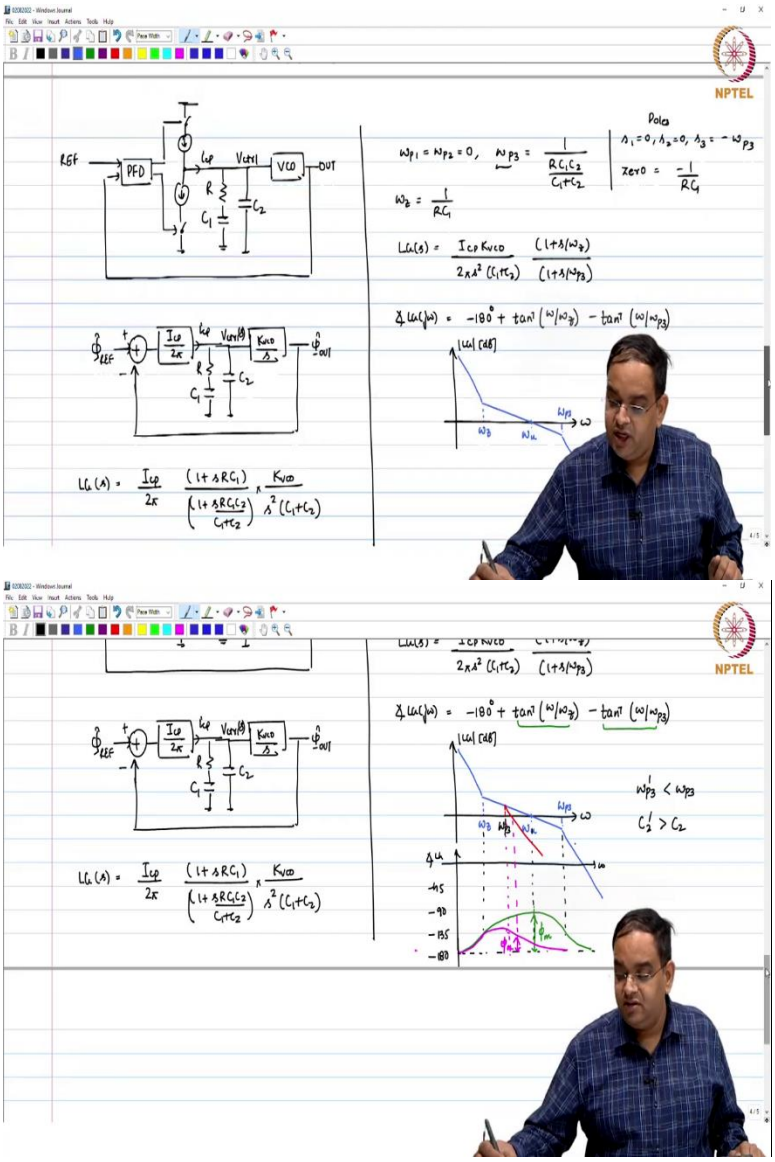

So now, let us just redraw our PLL with the ripple bypass capacitor. So, the charge-pump, another set of switches controlling here and then this goes through a loop filter using R C_1 and then C_2, R C_1 which goes to the VCO. So, what you see here is that we when we try to solve the problem, if we create another problem. We have to check that how much problem we solved and how much problem we created.

So here, we have the reference voltage, this is our OUT, this comes i_{cp} and this is the control voltage. The small signal model of this PLL, this again a simple one that you have the phase error multiplied by, I will write it as $\frac{I_{CP}}{2\pi}$ going into the loop filter with C_1 and C_2 which gets multiplied

by $\frac{K_{VCO}}{s}$, this is +, this is -, this is i_{cp}, this is $V_{ctrl}(s)$, so, φ_{REF} and φ_{OUT}. Look at the loop gain now.

So, loop gain for this particular PLL is given by,

$$LG(s) = \frac{I_{CP}}{2\pi}\frac{(1+sRC_1)}{\left(1+\frac{sRC_1C_2}{C_1+C_2}\right)} \times \frac{K_{VCO}}{s^2(C_1+C_2)}$$

So now, with this new loop gain, we will see whether this loop is stable or not. So, here you have two poles, at $\omega_{p1} = \omega_{p2} = 0$, and you have the third pole at $\omega_{p3} = \frac{1}{\frac{RC_1C_2}{C_1+C_2}}$. By the way, you must be used to writing these poles whether it is a left half plane pole or right half plane pole. Here when I am writing ω_{p3}, I am saying it is a pole but it is just the frequency part ω_{p3}. Poles are $s_1 = 0$, $s_2 = 0$ and $s_3 = -\omega_{p3}$.

So, I want to avoid any confusion here. $\omega_{p3} = \frac{1}{\frac{RC_1C_2}{C_1+C_2}}$ is not our pole. Now, zero in Laplace domain is actually at $-\frac{1}{RC_1}$ and the zero frequency which I use in the expression is $\omega_z = \frac{1}{RC_1}$. So, the loop gain expression can be rewritten as given below.

$$LG(s) = \frac{I_{CP}K_{VCO}}{2\pi s^2(C_1+C_2)}\frac{\left(1+{}^{s}/_{\omega_z}\right)}{\left(1+{}^{s}/_{\omega_{p3}}\right)}$$

The angle of this loop gain at any given frequency is given by,

$$\angle LG(j\omega) = -180° + \tan^{-1}\left({}^{\omega}/_{\omega_z}\right) - \tan^{-1}\left({}^{\omega}/_{\omega_{p3}}\right)$$

So, let us see whether our system is stable or not. First I am going to plot the loop gain with respect to ω, so, this is $|LG|$ in dB. What you see is that you are having two poles at 0, so, you will have -40 dB/dec, then you have a zero. So, it will be like this. Then depending on the position of our ω_{p3}, I am going to have the second pole. This is one option which you see that ω_{p3} is coming after ω_u. Looking at these things you can very well say ω_{p3} is surely going to be larger than ω_z because $\frac{C_1C_2}{C_1+C_2} < C_1$, but whether ω_{p3} is going to be greater than ω_u or less than ω_u, that we do not know.

So, if we have such a kind of loop gain, then the corresponding phase plot is going to be like this. So, at ω_u, you will have, so, I will just take another line here. So, this is -180°, -135°, -90°, -45°. So, it starts with -180°, it has a zero, so, it goes to -135°. If ω_{p3} comes much later, then it may reach close to -90° and when it comes ω_{p3} it may again go to -135° and then finally what you see here is that ω_{p3} is a pole. So, at maximum this can introduce 90°, this can introduce 90° which cancels out. So, as frequency tends to infinity, you may go to -180°. So here, the phase margin which you may calculate appears to be this.

Now, in place of the ω_{p3} location which we have seen, if it happens that ω_{p3} comes here because you increase C_2, so, ω_{p3} can change its location. If ω_{p3} comes here, then what you see is that you will surely have -135° and then you have another pole. So, before it reaches what you can say is your frequency comes, it does not reach -90°.

So, what you may see is that the phase is actually much lesser. It is not going to be -135°, it will be slightly larger than may be -135° and then it will finally go like this. So, these are the two cases which I have seen and if you now want to calculate the phase margin, it is going to be only this much. So, this I will write this as $\omega_{p3}{}'$. So, we have,

$$\omega'_{p3} < \omega_{p3}$$

$$C'_2 > C_2$$

C'_2 is the capacitor which you are using for ω'_{p3} and it appears that the phase margin is reduced.

So now, as we introduced another pole in the system, what we found is that yes you can reduce the control voltage ripple but you make your PLL more susceptible to instability. Well, we will not have a PLL which is unstable. So, we will try to make it stable with the desired phase margin. But if you do not pay attention, if you just use C_2 with a very large value, then what you will see as phase margin is not there, zero and pole cancel out, and with no phase margin, you will have an unstable PLL. So, we need to look at how we are going to choose this phase margin and how we place ω_{p3} in our system. Thank you.