Phase-Locked Loops

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Lecture – 26

Problems in Charge Pump PLL – Dead Zone in PFD

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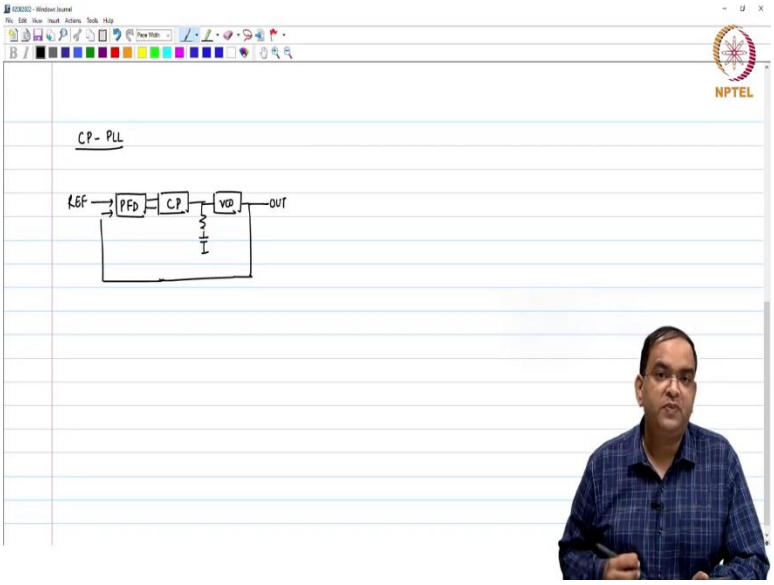

Welcome to this session. Having seen the basic operation of the charge-pump PLL and the small signal block diagram, we need to now look at some nitty-gritty of this charge-pump PLL and what we are going to see that the blocks which we thought are well behaved earlier, they have some problem and we need to fix that.

So, the first one is again just to give you a quick block diagram which we have been studying that you have a charge-pump, I will just write it like this, you have this loop filter followed by VCO and feed it back. So, this is the reference and this is the output.

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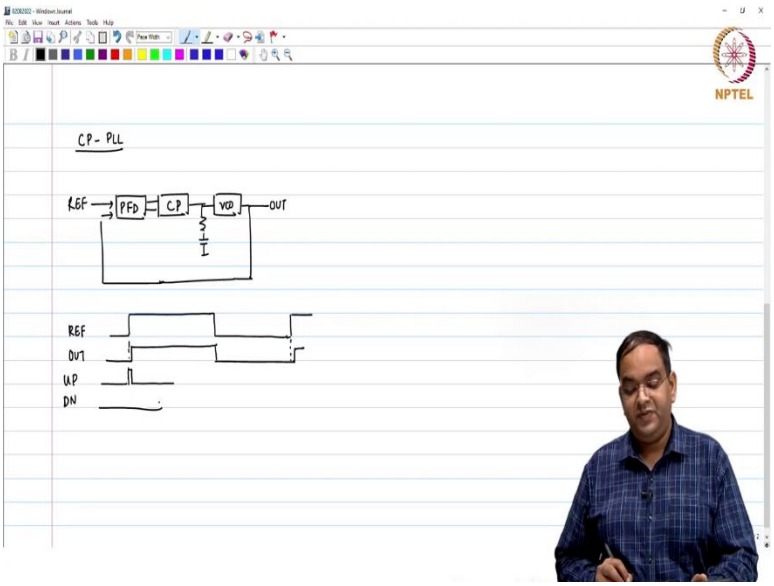

Now, given the reference and the output signal for the PFD, what happens is that when the reference signal comes very close to the OUT signal, very close, so, this error may be, phase error may be much much lesser, but it is still there, it may appear that it is zero but it is not zero. So, in response to this phase error, what we have is that UP goes high and it will come back as OUT signal goes high. So, these are the kinds of UP and DN signals which we have.

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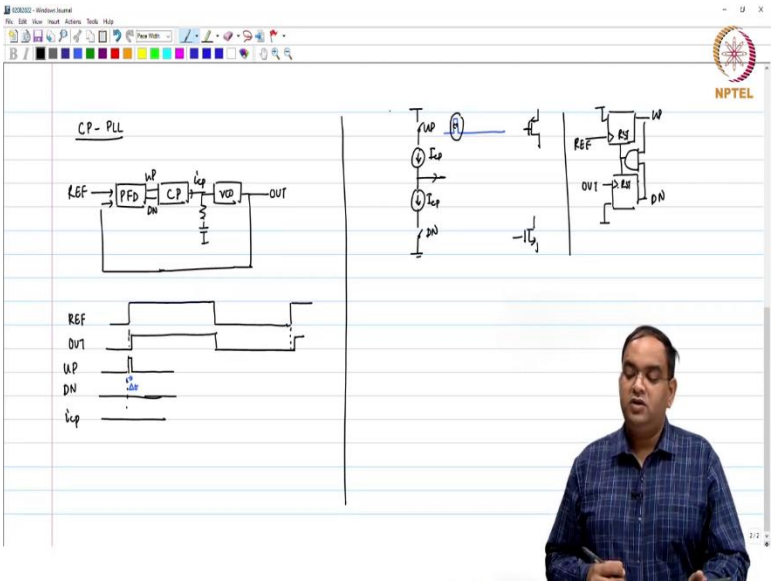

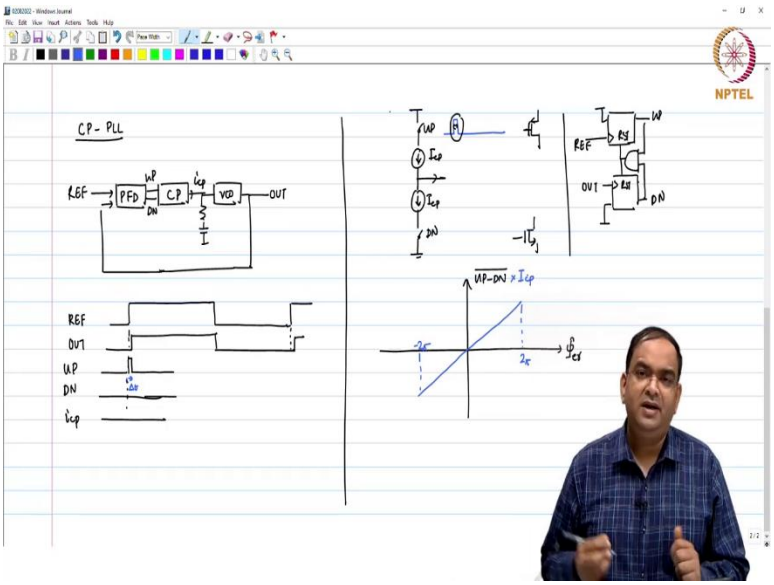

The problem with this kind of PFD is the following that when we use these UP and DN signals to clock the charge-pump, where was our charge-pump? Our charge-pump was something like this. Here we have the switches and this is UP and this is DN, this comes here, both are I_{CP}. So, these UP and DN pulses, so, just to tell you that the UP pulse which is coming here is a very narrow pulse, if you have very small phase error, then you are going to have a very narrow pulse which clocks these switches connected to UP and DN.

So, what will happen is that these UP and DN signals, see, UP and DN, at the end, they are switches. They may be realized using MOS switches such as either PMOS or NMOS. In any given technology, if you give this pulse to the MOS switch, if this pulse width is very narrow, then it will not even turn on. If it does not turn on for small phase errors, what it means is that i_{cp} the current which you are going to get out of the phase error detector, that current will remain zero, it will not change.

So, if the current does not change, then you can say even in the presence of the phase error at the input of the PFD, the PLL is not correcting for the output. So, there exists some region near the zero phase error in the PFD block which we have seen so far that your output does not change. What was the PFD block which we saw earlier? There were 2 D flip-flops whose inputs were connected to VDD. One was clocked you can say with reference, and the other was clocked with OUT in our case. The outputs of these blocks are UP and DN and they both were used by the AND gate to reset the outputs.

So, the UP and DN pulses which we have here, they are so narrow in this particular implementation that your switch cannot turn on which will now give different characteristics for PFD plus charge-pump. So, earlier, we saw PFD characteristics like $\overline{UP - DN}$ versus φ_{er}. Previously, our characteristics were something like this, from -2π to 2π. Now, if we are looking at the combined characteristics of the charge-pump and PFD, then you can say this is $\overline{UP - DN} \times I_{CP}$. It will just have the multiplication factor there.

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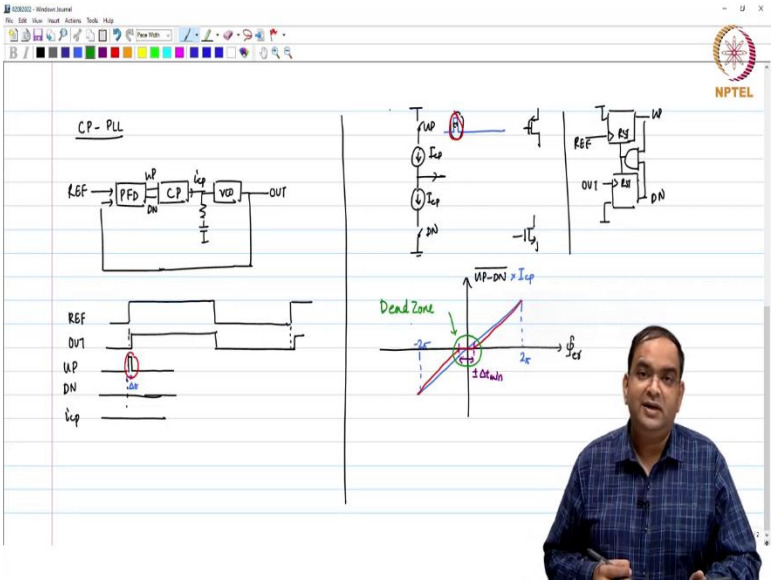

Now, as per our initial PFD analysis, for ideal PFD analysis, the characteristics will look like this. But what happens because it does not respond to phase error near zero, so, the output of PFD plus charge-pump is zero. And then when you have large enough phase error, you will surely have a linear response. So, here we are only saying that you need some minimum time for this pulse to turn on the switches.

So, if you do not give that minimum pulse time, you will have error and you can think about it that minimum pulse time is whatever you are seeing here. So, this is kind of the $\pm\Delta t_{min}$ which you need to have in your pulse width to correct for the phase error at any given time. This region of operation in the PFD which we have seen so far is called as dead zone. It is like the PFD is literally dead, it is not responding.

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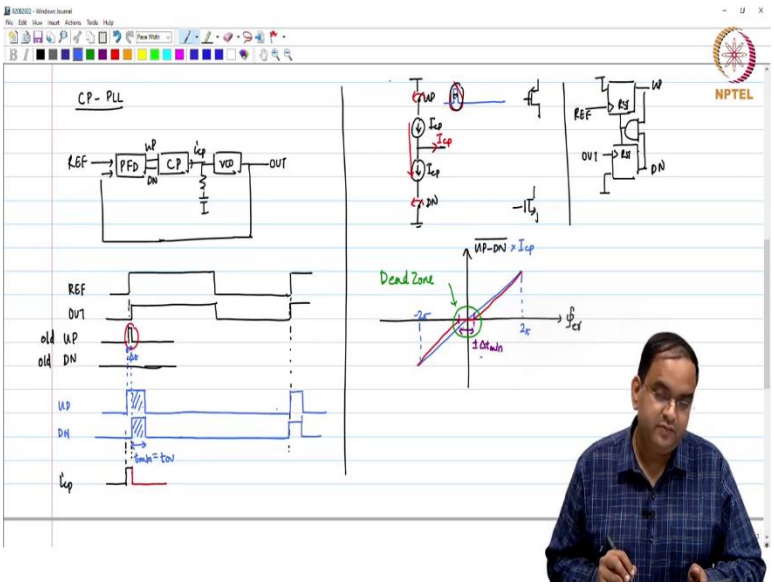

So, then we have to come up with some ways to get rid of this dead zone. So, to overcome this dead zone problem, what we do is the following. Let me just rewrite it. These are, let us say, these are old UP and DN signals. What do we do in the improved PFD or the PFD with removal of UP and DN? We make our pulse on for at least t_{min} time which is required to turn on our switches.

So, just look at this. So, when I get the reference pulse high, UP will go high like this. Whenever I get pulse on OUT, the DN pulse will also go high and both the pulses will remain high for t_{min} time and then both will come down. So, this is t_{min} period for which both the pulses UP and DN are high. It is also called as t_{ov} where the UP and DN pulses overlap each other. This is the region.

So, in response to this, if somehow we can implement it, you will see i_{cp}, if I provide minimum time for the switch to turn on, then current will also flow for now. So, what we have here is that i_{cp} goes high and it remains high for this time, and then as, so let us look at this. When UP pulse goes high, the switch closes, you get the current here, I_{CP}, then DN pulse comes, this also closes. So, I_{CP} which was flowing earlier into the loop filter, now, that flows down. You can look at it in multiple ways that you have a direct current path for I_{CP} from top to bottom. So, no current flows to the loop filter but in the charge-pump, the current flows and that current flows from top to bottom.

So, even if you think about it that your phase error is actually equal to zero. So, when your phase error is equal to zero, even then in that particular case, it is just, take another example that when I have phase error equal to zero, so, both the edges are aligned. In response to this, I will have the UP pulse going high for a minimum of t_{ov} period and come down. Similarly, I will have the DN pulse going high for the same amount of time and coming down.

So, in the charge-pump, both the switches get closed for zero phase error. You have zero current going into the loop filter but current flowing from top to bottom in the charge-pump. So, in this way, you can actually get rid of the dead zone problem.

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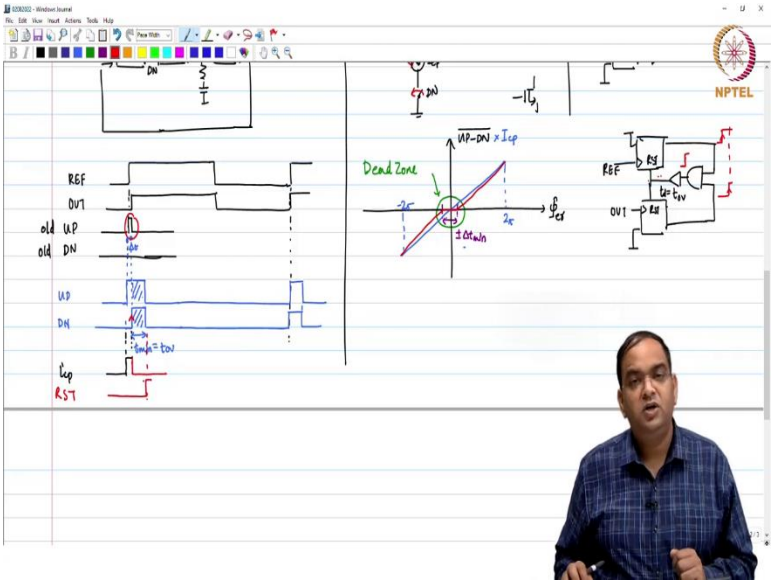

Now, how can we implement that thing in circuit? Well, what we actually need here is the following. Whenever the DN pulse goes high or the second pulse goes high like this, both the pulses come down only after a minimum amount of time.

So, just look back at the circuit here which we have been using for PFD. So, in this case, UP pulse goes high and then I have to wait for some time. So, what you can do is the following, the UP pulse goes high and the DN pulse goes high, so, the AND output becomes high which is going to reset the flip-flops.

So, what do I do? I introduce a delay of value t_{ov}, delay $t_d = t_{ov}$. If I introduce the delay in this path, then as soon as this goes high, when this particular thing goes high, AND output will actually

go high and when AND output goes high, because of the delay here, the reset pulse is delayed. So, when reset pulse comes, so, what we are doing here is I will just draw the RST also. So, ideally, the RST is coming at this node. As soon as RST goes high, the outputs will go low. So, you delay the reset such that this happens and how can you do that? You can do that by introducing a delay in the feedback path. So, in this way you can get rid of the dead zone problem in the charge-pump. Thank you.