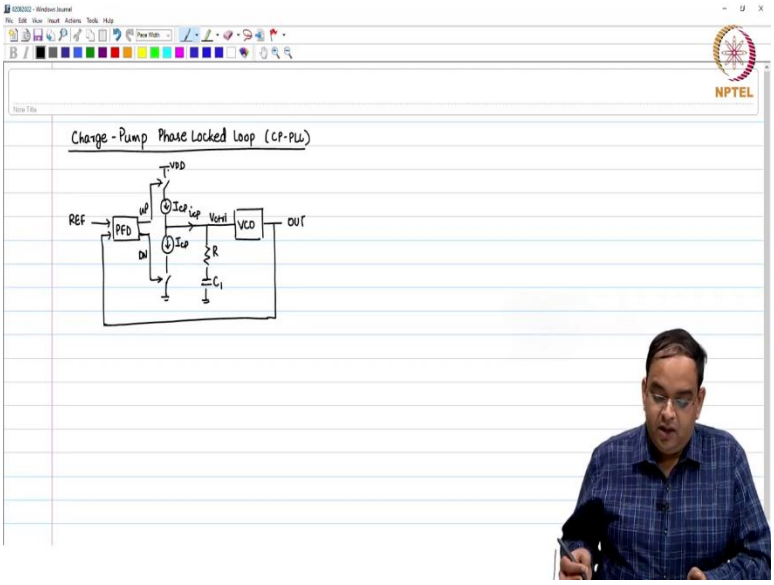
Phase-Locked Loops
Dr. Saurabh Saxena
Department of Electrical Engineering
Indian Institute of Technology Madras

Lecture – 25
Small Signal and Stability Analysis of Type-II Order 2 Charge Pump PLL

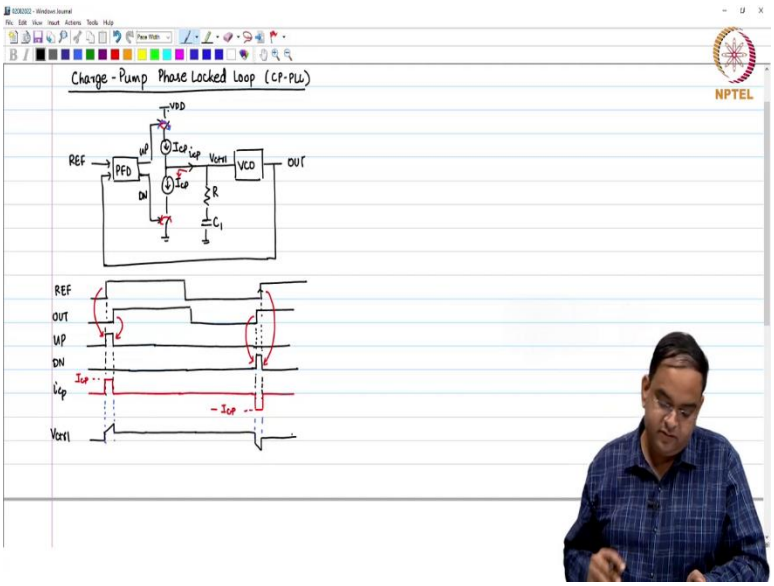
(Refer Slide Time: 0:17)



Welcome to this session everyone. In the previous session, we looked at the block diagram of a charge-pump PLL and we also drew the small signal model of the charge-pump PLL. So, today in this session, we will look at the analysis of the charge-pump PLL. So, our PLL included a phase frequency detector followed by a charge-pump. The charge-pump was realized using switches and current sources. So, we had two current sources, up and down. So, this was connected to VDD, this is ground as you see. These are UP and DN signals which actually open or close the switch. The output of the charge-pump here is the current I_{CP} in caps and you have a loop filter R and C_1. This loop filter output is connected to the oscillator in this manner.

So here, this is your reference signal. I will write this as reference and this is your output signal. The current which comes out of the charge-pump, I will write that as small i_{cp}, see, capital I_{CP} is the current in the charge-pump and depending on which switch is open, what current is flowing, that I am specifying with i_{cp}. This node voltage is control voltage.

(Refer Slide Time: 2:29)



Now, in this actual circuit, if we look at the reference and the output pulses at any given instant of time, you may have some phase error at any given time, so, these are reference and output. So, deliberately I am showing you what happens when you have some small phase error. At that particular instant of time, for the other one let me just draw the negative phase error for example, like this.

So, in response to this reference and OUT pulse, you will have UP and DN pulses going like this, this will be your UP pulse, and corresponding DN pulse, it will actually remain 0, ideally, and the DN pulse goes high when you get a rising edge on the OUT pulse before the UP pulse. So here, I am just giving you one example where the OUT pulse goes high before, so the OUT pulse goes high and then when you have a rising edge on reference, the OUT pulse goes down.

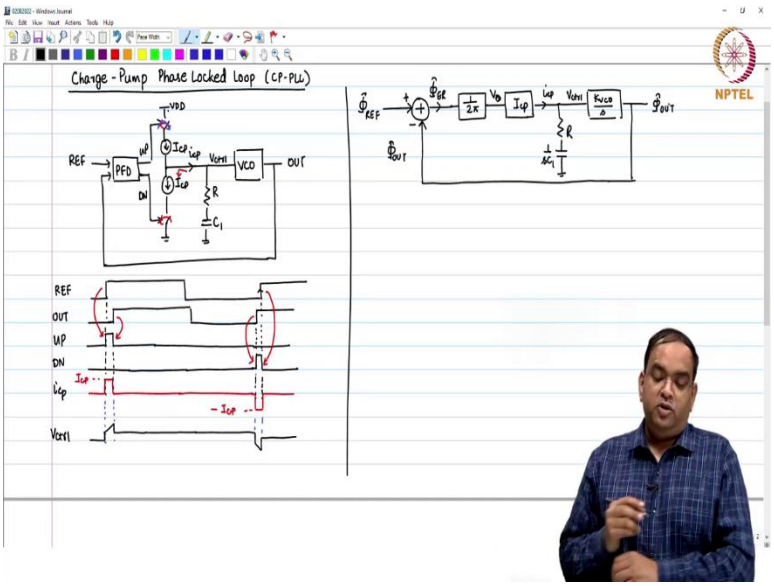
So, effectively your reference is triggering this, your output is triggering this, similarly here. So, these are your reference and OUT pulses. In response to these reference and OUT pulses, we have i_{cp}, this current should be equal to our I_{CP} current.

So, when the UP pulse goes high, you actually close the switch and i_{cp} flows here. So, you have i_{cp} current flowing in the given direction, the current value is capital I_{CP}, it flows for this much amount of time. And then when DN pulse goes high, the UP pulse goes low, so the switch is open again. DN pulse goes high, this switch gets closed, the current i_{cp} flows in this direction. So, giving

the direction, we define the direction by the sign, your i_{cp} current is like this, this value is you can say $-I_{CP}$. This is how the current flows.

Now, in response to this current, you are going to have a change in the voltage, a control voltage change and this control voltage V_{ctrl} happens to be you will take a jump $I_{CP}R$, it will integrate and it will come back to I_{CP} and then it will remain constant. When you get a negative pulse, then what you will do is you will take a negative jump of I_{CP}, it will integrate in the opposite direction and your control voltage will become like this. So, this is what is happening to your control voltage. Now, based on the control voltage, your frequency will change and the phase will change and the PLL is going to lock.

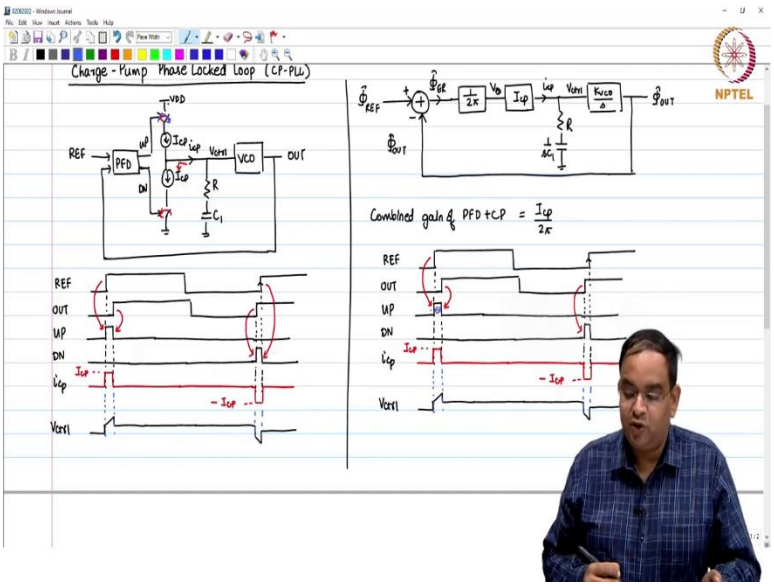
(Refer Slide Time: 6:20)



Now, for this particular charge-pump PLL, we drew the small signal diagram and small signal diagram was shown like this. You have φ_{REF}, and you detect the phase error. So, effectively you are subtracting the output phase from the reference phase, and you get the phase error. The phase error output, you have a PFD. So, PFD plus charge-pump combined gain is equal to $\frac{I_{CP}}{2\pi}$, if you want to write it separately, we can write it as $\frac{1}{2\pi}$ for phase error detector gain in steady state and this is I_{CP}.

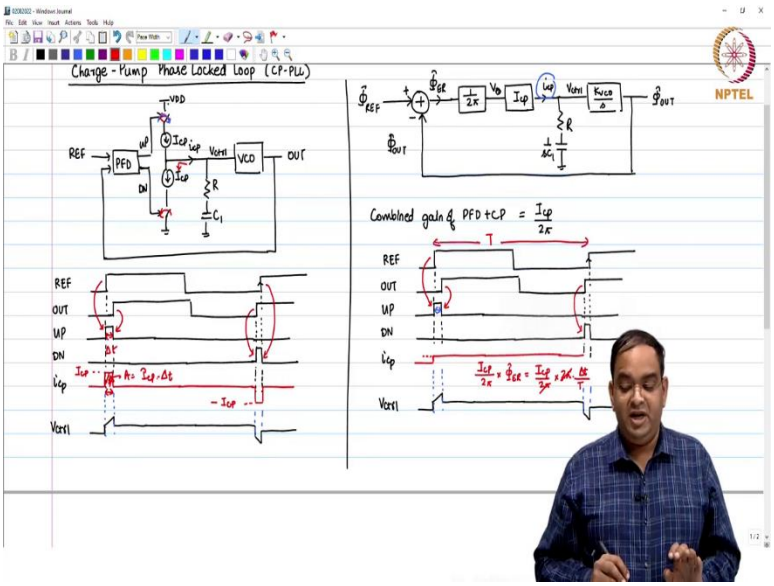
So here, you can still say this is V phase error detector, V_{PD}, in our case PFD and this is the charge-pump current. So, this current goes through the loop filter as shown here, R and $\frac{1}{sC_1}$. $\frac{1}{sC_1}$ is the impedance of the capacitor and then it has a VCO whose response from control voltage to output phase is $\frac{K_{VCO}}{s}$. So, this is the small signal model of the charge-pump, this is φ_{out}.

(Refer Slide Time: 8:14)



So, in the previous session, we approximated the combined gain of the PFD plus charge-pump as equal to $\frac{I_{CP}}{2\pi}$. So, that was an approximation actually, if I look at the actual operation and our modeling, there is some difference and we will tell that this difference is actually negligible in many cases. First, you can say, approximation here is what we are considering is with respect to the phase error. So, this corresponds to the Δt error or phase error, whatever you call it. So, the phase error gets multiplied by $\frac{I_{CP}}{2\pi}$ and that current is there.

(Refer Slide Time: 9:36)



So, the average current i_{cp}, average current if we would like to write based on the phase error which we have, this is an approximation which we are using by the way. So, this current is like this, this is an approximation. What is the value of this current? The value of this current is as follows:

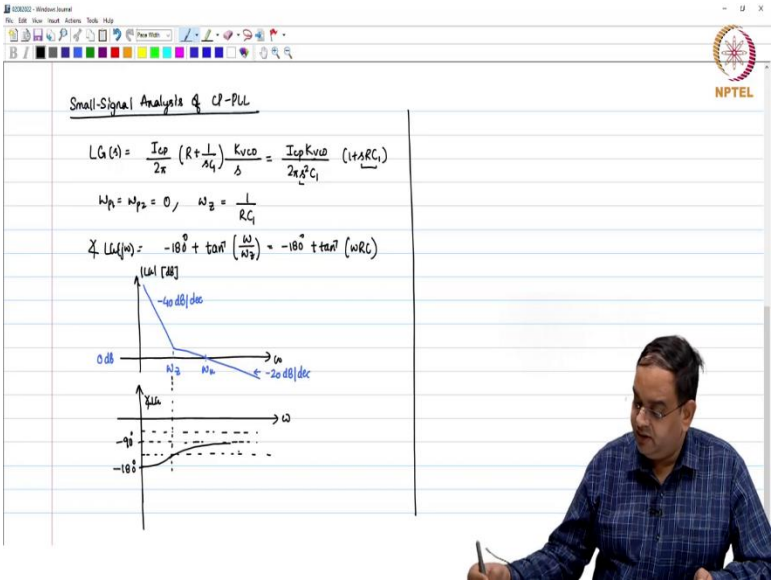
$$\frac{I_{CP}}{2\pi} \times \varphi_{er} = \frac{I_{CP}}{2\pi} \times 2\pi . \frac{\Delta t}{T}$$

So, these things cancel out, if you look at it, the average of the total charge which I am going to add here is, that is the area under this curve, this area under this curve is equal to $I_{CP}.\Delta t$ which corresponds to the phase error. Here also, this is this value $I_{CP}\frac{\Delta t}{T}$. If you integrate it over time period T which is the reference clock period, you will get the same value.

So, our modeling is slightly different from our actual operation and under the assumptions that our frequency of operation or the frequency at which the changes are happening in the system, that frequency is much lesser than the frequency at which we are clocking this system. So, well, under those assumptions, you can approximate your charge-pump current like this. We will see later that when the bandwidth of this whole loop is much higher or it becomes closer to reference frequency, then our assumptions will not be valid.

So, for now, assume that the assumptions which we have made, those assumptions are valid and the relationship between the actual operation and the operation in our small signal model is as shown. Let me just remove V_{ctrl} from here because now with respect to this i_{cp}, V_{ctrl} will change. So, with respect to this small signal model, the thing which we need to understand is that whether this model is stable or not, and what are the gains from different nodes to the output.

(Refer Slide Time: 12:38)



So, for the small signal analysis of charge-pump PLL, our loop gain which is defined as the gain around the loop, that is this loop we are talking about. The loop gain of this system is given by,

$$LG(s) = \frac{I_{CP}}{2\pi}\left(R + \frac{1}{sC_1}\right)\frac{K_{VCO}}{s} = \frac{I_{CP}\,K_{VCO}}{2\pi s^2 C_1}(1 + sRC_1)$$

So, this is our loop gain. There are two poles, so, $\omega_{p1} = \omega_{p2} = 0$, the two poles are at 0, and the zero for this transfer function is at $\omega_z = \frac{1}{RC_1}$. The angle of the loop gain is given by,

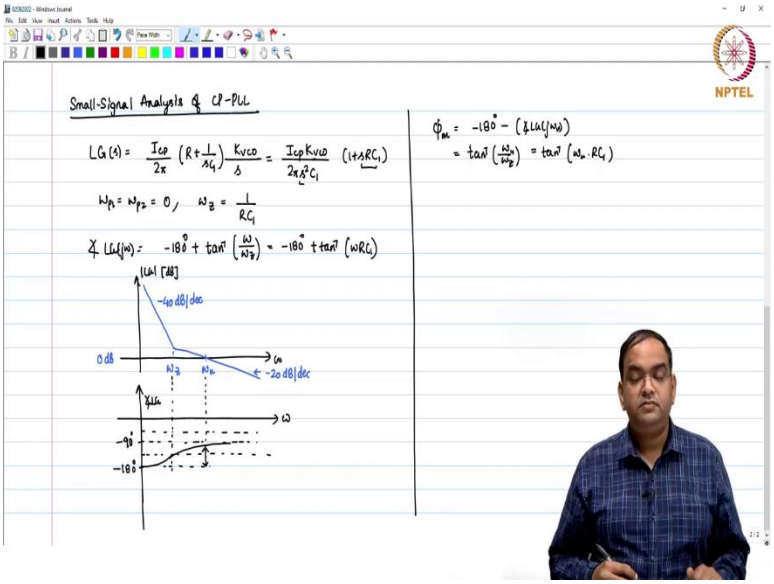
$$\measuredangle LG(j\omega) = -180° + \tan^{-1}\left(\frac{\omega}{\omega_z}\right) = -180° + \tan^{-1}(\omega RC_1)$$

Now, just to plot this particular loop gain with the help of Bode plot, we have $|LG|$ versus ω. I will plot this in dB 20. So, you have -40 dB/dec starting from zero frequency, and then you will have a zero, and based on the zero, you will have this is going to be -20 dB/dec. This frequency is zero

frequency. The frequency at which you cross the unity gain or 0 dB line, that frequency is unity gain frequency.

Corresponding to this magnitude plot for the loop gain, you have the phase plot, angle of loop gain, $\measuredangle LG$, the starting phase happens to be $-180°$. So, I will just plot this. So, there are two frequencies which are important right now, one is the zero frequency, so, you start from $-180°$, so this, this I make as $90°$. When you come to the zero frequency, you are going to add a phase of $45°$, so, it will become $-135°$ and then from $-135°$, it is going to, at infinity, this frequency is going to be $-90°$, it will not cross $-90°$.

(Refer Slide Time: 16:26)

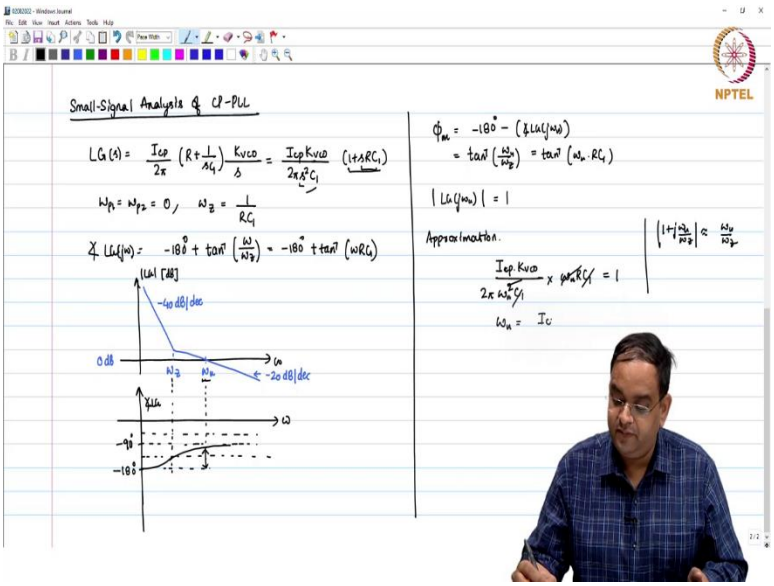


So, to check the stability of this particular loop, what we need to see is, what is the phase margin. The difference between $-180°$ and the actual phase at unity gain frequency. So, the phase margin is given by,

$$\varphi_m = -180° - \left(\measuredangle LG(j\omega_u)\right)$$

$$\varphi_m = \tan^{-1}\left(\frac{\omega_u}{\omega_z}\right) = \tan^{-1}(\omega_u . RC_1)$$

(Refer Slide Time: 17:12)



Now, how do we know what is ω_u? Well, to find ω_u, you can very well find ω_u such that the magnitude of loop gain is equal to 1. So, we have,

$$|LG(j\omega_u)| = 1$$

You substitute it back, you will find what is ω_u, or the other way is an approximate way. So, you can do an approximation, quite often it works. The approximation is given by,

$$\frac{I_{CP}K_{VCO}}{2\pi\omega_u^2 C_1} \times \omega_u RC_1 = 1$$

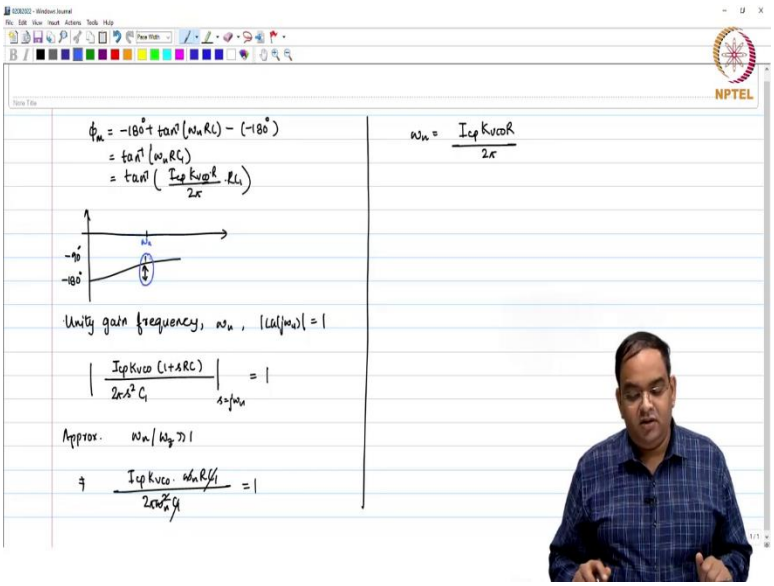
This is an approximation. So, what I am saying here is that $1 + sRC_1 \approx sRC_1$ and the reason you can say that $\omega_u \gg \omega_z$. So, we have,

$$\left|1 + j\frac{\omega_u}{\omega_z}\right| \approx \frac{\omega_u}{\omega_z}$$

This is the approximation. If I do this approximation, then we get,

$$\omega_u = \frac{I_{CP}K_{VCO}R}{2\pi}$$

(Refer Slide Time: 18:48)



So, we have seen the loop gain of the PLL in order to calculate the phase margin of the PLL. This is equal to the separation between your actual phase and $-180°$. So, let me just redraw this where you start from $-180°$ and after sometime this goes to $-90°$. So, given the ω_u frequency, this is the value which we need which is going to be,

$$\varphi_m = -180° + \tan^{-1}(\omega_u RC_1) - (-180°)$$

$$\varphi_m = \tan^{-1}(\omega_u RC_1)$$

Now, the question is how to find ω_u? Well, for unity gain frequency ω_u, you have,

$$|LG(j\omega_u)| = 1$$

So, you find the ω_u from that loop gain expression or you can also write it as,

$$\left|\frac{I_{CP}K_{VCO}(1+sRC_1)}{2\pi s^2 C_1}\right|_{s=j\omega_u} = 1$$

Now, here I can do one substitution by approximating the following:

$$\frac{\omega_u}{\omega_z} \gg 1$$

$$\Longrightarrow \frac{I_{CP}K_{VCO}\omega_u RC_1}{2\pi\omega_u^2 C_1} = 1$$

Given this approximation,

$$\omega_u = \frac{I_{CP}K_{VCO}R}{2\pi}$$

So, you can substitute this back here in the phase margin stuff and this is going to be your ICP KVCO by 2 pi into R divided into RC1. So, this will give you the phase margin for the PLL and looking at the plot, we know that the phase margin is greater than, or it is very close to 90 degree. So, this system is going to be quite stable. If you have a zero, that is why we earlier also introduced the zero to make the PLL stable. Thank you.

So, you can substitute this back here in the phase margin and we get,

$$\varphi_m = \tan^{-1}\left(\frac{I_{CP}K_{VCO}R}{2\pi}RC_1\right)$$

So, this will give you the phase margin for the PLL and looking at the plot we know that the phase margin is close to 90°. So, this system is going to be quite stable if you have a zero, that is why we earlier also introduced the zero to make the PLL stable. Thank you.