Phase-Locked Loops
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Lecture – 23
Digital Frequency Detector

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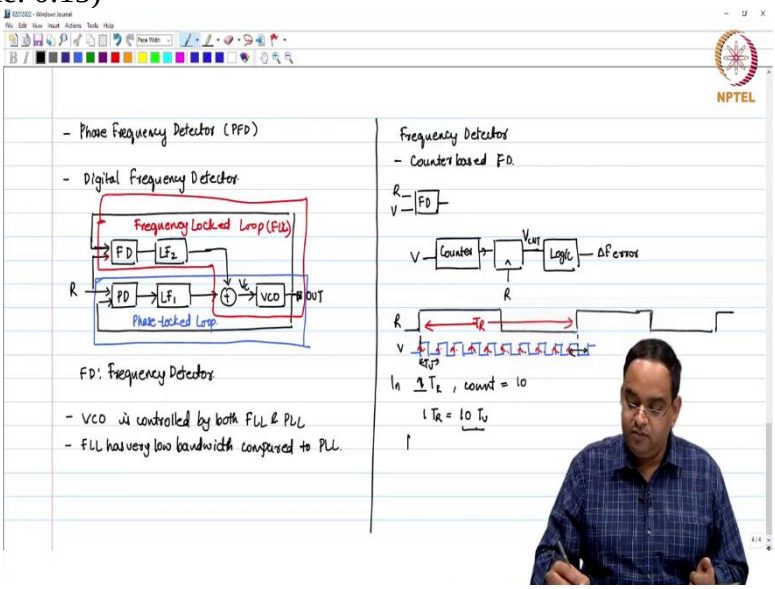

Welcome to this session. In the previous session, we talked about Phase Frequency Detector (PFD) whose average output voltage was proportional to the phase error and in the presence of frequency error also, the average output voltage of PFD has the correct sign for the given frequency error. Now, there are other blocks which can also detect the frequency and you can say that these blocks are other methods for frequency acquisition. These are digital frequency detectors.

You can ask a question that why do we need that, well, we know that the phase detectors like EXOR gate based or S-R latch based phase detectors, if you think about it, they are quite simple as compared to the PFD. PFD uses two D flip-flops and one AND gate while the EXOR gate PD uses just one EXOR gate. So, sometimes you would like that you can use that phase error detector but in order to avoid the problems in the presence of frequency error, you need a frequency detector separately.

So, first, where it will be used, well, you can have a dual loop PLL where you have the phase detector, all the phase detectors which we have talked so far, with a loop filter, let us say, LF_1, and then that controls the VCO. I will tell you why I am using the plus sign, well you have a VCO and this is one loop. Then in the other case, what you can do is, you can have a separate frequency detector FD, you can have another loop filter, LF_2, depending on your loop

requirement and this is going to add to the control voltage. The output of the VCO will go to the frequency detector and the reference goes to both. So, this is the reference, this is the OUT. FD here refers to Frequency Detector.

This is the control voltage, the control voltage is coming from two loops, one is phase detector loop, and the other is from the frequency detector loop. This loop where you normally correct the phase error is called as PLL loop, Phase-Locked Loop. Do not think that in case of phase-locked loop, we will not change the frequency, well, at the end it is also changing the frequency of the oscillator.

But at any given instant of time, we are measuring the phase error between the reference and the output signal. Whether that phase error is coming because of the frequency error or because of phase error itself, that is not taken into account. The only thing which is taken into account is what is the phase error right now. You have phase error due to some phase change in the loop or because of the frequency error, that is immaterial.

In the other case, where you have the frequency detector loop, here you do not worry about the phase error, you actually worry about the frequency error only. So, this loop is called as Frequency Locked Loop, FLL. So, one is PLL, and the other is FLL. Both these loops have their own functions. In the PLL loop, you will correct for the phase error, and in the FLL loop, you will correct for the frequency error. If you are using both these loops, then you can use EXOR based PD without worrying about the frequency locking. The frequency locking will be taken care of by the frequency locked loop.

The important point here is that the VCO is controlled by both FLL and PLL. Now, this is a problem, so it is like you are having one block which is controlled by two different loops, so the two loops should control it in such a way that they do not oppose each other. If the frequency locked loop is trying to increase the frequency, at the same time if your PLL starts reducing the frequency, it will create a bigger problem.

So, in general, what we do is, FLL has a very low bandwidth as compared to PLL. You can design as per your requirement, but you have the option here to correct for the frequency separately and for the phase error separately. Now, given the need for such frequency detectors where I am only worried about the frequency and not the phase error, there are a couple of options.

Let me just write frequency detector, the first one is counter based frequency error detector. So, what is this counter based frequency error detector? Well, it is simple, so, you have FD and the output, let us treat this output as a digital output, this is R and this is V.

So, somehow the output of the FD should reflect the frequency error, so the way you can do it is, you can have a counter. You can feed V signal to the counter and at the output of the counter, you have another block which is clocked by R. So, every rising edge of R, you can actually add the value, you can give the value of count, V_{CNT}, there is some logic here now. At the output of the logic, you will get the frequency error. How? So, if I have the reference clock like this and the easiest way to find the frequency error is because R acts as a reference, so, if I have my V clock, I just keep on counting.

So, here is just an example. So, if you look at it, in one reference period, I will check how much I have counted. So one reference period, I am going to count the rising edge, let us say, so, at every rising edge of the V signal, you increment the count by 1, so I have 1, 2, 3, 4, 5, 6, 7, 8, 9, 10. So, in one reference period, because I was counting rising edge, so I counted in one reference period, the count value is 10. So, 4, 5, 6, 7, 8, 9, 10, so count value is 10.

So, approximately, you can say, $1T_R = 10T_V$. Now, you will say that it is not $10T_V$ because the whole cycle is not included in the reference period, well, that is the error which you will have to deal with, you cannot avoid that error. So, it is like this, if you look at it, it is not 10, it is actually you can say 9.5. So, this 0.5 times T_V or the V period is the error which you may anyways have.

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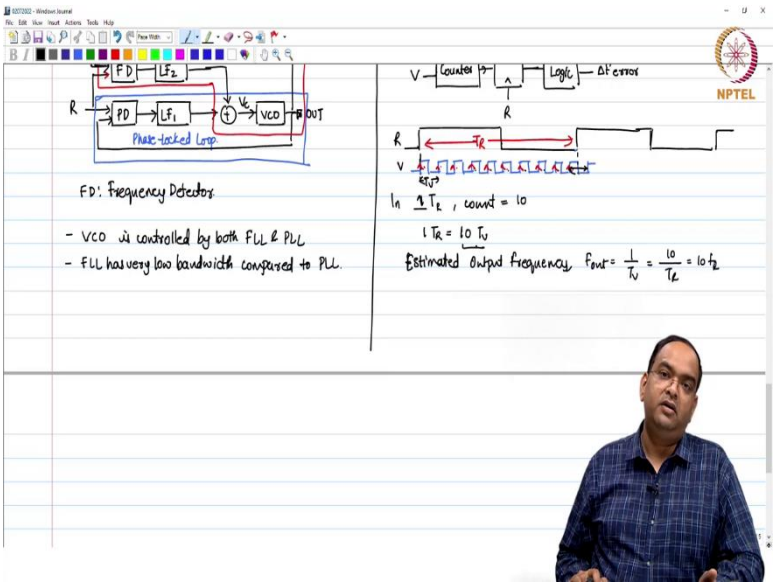

So, if someone wants me to find the frequency of the V signal, well, from here, the estimated output frequency f_{out} is given by,

$$f_{out} = \frac{1}{T_V} = \frac{10}{T_R} = 10 f_R$$

So, in this way, you will know what frequency error you have.

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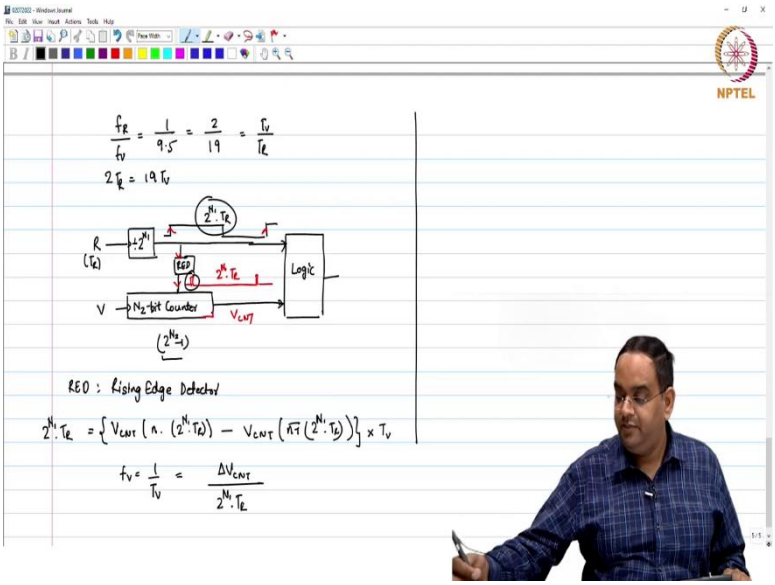

Now, here the thing is that we are counting only with respect to one reference period. Sometimes, you will see in one reference period we are not going to get more accuracy. What it means is if you look at it, in case, it will be easier to understand from here. In our previous example, we had,

$$\frac{f_R}{f_V} = \frac{1}{9.5} = \frac{2}{19} = \frac{T_V}{T_R}$$

So, f_V was 9.5 times larger than f_R which means that if I take $\frac{2}{19}$ which is $\frac{T_V}{T_R}$, so, we will have 2 times the reference period equal to 19 times the T_V period. So, if I happen to take two reference periods and count in two reference periods, I will be counting 19 times the T_V period. And then if the count after two reference cycles happens to be 19, then my estimate for the V frequency or the V signal will be more correct.

So, as you increase the time period for counting, your estimate for the frequency will also improve. So, in order to do that, what we can do is, we can actually improve our counting. So here, you see another counter based frequency error detector. First, what I will do is, on the

reference signal, I will add a reference clock divider. So, when I have a reference clock divider $\div 2^{N_1}$, then if I have a reference period T_R, the period of this particular output clock is going to be $2^{N_1}.T_R$, so you increase your counting period.

Then, you take a counter, here you are counting V signal and you make it like a N_2-bit counter, what does N_2-bit counter mean? It means that the maximum count value which you are going to have here is $2^{N_2} - 1$, that is the maximum count. You say, you are doing a binary counting here, so it is like this is going to be counted with the help of an accumulator digitally, so you will define the number of bits which are used in the counter. So, when I say it is N_2-bit counter, it means that the maximum count value this particular block can have is $2^{N_2} - 1$.

Now, what we are going to do is, we feed these two signals to a logic and here, we have a circuit called RED which is Rising Edge Detector. RED stands for Rising Edge Detector. So here, what you are going to do is, whenever you get a rising edge, you actually generate a pulse here, so these pulses are going to be generated at the rate of $2^{N_1}\ T_R$ and whenever you get the rising edge detector high, you pass V_{CNT} signal to the logic.

So, whenever you get this, you pass V_{CNT} signal to this logic and then you will look at the previous count value and you will look at the current count value, so, you can say,

$$2^{N_1}.T_R = \{V_{CNT}(n.(2^{N_1}.T_R)) - V_{CNT}((n-1)(2^{N_1}.T_R))\} \times T_V$$

This is the actual count value which you registered in one period here.

So, from here, we can actually calculate f_V which is given by,

$$f_V = \frac{1}{T_V} = \frac{\Delta V_{CNT}}{2^{N_1}.T_R}$$

So, you can calculate the frequency, you know whether you have the frequency error or not and based on that you can correct it in the frequency locked loop.

We will look at different implementations for the frequency error detector and the phase error detector in due course of time. But these are the phase error detectors and the frequency error detectors which we use commonly. The circuit level implementation will be seen later. Thank you.