Phase-Locked Loops
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Lecture – 20
Digital Phase Error Detectors: Part II

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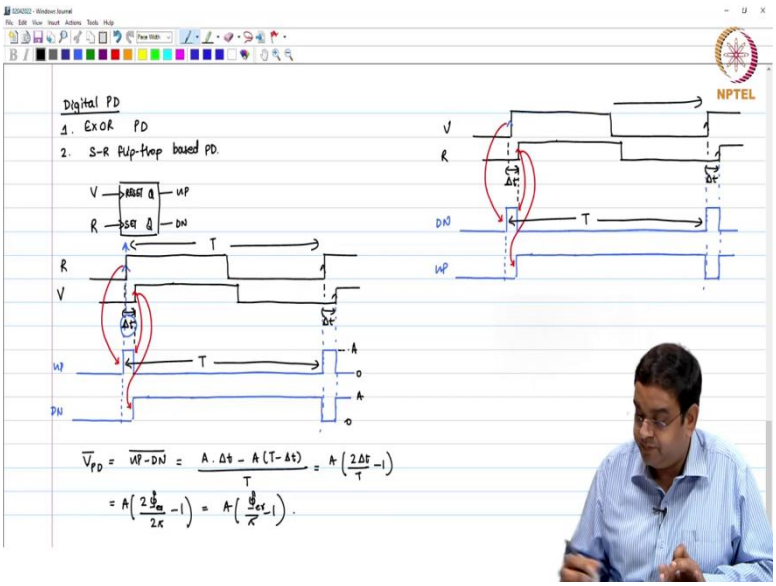

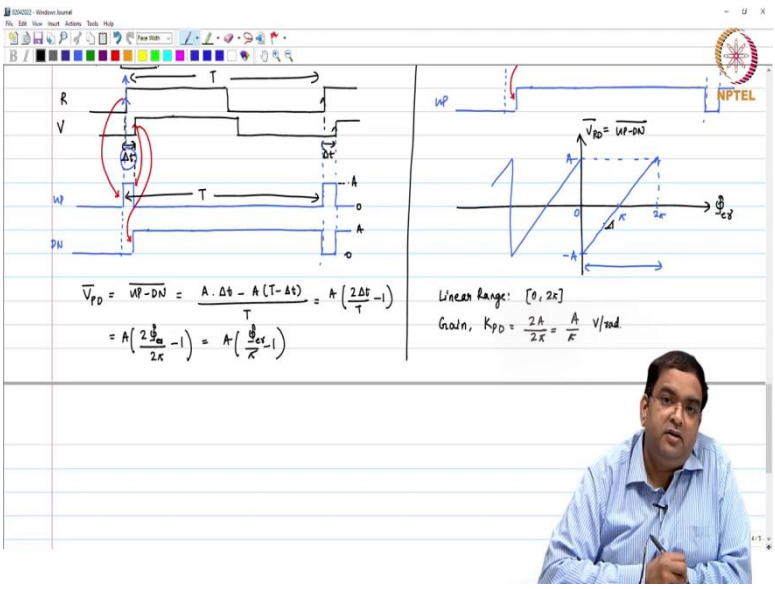

Welcome to this session. In the previous session, we looked at digital EXOR based phase detector under digital PDs. So, this is what we looked at and the problem which we found in the Exclusive-OR gate PD was that V_{PD} or the output of the phase error detector was actually depending on the duty cycle of the clock signals.

So, what we plan to do is that we plan to have a phase error detector which does not depend on the duty cycle of the clock signals. So, let us look at it. So, the other one is S-R flip-flop based PD and this particular phase error detector tries to overcome the problem which we had with the Exclusive-OR gate.

So here, you have S-R based phase error detector. So, what I will do is, I will say, you have inputs R and S, for example here, this is reset and the other one is set, you can call that. Well, you can put it on any side and then you have Q and $\bar{Q}$ which I call, let us say, UP and DN. This is just a terminology. So, what happens here? Let us look at it. Let us continue with our signals R and V, I think that would be better.

So, we have our R signal which is like this and V signal is nothing but the same signal shifted by time if the frequency is same, you have been dealing with that. The time period is same for both the cases, this is R, this is V, same Δt here, Δt here. So here, let us say you start at this particular time, as the R signal goes high, the UP signal will go high, and when the V signal goes high, the DN signal will go high and UP will go down.

So, it is like this goes high and UP signal comes down. So, this particular configuration makes whichever signal goes high first, it is going to set the Q and $\bar{Q}$, UP and DN. So here, R signal goes high, UP goes high first and then when as soon as V signal goes high, DN goes high and UP goes low.

Now, this is for one particular case. Also, it is not susceptible to the falling edge of the clocks, this is not susceptible to that, this will remain like this and this is going to be in the same manner. Next, again for the rising edge on UP, it goes high and then you again get this, this goes low, here you get rising edge on V. So, it will go high again and this will go low. So, this repeats at every clock period T. Just for an example, what I am going to do here is that I am just going to interchange UP and DN. Now this becomes R and this becomes V which means UP and DN are swapped, nothing much.

So, depending on which signal comes first, the phase error will be either positive or negative. This will be decided by which signal comes first here. Now for this Δt error for the same frequency signals, what is the average value of V_{PD}? So, this is measured as the average of the difference between the UP and DN signals, and is given below.

$$\overline{V_{PD}} = \overline{UP - DN}$$

As per the convenience, I choose whether I want signal amplitudes as A and $-A$ or I want A and 0. So here, I am going to choose this as A and 0, you can choose anything which you like. So, this is A and this is 0 here. So, we get,

$$\overline{V_{PD}} = \frac{A.\Delta t - A(T - \Delta t)}{T}$$

$$\overline{V_{PD}} = A\left(\frac{2\Delta t}{T} - 1\right)$$

$$\overline{V_{PD}} = A\left(\frac{2\varphi_{er}}{2\pi} - 1\right)$$

$$\overline{V_{PD}} = A\left(\frac{\varphi_{er}}{\pi} - 1\right)$$

So, let us just draw this phase error versus $\overline{V_{PD}}$ or defined as $\overline{UP - DN}$. At phase error equal to zero, the value is $-A$ and at phase error equal to 2π, the value is A. As phase error is equal to π, this is zero and it is linear in this range and what you will find is that as the phase error exceeds 2π, this is going to repeat. So, what you see here is that for phase error lesser than zero, you will see characteristic like this, you can plot it.

So, let us focus on this particular part which is between the range 0 to 2π. So, the problem which we had previously with the duty cycle of the clocks between which the phase error is measured, that problem is no more there. Then the linear range in this case has been extended to $[0, 2\pi]$. Earlier in case of the EXOR based PD, you had range $[0, \pi]$, here it is $[0, 2\pi]$. What is the gain of the PD? The gain is given by,

$$K_{PD} = \frac{2A}{2\pi} = \frac{A}{\pi} \text{ V/rad}$$

So, again, a digital block inherently non-linear gives you a linear gain with respect to the phase error. So, if you compare this particular phase error detector with respect to the Exclusive-OR based phase error detector, so, let us just look at it. So, I will take one example.

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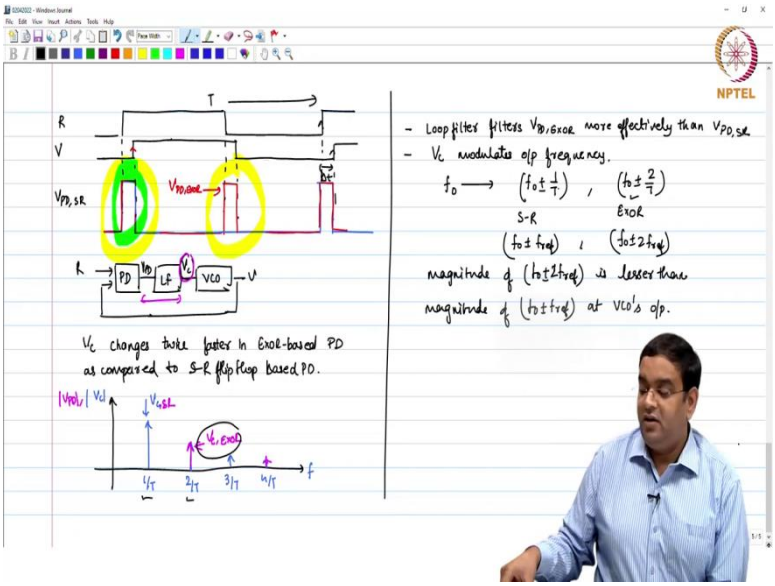

So, for this particular S-R flip-flop based phase error detector, if you have R and V signals like this, I am just going to look at V_{PD} and V_{PD} is measured as $UP - DN$ in this case. So, V_{PD} in our case is going to be something like this whereas if the same two clocks R and V were given to the EXOR based PD, in that case you would have got, so, this is $V_{PD,SR}$ and now I will plot V_{PD} in EXOR case.

So, V_{PD} in EXOR case is, this is going to be something like this, there I used A and $-A$, other than that everything is the same, it is going to be like this. So, the red one is $V_{PD,EXOR}$ one. Now, what is so important about it? Well, in the PLL, you have phase detector followed by loop filter and then VCO, this is R and this is V, you can think about it right now, this is V_{PD} and this is V_c.

So, in case of EXOR based phase error detector, V_{PD} is changing twice every clock period. What are these two instants at which V_{PD} is changing? One is this and the other is this. Every clock period, it changes twice whereas V_{PD} for the S-R latch based phase error detector changes only once. So, if that is the case, it translates to that the control voltage of the oscillator (V_c) changes twice faster in EXOR based PD as compared to S-R flip-flop based PD.

Well, so, what is the bigger problem if your PD is changing twice? So, let us just look at the control voltage spectrum. This is not accurately to the number which I am plotting. It is just showing what frequencies you are going to have. So, the S-R latch based PD will have the fundamental frequency as $\frac{1}{T}$ and then you will have second harmonic and third harmonic for

that frequency. So, $\frac{1}{T}$, $\frac{2}{T}$, $\frac{3}{T}$, $\frac{4}{T}$ and so on whereas what you are going to see for this one is, by the way, this is for V_c in S-R flip-flop based PD you will see such kinds of components with respect to f. I am plotting the spectrum of the control voltage in the two cases. Now, for $V_{PD,EXOR}$, the first frequency comes here. Right now, we are not talking about the magnitude, we are just talking about the frequency here. So, the first frequency comes at here, then you will have a component at $\frac{4}{T}$ and so on. So, this one is V_c for EXOR based PD. The control voltage spectrum is like this.

It is the same thing whether you look at V_c or you look at V_{PD}, same things are going to happen at V_{PD}. So now, if you are having any loop filter between V_{PD} and V_c, two things will happen. The first thing is that the loop filter filters $V_{PD,EXOR}$ more effectively than $V_{PD,SR}$. The simple reason is because the fundamental frequency component in $V_{PD,EXOR}$ is at a higher bandwidth, that is why if you keep the same loop filter bandwidth and you give $V_{PD,SR}$ and $V_{PD,EXOR}$, well, the EXOR case has its fundamental frequency at twice the frequency in case of S-R. So, obviously it will filter it more.

Also, you have seen that the control voltage of the oscillator modulates the frequency of the oscillator. So, V_c modulates the output frequency. This is something which you may remember by now, the other thing is the magnitude. So, effectively, whatever the oscillator frequency f_o you have, then you are going to have f_o, here it is $\frac{1}{T}$ in this case, $f_o \pm \frac{1}{T}$, you will get these frequencies. You are going to get these frequencies in case of S-R based PD whereas you are going to get $f_o \pm \frac{2}{T}$, that is the first modulation in case of Exclusive-OR or EXOR gate based PD. So, you get these frequencies at the output and normally this $\frac{1}{T}$ is not written as $\frac{1}{T}$, it is written as f_{ref}. So, we have $f_o \pm f_{ref}$ for S-R flip-flop based PD and $f_o \pm 2f_{ref}$ for EXOR based PD.

So, the frequency modulation happens in case of the EXOR gate at higher frequency. Also, the magnitude of $f_o \pm 2f_{ref}$ is lesser than the magnitude of $f_o \pm f_{ref}$ component at the output of the VCO. You can use the same VCO in both the cases, but you will see that the magnitude of the unwanted component which is $f_o \pm 2f_{ref}$ in case of EXOR is lesser than the case of S-R.

So, now you see there is some good part and some bad part to both the designs. The good part with EXOR is that the unwanted frequency modulation which is done for the VCO because of

this phase error detector appears at higher frequency and it is more filtered. So, the magnitude is going to be lesser. This is the good part. The bad part is that it is susceptible to the duty cycle of the clocks which are used for the phase error detection. So, based on your choice, what you can do is that you can choose either of these phase error detectors. Let me stop here.