Phase-Locked Loops
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Lecture − 2
Course Introduction and Motivation: Part II

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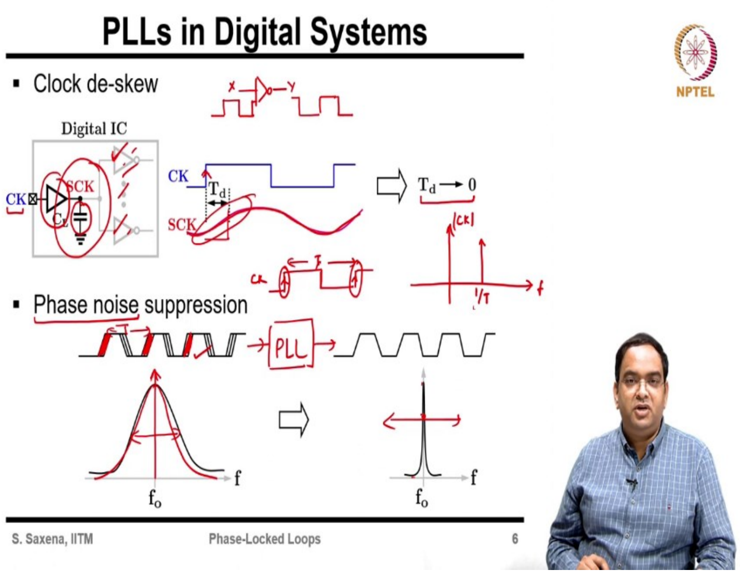

So, learning about the PLL is quite interesting, and if you know how to design a PLL, you can help design a wireless IC, wireline IC, ADC IC, digital systems and many more things. Now, the question arises is, see, we need PLL in all these cases to generate the high frequency, to generate the clock. Let me not use the term high frequency for now. Are there any, if the nature around you which has so much of periodicity associated with it in days, years and everything, do we have something in nature which can give us what we want.

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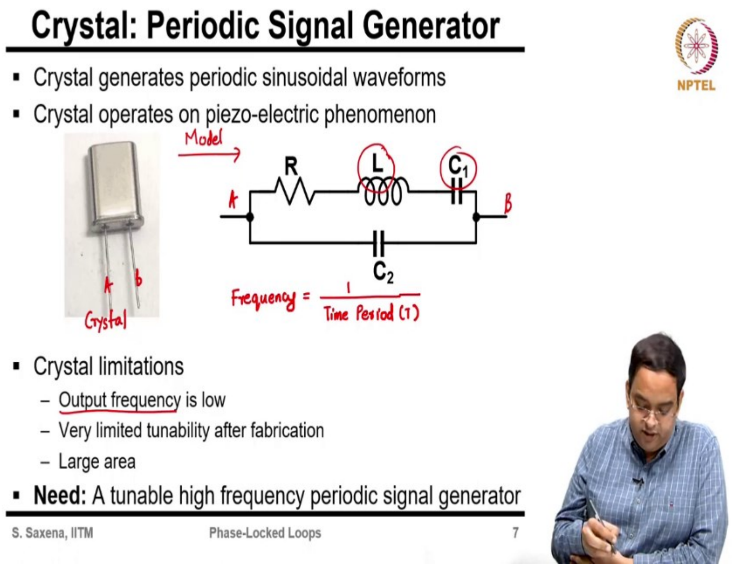

And it is not to our surprise that there is something which generates a really good signal. Good signal is lesser phase noise, the thing which we just saw. Very highly accurate periodic signal kind of requirements, we have something called as crystal. I am just showing you a packaged photo of the crystal.

So, crystal works on the piezo-electric effect. It generates periodic signals and depending on how you use it with the associated circuitry, you can get periodic voltage or current signals. The basic phenomenon behind the operation of the crystal is piezo-electric effect. You can get periodic signals in voltage or current form.

This particular crystal is manufactured, there is not much electronics involved with this. You can model this piezo-electric crystal. Because we are all electrical engineers, you would like to model this thing using the electrical components which we easily understand. So, this is the RLC model of the crystal between its two terminals A and B.

The frequency of oscillation or the frequency or the period at which you will see periodic waveforms at the terminals A and B is related to these L and C components, and the effective value of this inductor L and capacitor C_1 depends on the physical dimension of the device which is crystal. So, L and C here, they are not real inductors and capacitors which are present inside the crystal. They are modeling the operation of the crystal. And you can say, the value of inductor you are using to model depends on the dimensions of the crystal. So, these are like the fundamental sources of your periodic signal generator which you have easily available. And these crystals generate really good highly accurate periodic signals. And they are mechanical devices by the way. Now, if we have such a good device available with us, then why do we need PLL? The answer to that is, if the crystal is so good, if something is too good, there is some kind of drawback which is normally associated with it. It is not always the case, if everything is good, it is like too good to be true.

So, in this particular case, what you see here is that the limitations of these crystals are the output frequency is low. Here, the frequency is the frequency at which your crystal oscillates, it is nothing but $\frac{1}{\text{Time Period}}$. So, the frequency at which these crystals oscillate is quite low. It is very difficult to have crystals which oscillate at a very high frequency or very low time period and are accurate. So, it is not that easy and not viable. The other drawback of the crystal is that once you fabricate the crystal, see this is like a device whose frequency depends on the physical dimensions of the device. So, once you fabricate the device, there is hardly any kind of tunability which you have available at your end to change these to change the frequency of the device, it is not possible. You may lower it using some other thing, but it is not possible to increase the frequency at all. If you want to change the output frequency, there is no other option but to use a different crystal. Now, just think about it, in your wireless application, in your GSM standard, there are so many channels. For every channel you cannot use a different crystal. The dimensions are quite large.

So, you cannot use crystal everywhere. And the area is also large. The area will be of the order of going by few millimeters by few millimeters to centimeters also. So, because of these drawbacks associated with the crystal, we need a clock generator, a periodic signal generator which can generate a high frequency which is tunable with low phase noise, as we learnt in the previous slide or a low disturbance in the clock signal. But one thing is sure that, see, you have a crystal which is really good, which has very little disturbance in the period, you have very little disturbance, now when you try to generate clock at a higher frequency, there is some cost associated with it. So, generating a clock which has disturbance lesser than the crystal may or may not be possible. So, crystal acts as a reference clock for high frequency clock generator. And we will see how to use it. But crystal as such cannot be used as a high frequency clock generator for the reasons which we just discussed. So, now we need to understand exactly what kind of periodic signals we are looking at, what do we mean by disturbance, what we are going to do in the PLL. One thing which we know is that crystal generates a lower frequency while we need to generate higher frequency and we need to tune the output frequency also. But in the process of doing all that, we will have some problems, and we will try to overcome them.

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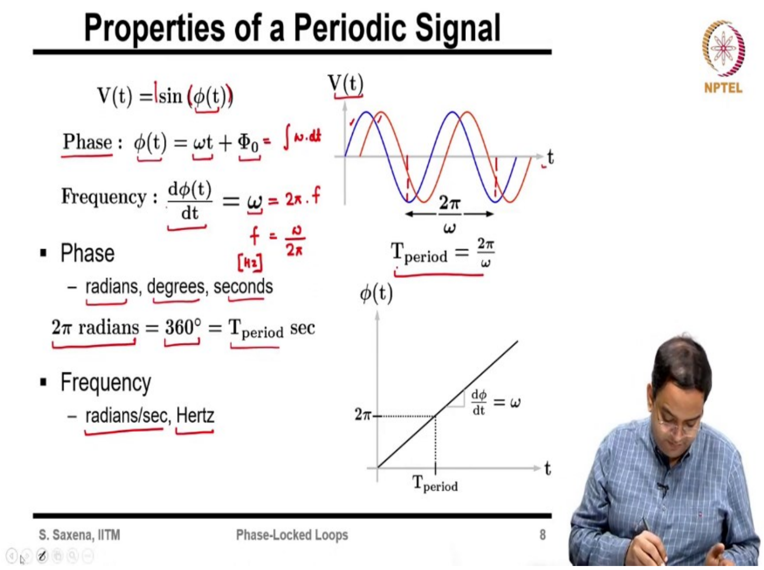

So here, this is a very simple slide where I show you the terms which are associated with the periodic signals and are used during the course. So here, I show you a voltage waveform with respect to time and this is a sinusoidal waveform. We have defined the period T_p here, earlier only T now T_p. This is the time period after which the signal repeats. And you see the two sine waves, one in blue and the other in red. Both the sine waves have the same period T_p. They are just shifted in time.

So, this signal V(t), the way it is drawn here, can be written as $sin(\varphi(t))$. The argument of the sin function, $\varphi(t)$, is called phase. This phase can be written as, in general, $\omega t + \Phi_0$. This is the total phase. The frequency of this signal is defined as the derivative of phase, $\frac{d\varphi(t)}{dt}$, which is normally called as ω. And there are units associated with it. ω is defined in radians/sec. And, $\omega = 2\pi f$, 2π is just a constant. So, the frequency defined in terms of $f = \frac{\omega}{2\pi}$ has units of Hertz. ω has units of radians/sec. Both the parameters are used for frequency.

The phase, on the other hand, is the argument of the sin and frequency is the derivative of phase. You can say the other way also that the phase is $\int \omega\, dt$. So, they both are related. Phase is defined in terms of radians, degrees or seconds. And this you know that 2π radians $= 360° = T_{\text{period}}$ sec. So, these are the basic terms which are associated with the periodic signal. What are they? Phase and frequency. Here, there is no specific amplitude, you can say that the amplitude is 1. Amplitude is not that much important in case of clock generators or PLLs. The argument of this periodic waveform, for example, here it is the argument of the sin function, is much more important. So, when you have a simple sine wave signal, where is the problem?

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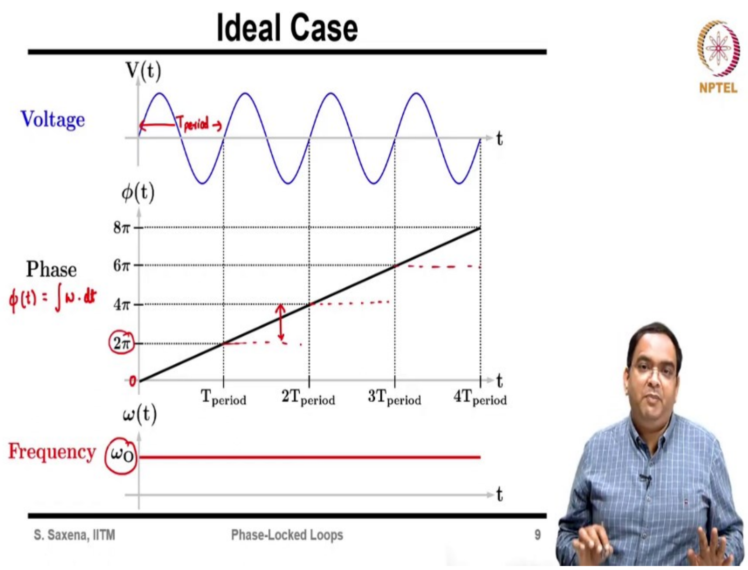

Well, you take an ideal case. In the ideal case, as I have drawn here, the voltage waveform if you look at, the voltage waveform is periodic in nature, sine wave, perfect. The phase, $\varphi(t)$, which is the argument of the sine waveform is defined as the integral of the frequency. So, $\varphi(t) = \int \omega \, dt$.

If this is an ideal periodic sine wave, the period of this signal is fixed. You integrate omega with respect to time. What happens from time instant t equal to 0? Every time period, 0 to T_{period}, you actually accumulate 2π. So, in every time period, the phase argument accumulates 2π. Now, that happens in case of ideal signals. The frequency, ω_0 or ω remains constant. If this is the kind of the clock I have available with me at any frequency I want, I do not have to design PLL. The reason is this does not happen.

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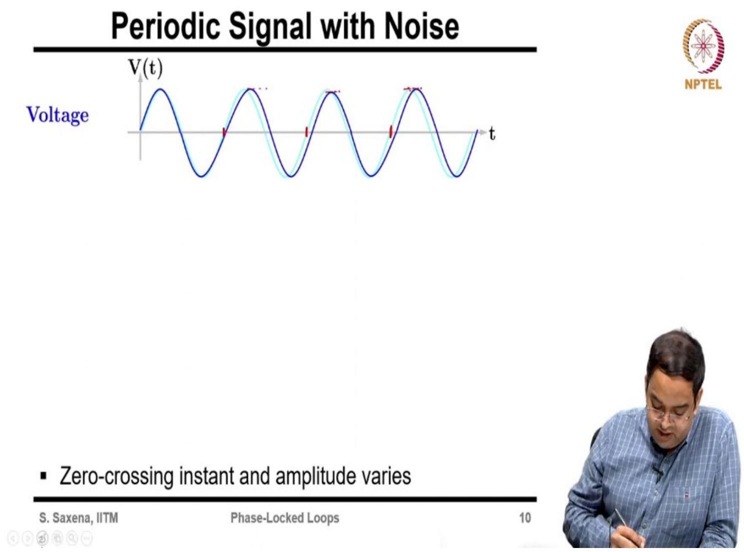

So, what happens? Let us see. Actually, the voltage signal which you see, the one which is shown to you in dark blue color, is the ideal waveform. What happens in practice is, this waveform shifts. Sometimes it may come early, and sometimes it may come late. So, this clock, the one in the light blue color, is the real waveform. Sometimes, even the amplitude is different, though it may or may not be of much consequence. What is of consequence? The zero-crossing point or the actual period of this waveform is changing. So, if you look at the blue waveform, from here to here is one period. From this node to this zero-crossing is another period. So, the period is different. It is not ideal anymore. If this happens, then what will be the case for the phase?

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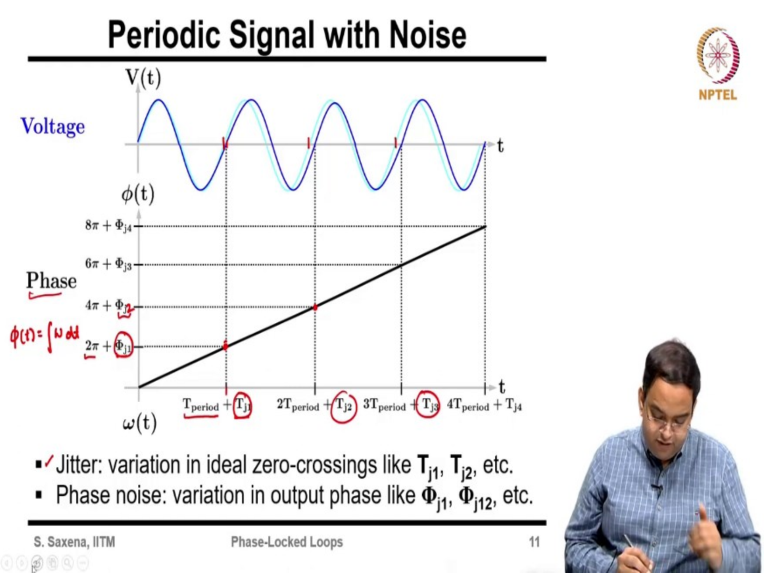

So, I have told you here, if you look at the phase of this waveform, which we know $\varphi(t) = \int \omega\, dt$. So, at this point for the sine wave which you are seeing in light blue color, with respect to the one in the dark blue at that time instant, the period of the one which you have for light blue color, that time instant, you have an extra time T_{j1} between these two. So, the light blue color accumulates phase 2π in lesser time. It accumulates in its time period, but that time period is not the ideal time period.

So, you can look at it in multiple ways. You can either look at the absolute time periods of the new wave or you can look at the total phase accumulated by the corrupted waveform which is the sinusoidal waveform in light blue color, and there you see the phase is different, it is $2\pi + \varphi_{j1}$. Here, it is $4\pi + \varphi_{j2}$, then, $6\pi + \varphi_{j3}$, and so on. When we are talking about the variation in the zero crossing, we are talking about T_{j1}, T_{j2}, T_{j3}, and so on. What is T_{j2}? It is the variation in the time period of the waveform which in normal convention, here, in this particular course, is defined by the term 'jitter'. It is the variation in ideal zero-crossing of sine wave or any ideal clock. When you are talking in terms of the same disturbance, it is the same thing, one is looked at in time domain and the other is looked at in relation to phase. If you are looking at phase which is φ_{j1}, φ_{j2}, φ_{j3}, and so on, that is used to define phase noise. So, phase noise and jitter are related. It is just the way you are defining them. When you are defining in terms of time domain, normally you use the term jitter. When you are in frequency domain, you use the term phase noise. We will look at the relation between the phase noise and jitter in this course for sure.

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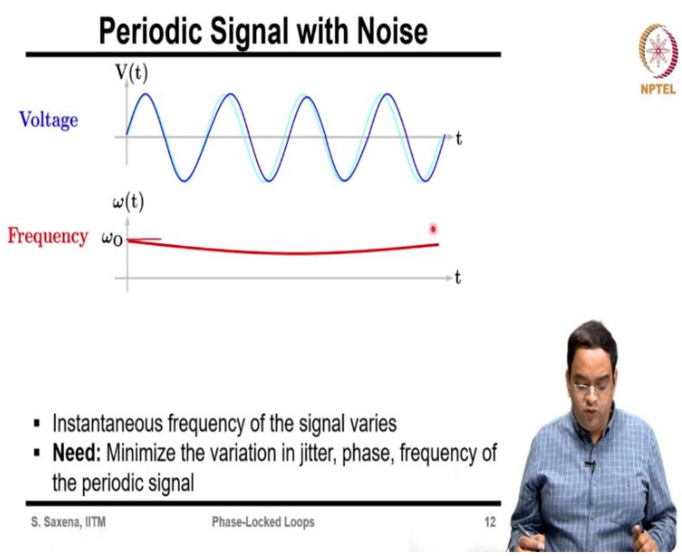

So, if that is the case when our clock waveform is changing, if you look at the instantaneous frequency, this is no more constant. The frequency here is no more constant. It is varying. That is what exists in reality. If you do not do anything and you think that with some or the other block which is on its own, standalone, without any feedback, you can just get the frequency which you want, it does not happen that way. You need some kind of closed loop system to make sure that the frequency does not vary that much, the phase disturbance is not much, the timing variation or the jitter is limited, and it is not that it can be done so, without doing anything. You have to put some kind of logic there, some kind of effort, PLL is all about that.

So, in this particular course, we will see how to minimize this variation in the time domain disturbance, in the frequency domain, and to generate whatever frequency we want. As I told you, the crystals generate only low frequencies and they cannot be tuned once fabricated. We have to design clock generators which can generate a lot more frequencies, are highly tunable at much higher frequencies with lesser amount of jitter. So, we will learn how to do it in a systematic manner.

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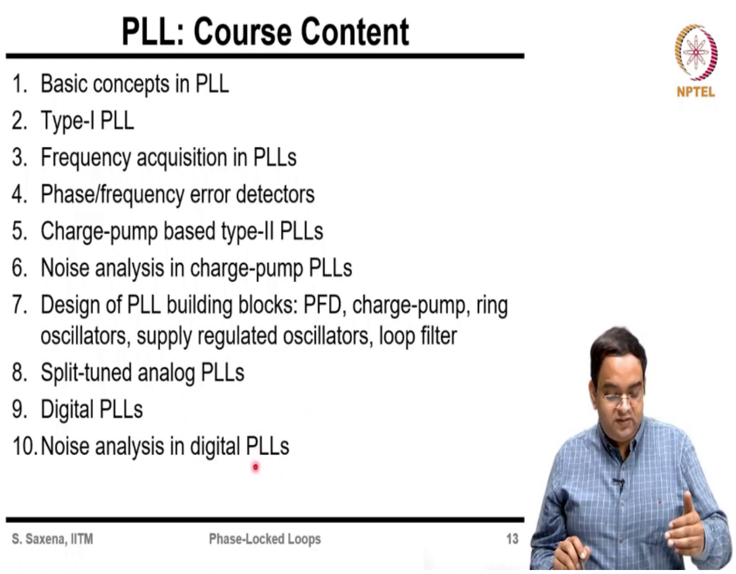

Here is the course content for this course. We will go through the basic concepts in PLL. Then, a very standard Type-I PLL. Later, we will see how we acquire frequencies in PLLs. You start your PLL, it will not be on, it will not acquire the frequency as you desire, it will take some time. Then, we will start designing the PLLs. We will understand how to reduce this error, which block helps in reducing the error, and how to actually measure the error. Then, there will be charge-pump based type-II PLLs. You can say this is the main work force for all kinds of PLLs. You can implement it differently, but the basic logic lies here.

Then, we will see what all noise sources come. You are getting something, so, there will be some problems with that. So, we will do the noise analysis to figure it out and have an efficient design. Then, we will go through all the building blocks of the PLL: PFD, charge-pump, ring oscillator, supply regulated ring oscillator, and loop filter. Later, we will go through the split tuned PLLs. Then, we will see the digital world, how to implement it digitally, what are the benefits and drawbacks of the digital PLLs and the noise analysis in digital PLLs. So, these are the broad topics which we will cover during this course.

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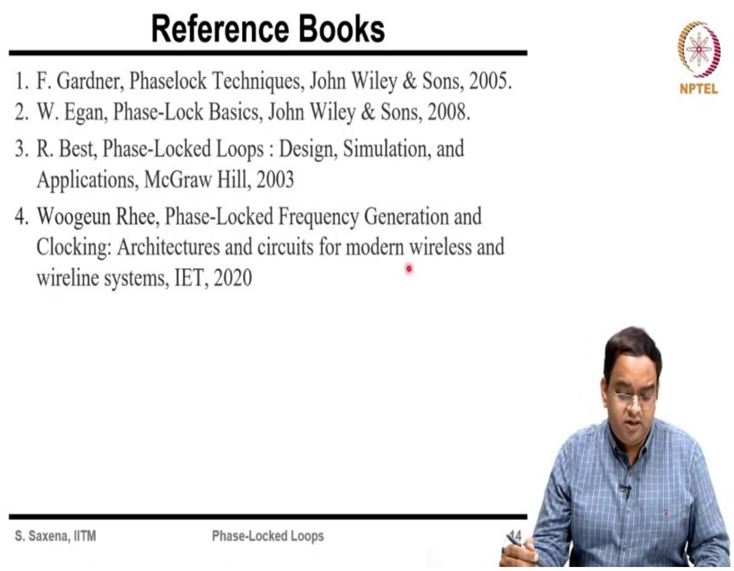

There is no textbook for this course as such, but these are the reference books. Some of them are the first editions while some are second or third editions. So, the first one is by Gardner, it is a very old book, like a fundamental for PLLs. Then, you have the ones by Egan and R. Best, and then this is a recent book, which is not only about PLLs, but it is about other blocks also which use PLLs. So, it is Phase-Locked Frequency Generation and Clocking which is used for wireless as well as wireline applications, how the clock requirement changes as per the application. So, this is all about those particular clock generations. You can read as you like. We do not prescribe any particular textbook for this course. So, let me stop here. We will start with the basic concepts of the PLL in the next class. Thank you.