Phase-Locked Loops
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Lecture – 18
Analog Phase Error Detectors: Part II

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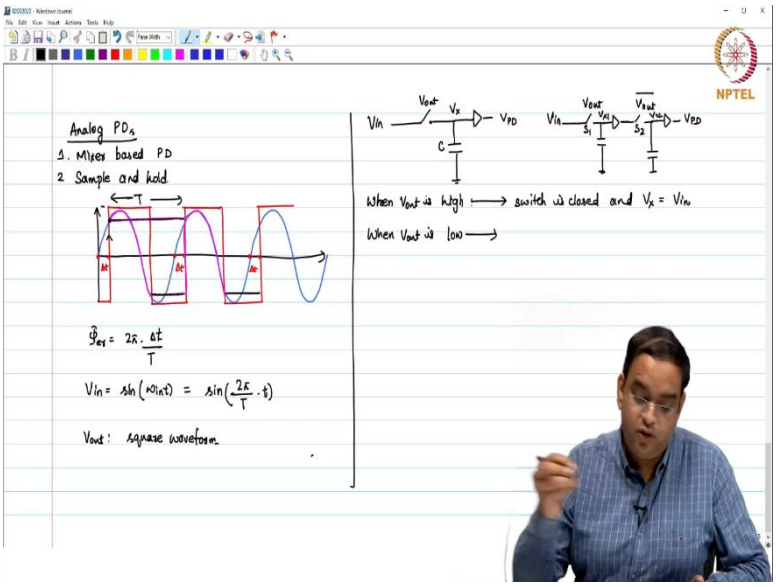

In the previous session, we looked at the first analog phase detector which is the mixer based phase detector. So, let us continue with that. These are analog PDs. The first one was mixer based, and the second one which is interesting is sample and hold. So, as we have the term sample and hold, you can just think about it that there should be something which is sampling the clock. So here, normally you have two clocks, one a sine wave, and the other a square wave.

That will make life much better here. So, I will draw the sine wave and the other waveform which we have is a square wave. So, I will just show you the square wave, maybe like this. And I am assuming here that the frequencies of the two waveforms are same. So, the time period is same. The only thing is that their zero crossings are not matched. So, this Δt is same in all the cases, Δt, Δt, Δt. I want to detect this Δt or the phase error which is proportional to Δt.

So, the phase error is given by,

$$\varphi_{er} = 2\pi.\frac{\Delta t}{T}$$

where, T is the time period of both the waveforms. So, I will write the input voltage as,

$$V_{in} = \sin(\omega_{in} t) = \sin\left(\frac{2\pi}{T}.t\right)$$

The output voltage (V_{out}) is a square waveform as shown to you here. I want to detect this phase error. The method which you can use here is sample and hold.

So, what is this sample and hold? Well, you give this input signal V_{in} to a switch which connects to a capacitor C. Also, I am having a buffer and the output here is V_{PD}. The switch is controlled by V_{out} signal. Please note here that both of these things can be exchanged which means that V_{in} can be used to control the switch and V_{out} can be the other one. It can be either way. But the only thing is that one is a sinusoidal waveform, and the other is a square waveform. So, you can do it both the ways.

So here, this voltage is V_X. So, what happens in this case? When you close the switch, when V_{out} is high, here high is the positive amplitude, what you have is that the switch is closed, and $V_X = V_{in}$. When V_{out} is low, whatever value of V_{in} you have previously, that value will be held on the capacitor. So, in this example, just think about it that when the switch is high like the red one here, the V_X voltage is going to be equal to the V_{in} voltage. So, V_X is going to track this. Also, when V_{out} voltage is low, at that time V_X will not track V_{in}. It will actually hold this value. Then again, when V_{out} comes, it is going to again going to track this input and it will again hold this value. So, you see in this particular case, what is happening is that the value which I am holding here, this value is like a sampled value of the sinusoidal waveform.

You have multiple ways in which you can implement this particular circuit. And depending on how you are implementing this sample and hold, you will actually get V_{PD}. But it is only the shift which you will change. If the two frequencies are same, this held value is always going to be the same.

For example, if I implement a block here where whatever value you have at the rising edge, that value is sampled and it is held. Let us say, if we implement the sample and hold circuit like that, that value will be held. Yes, it will be like this, which I can do it, I will just plot it with a different color.

So, let us say, I have this switch connected to the capacitor, I use a buffer and then another switch connected to this capacitor. This output is V_{PD}, where this is working at V_{out} and this is

working at $\overline{V_{out}}$. When I say $\overline{V_{out}}$, that means when V_{out} is low, at that time the switch will be closed. So, this is S_1 switch, this is S_2 switch and this is V_{in}. This is V_{X1} and this is V_{X2}.

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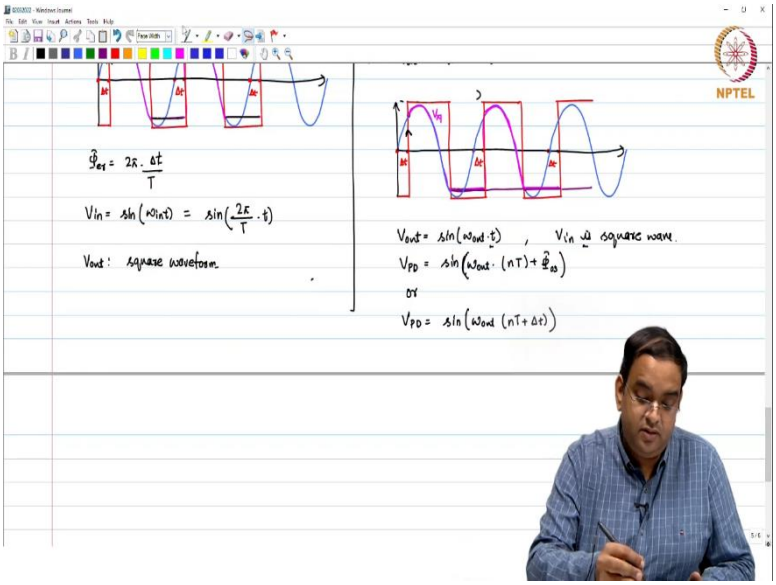

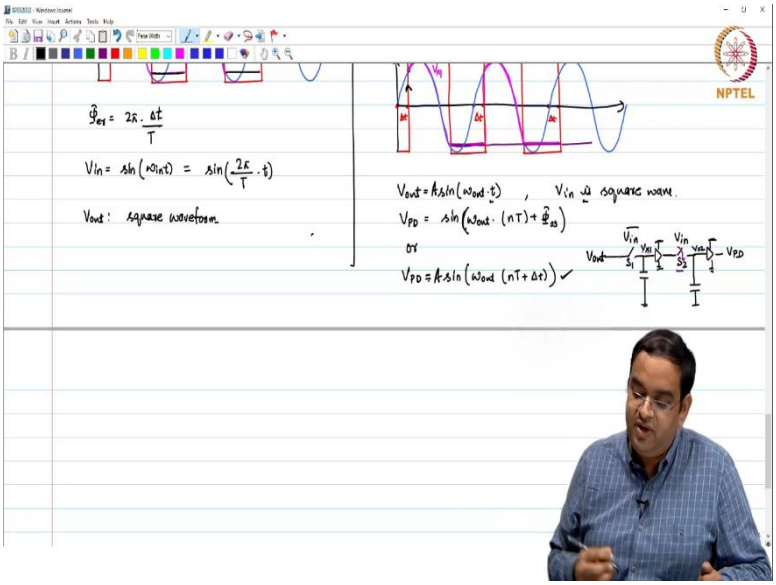

So, V_{X1} is shown to you in magenta and this is V_{X2}. So, V_{X2} is actually, if you look at it, when V_{out} is low, that time this switch closes, and whatever value you have at V_{X1}, that value is passed. So, whatever value you have, this value is passed to V_{X2} and when the clock is high, whatever value you have, that value will be held like this. So, you will always keep the same value.

So, based on the sample and hold circuit, you will sample at one particular point, and based on that, you will get V_{PD}. So, we have,

$$V_{out} = \sin(\omega_{out}.t)$$

I am just changing the waveform for V_{in} and V_{out} here. So, $V_{out} = \sin(\omega_{out}.t)$ and V_{in} is the square wave. You can do it either way. So, I am showing you both the ways, that is why do not get confused here. It is possible in both the ways. So, I sample this t at nT. This is what I am sampling, and this can have some offset. Hence, V_{PD} is given by,

$$V_{PD} = \sin(\omega_{out}.(nT) + \varphi_{os})$$

Either $\sin(\omega_{out}.t)$ can have an offset or V_{PD} can also be given by,

$$V_{PD} = \sin\big(\omega_{out}.(nT + \Delta t)\big)$$

Either case is fine.

So, the waveform which you are seeing here at the top, $\sin(\omega_{out}.t)$ is a sine wave with phase offset of 0, the square wave is actually coming at some Δt time away. So, it is sampling the square wave at Δt time, and if that is the case, then the sampled value is going to be like this. This expression $nT + \Delta t$ will follow the phase error detector which I will just show you here.

So, what I am going to do is that I will just write this particular expression. Because V_{in} and V_{out} have changed their roles, so, this is V_{out}, this one is $\overline{V_{in}}$ and this is V_{in}. Please try to draw these waveforms so that you are sure that how I came up with this expression.

Now, depending on the V_{DD} and ground of the buffers which you are using, the value which you are going to have at the output will be limited by the V_{DD} of these buffers. It cannot be more than that. So here, I am just using the initial sine wave which I had has amplitude 1. If that has any amplitude, that will also be reflected. So, if this happens to be $A.\sin(\omega_{out}.t)$, then, we will have V_{PD} as given below.

$$V_{PD} = A\ \sin\big(\omega_{out}.(nT + \Delta t)\big)$$

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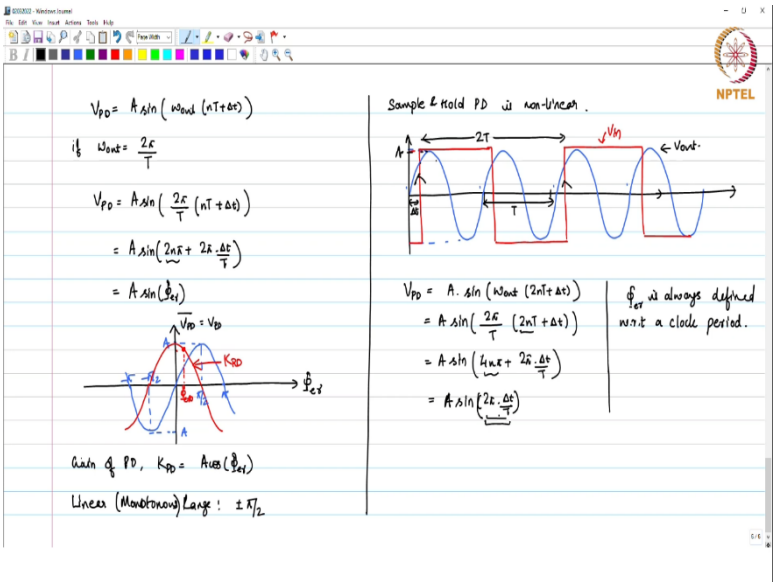

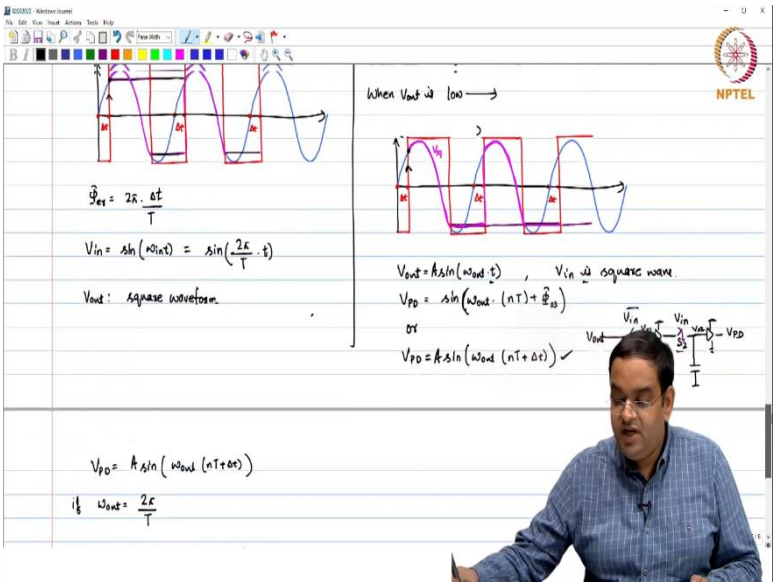

If the two frequencies are same, then, we have,

$$\omega_{out} = \frac{2\pi}{T}$$

This is because T is the time period of the square wave clock waveform which is the input frequency, so, $\frac{1}{T}$ is the input frequency. Then, we have V_{PD} as given by,

$$V_{PD} = A \sin\left(\frac{2\pi}{T}(nT + \Delta t)\right)$$

$$V_{PD} = A\ \sin\left(2n\pi + 2\pi.\frac{\Delta t}{T}\right)$$

$$V_{PD} = A\ \sin(\varphi_{er})$$

So, even when we have one as a square wave and the other as a sine wave, and we use this sample and hold circuit as shown to you, you get the V_{PD} output as $A\ \sin(\varphi_{er})$. The 2 times frequency component is not there here. So, if you look at V_{PD} or $\overline{V_{PD}}$, the way I have implemented here, with respect to the phase error, $\overline{V_{PD}}$ is same as V_{PD} in this case for a fixed phase error and the waveform is sine wave here.

So, we know that this is A, this is $-A$, and this is $\frac{\pi}{2}$, this is $-\frac{\pi}{2}$, this is $-\pi$ and this is $+\pi$. Well, it will continue on either side but this is what is of interest to us. The same thing will apply here that the gain of the above phase error detector is given by,

$$K_{PD} = A\ \cos(\varphi_{er})$$

The linear (monotonous) range is $\pm\frac{\pi}{2}$. So, how is it different from the previous mixer based phase error detector? Well, in this particular case, you do not have that high frequency component to begin with, and the output which you are getting is actually held output for fixed phase error. If the frequency is fixed, your phase error will be fixed. If you have a frequency error, then it is going to be different.

Inherently, what you see here is that the sample and hold phase error detector is non-linear. It is actually not linear at all. As you see, the gain of this phase error detector also varies. I will just plot the gain of the phase error detector in the same curve. It is like this. You can plot it in a different curve which is fine. This is K_{PD}. It depends on what phase error you have.

So, when you have a PLL and it is in steady state and you have some phase error in steady state, you apply any disturbance, you should choose the gain to analyze how the loop is going to react for that particular phase error. For example, if I have the steady state phase error as this φ_{er0}, then the gain which I am going to use for the analysis of the PLL for small disturbances in the system will be this.

Now, what happens in the case your sinusoidal frequency is much larger or the output frequency is different? Can you do anything here? So, let me just take an example. So, let us say, you have a sine wave and I will show you, this is interesting here. So, I have shown you

one case where the output signal is shown here. This is V_{out} and the input signal happens to be half the frequency. So, if the input signal happens to be half the frequency, I will just plot that input signal. Half the frequency means that the input clock period of the square wave is two times the clock period of the sine wave. That is what we mean by half the frequency.

So, this is my input clock and I am using the same sample and hold circuit to detect the phase error. So, this is Δt and I have deliberately chosen my frequency in exact multiples. So, this is $2T$ and this period is T for the sine wave. Here we are sampling not at T but we are sampling at $2nT$, because we sampled always at whatever value you have at the rising edge on the sine wave, that value is held. So, if that is the case, the output of the phase error detector is given by,

$$V_{PD} = A\ \sin\left(\omega_{out}\ (2nT + \Delta t)\right)$$

$$V_{PD} = A\ \sin\left(\frac{2\pi}{T}\ (2nT + \Delta t)\right)$$

So, what you are measuring here is with respect to $2T$. You measure the phase error with respect to two times the time period. So, we get,

$$V_{PD} = A\ \sin\left(4n\pi + 2\pi.\frac{\Delta t}{T}\right)$$

$$V_{PD} = A\ \sin\left(2\pi.\frac{\Delta t}{T}\right)$$

So, the phase error which you are measuring here is with respect to the output waveform.

So, let me explain to you. The phase error is always defined with respect to a clock period. In all our previous cases, we were using the same clock period for the input and the output waveforms. In this particular example, the input and output clock periods are different. So, it completely depends on how we define.

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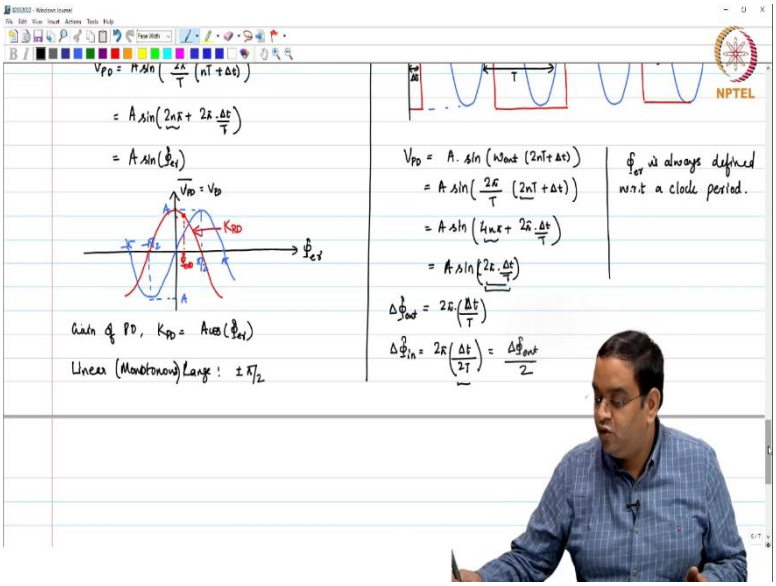

So, the phase error with respect to the output phase is given by,

$$\Delta\varphi_{out} = 2\pi.\left(\frac{\Delta t}{T}\right)$$

Also, the phase error with respect to the input phase is given by,

$$\Delta\varphi_{in} = 2\pi.\left(\frac{\Delta t}{2\,T}\right) = \frac{\Delta\varphi_{out}}{2}$$

So, what you see here is that with respect to the input phase, the phase error is half of the phase error with respect to the output phase. This is because we are treating the output frequency as two times the input frequency.

So, even when there is a frequency error between the input and the output signal and if you are using the output frequency as some n multiple of the input frequency, you can still detect the phase error, not with respect to every zero crossing of the output waveform but with respect to every rising edge of the input waveform.

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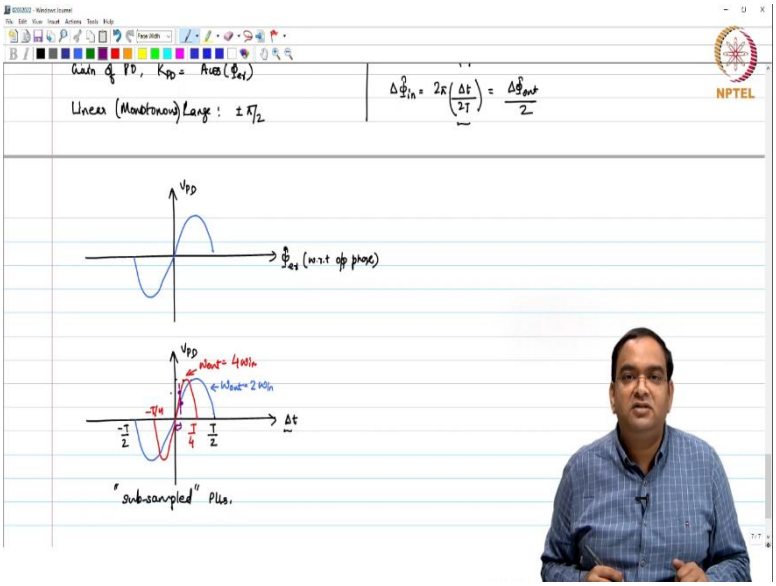

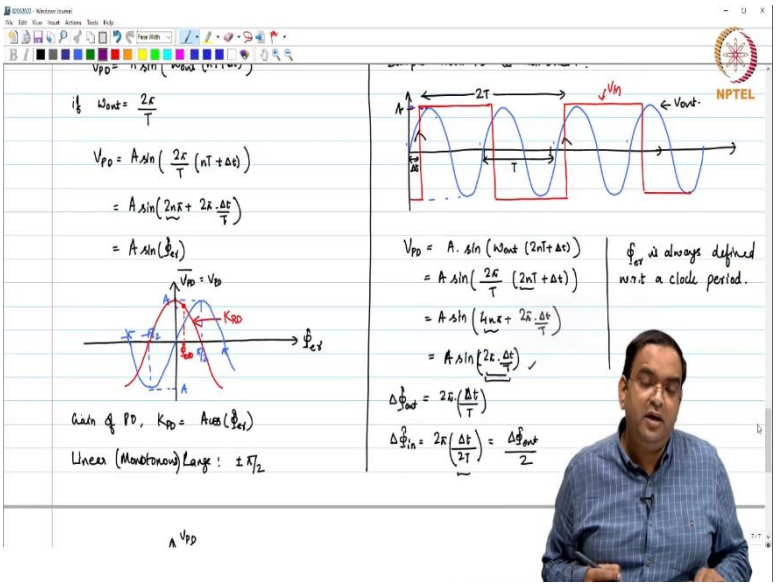

So, when we plot V_{PD} versus the phase error with respect to output phase, we see that it is sinusoidal. This is going to be like this. If you plot the same thing with respect to the timing error, I am not plotting with respect to the phase error, I plot with respect to Δt. If I plot with respect to Δt, then this value is $\frac{T}{2}$ and this value is $-\frac{T}{2}$.

You see this. What is interesting here? If, let us say, the time period is not a multiple of 2, and you have a multiple of 4. Well, then you will see the waveform like this. This will be $\frac{T}{4}$, this will be $-\frac{T}{4}$. In the previous case, you had $\omega_{out} = 2\,\omega_{in}$. In the case shown in red, you have $\omega_{out} = 4\,\omega_{in}$. This property is exploited in some kinds of PLLs which are known as sub-

sampled PLLs. Well, we will see that later but the phase error detection is based on this sample and hold itself.

So, if you look at it, in both the cases for the same phase error or the same timing error between the reference rising edge and the sinusoidal zero crossing, for the same Δt error, depending on whether the output frequency is two times or four times the input frequency, you get a different output. This is an interesting part about the sample and hold phase error detectors. Thank you.