Phase-Locked Loops
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Lecture – 16
Introduction to Clock Multipliers

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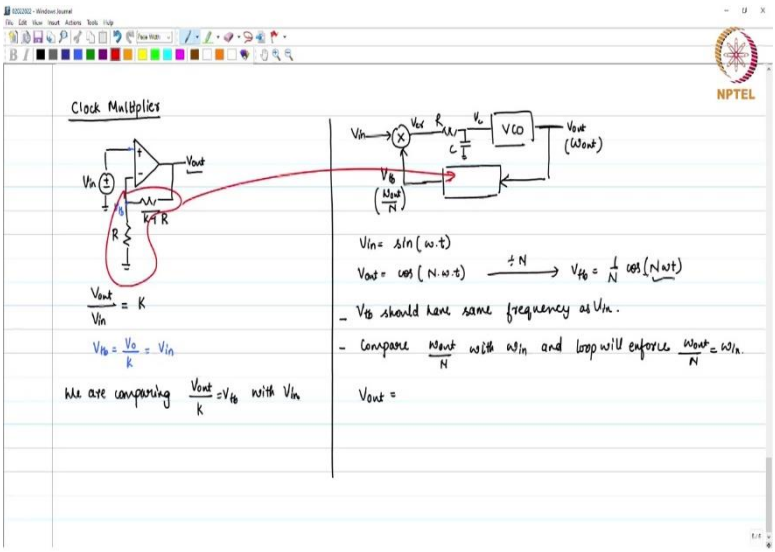

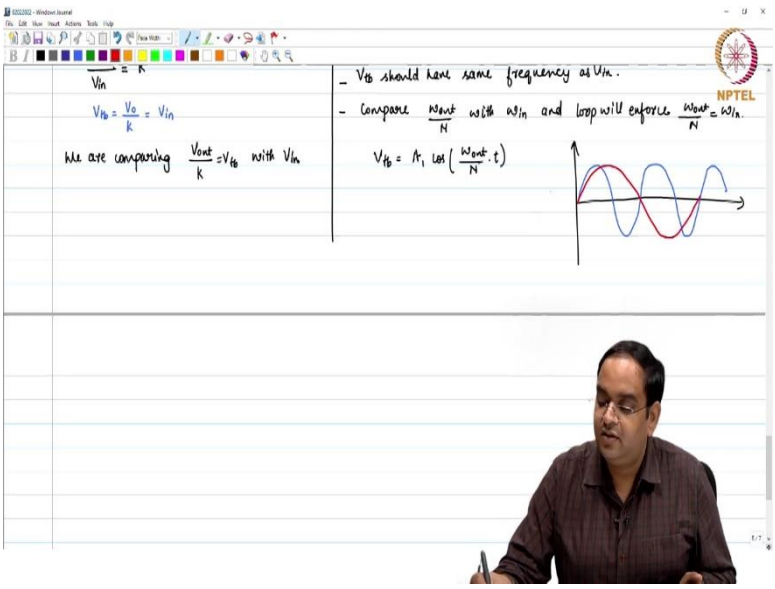

Earlier, we have seen PLLs where the output frequency happens to be the same as the input frequency. Today, we will talk about the clock multipliers where the output frequency is some N times of the input frequency. So, the output frequency does not need to be the same as the input frequency always.

So, you can think about the voltage follower as the analogy for that. So, we know voltage follower using an amplifier. I will just help you to understand a simple voltage amplifier where you apply an input voltage V_{in} and you get an output voltage V_{out}. This resistor happens to be $(k-1)R$, and this resistor is R. If the amplifier is ideal, you can work it out from this circuit and see that $\frac{V_{out}}{V_{in}} = k$. The amplifier is ideal, we know that this circuit is in negative feedback, and these two terminals are going to be the same. I call this as V_{fb}, the feedback voltage, and in this case, it is given by,

$$V_{fb} = \frac{V_{out}}{k}$$

V_{fb} and V_{in} have to be equal because it is in negative feedback, so it is a straightforward way of calculating it. So, we have,

$$V_{fb} = \frac{V_{out}}{k} = V_{in}$$

Now, what you need to conclude from here is that to make sure that $V_{out} = k\,V_{in}$, we are comparing $\frac{V_{out}}{k}$ which is V_{fb} with V_{in}.

So, you have an amplifier whose output voltage is k times the input voltage. You are not comparing the amplified output voltage with respect to the input directly. You are dividing the output voltage and comparing the divided output voltage with the input and the closed loop feedback ensuring that the feedback voltage is same as V_{in} and the feedback ratio is $\frac{1}{k}$. So, the output voltage will be $k\,V_{in}$.

The same thing happens in a clock multiplier. So, for example, let us say I do not know how I will get the whole circuit. I have this V_{in} and I have V_{fb} signal here, the output of this PLL, we have been doing it for a lot of time, so let us just continue with that very simple example. This loop filter and you have a VCO and this is V_{out}. What I want is the following:

$$V_{in} = \sin(\omega.t)$$

$$V_{out} = \cos(N.\omega.t)$$

This is what I want. I want the output frequency to be N times the input frequency.

If I connect it like this, the way we have been connecting it, we have seen that if you connect it like this, the loop is going to force the output frequency to be equal to the input frequency because that is what the loop will do. If it does not do that, then the phase error will keep on changing always, you will never reach steady state. So that is not going to happen here. If we do not want the output frequency to be equal to the input frequency, we cannot make this connection. If we cannot make this connection, then what do we need to do? We need to find a block somehow, which we do not know right now, so that the feedback signal has the frequency equal to the input frequency. The V_{fb} signal, if we want to lock this and reach steady state for this block, V_{fb} should have the same frequency as V_{in}. Well, if that is the case, it means that we have to divide the frequency.

So, what I need to do is, if I have ω_{out} here, somehow I need to get $\frac{\omega_{out}}{N}$ here. If I get $\frac{\omega_{out}}{N}$ at the feedback signal, then I will compare $\frac{\omega_{out}}{N}$ with ω_{in}, and the loop will enforce $\frac{\omega_{out}}{N} = \omega_{in}$ since this is a negative feedback loop. Keep this difference between a voltage follower and a PLL in mind. In case of a voltage follower, you were dividing the voltage.

So, if I happen to do this, I know that $V_{out} = \cos(N.\omega.t)$, I just divide the voltage using a resistive divider the way I have been doing for the voltage follower. What will I get V_{fb} as? So, we get,

$$V_{fb} = \frac{1}{N}\cos(N\ \omega\ t)$$

Does it divide the frequency? Not at all. It does not divide the frequency at all. So, you cannot use this kind of resistive network here, it is not possible.

So, how we do it, well, that you will come to know during this course, but what we need to do is that we need to somehow divide the frequency. Ideally, V_{fb}, is given by,

$$V_{fb} = A_1 \cos\left(\frac{\omega_{out}}{N}.t\right)$$

This is what we want V_{fb} to be. So, just to make sure that you follow this, if my output signal happens to be a signal like this and I want to divide the frequency by two, I want a signal like this. How we are going to do it, that is something which we will see later.

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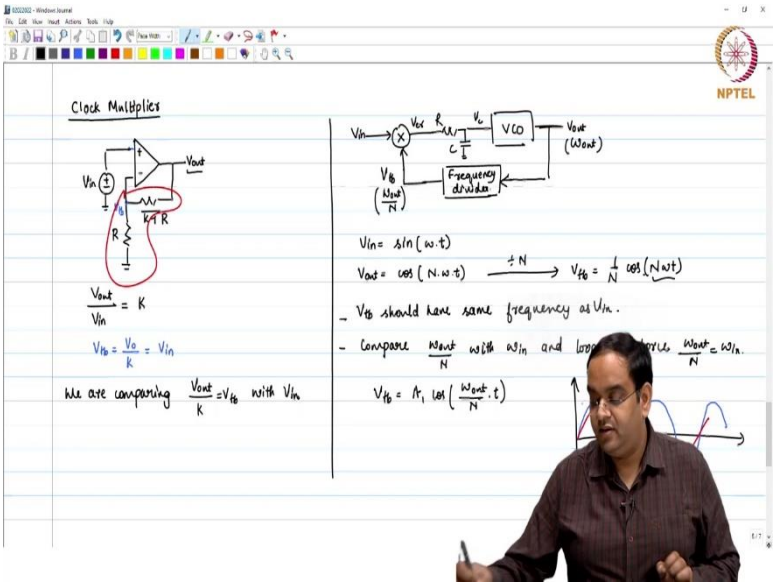

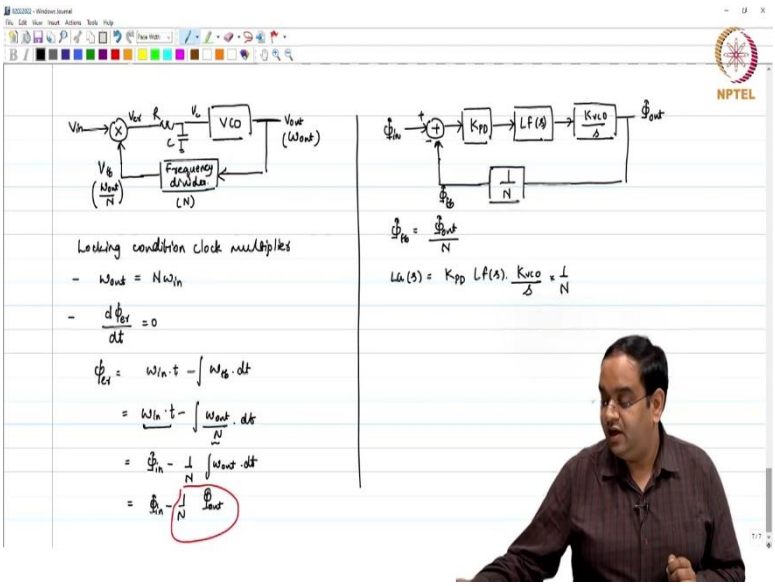

So, you need a block called frequency divider. If you do that, then you can enforce in this case. So, if I have the frequency divider here, in closed loop, the loop is going to be locked only when the following locking conditions for clock multiplier are met:

$$\omega_{out} = N\,\omega_{in}$$

where, N is the frequency division ratio. You should be able to choose different values for N. So, one condition is this, and the other condition always remains and is given by,

$$\frac{d\varphi_{er}}{dt} = 0$$

This is also a phase-locked loop by the way, do not think that this clock multiplier is different from phase-locked loop, it just has a frequency divider in the feedback path.

Now, what is the phase error? Well, the phase error at any given time is given by,

$$\varphi_{er} = \omega_{in}.t - \int \omega_{fb}.dt$$

So, this is the phase error. So, you should be able to lock the PLL with a frequency multiplication at the output. So, we have,

$$\varphi_{er} = \omega_{in}.t - \int \frac{\omega_{out}}{N}.dt$$

$$\varphi_{er} = \varphi_{in} - \frac{1}{N}\int \omega_{out}.dt$$

$$\varphi_{er} = \varphi_{in} - \frac{1}{N}\,\varphi_{out}$$

So, what is interesting here? If you are dividing the frequency by N in the feedback path as shown, then you are actually dividing the output phase by N. The feedback phase is output phase divided by N. So, a small signal model of this PLL will have the phase error detector like this with gain K_{PD}. This will be followed by the loop filter with transfer function depending on the loop filter you would like to use. This will be followed by the VCO with gain $\frac{K_{VCO}}{s}$, and $\frac{K_{VCO}}{s}$ is going to give you the output phase and because you are using a frequency divider, the feedback phase gets divided. So, this has a gain of $\frac{1}{N}$, and this is feedback phase and this is input phase. Here, the feedback phase is given by,

$$\varphi_{fb} = \frac{\varphi_{out}}{N}$$

The loop gain for this particular loop is given by,

$$LG(s) = K_{PD} \times LF(s) \times \frac{K_{VCO}}{s} \times \frac{1}{N}$$

So, the loop gain will have this transfer function. So, we will implement the clock multiplier in this course, and we will go into detail of each block from the next session onwards. Thank you.