Phase-Locked Loops

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Lecture – 14

Frequency Acquisition Ranges in Type-II PLLs with Ideal and Non-Ideal Integrator

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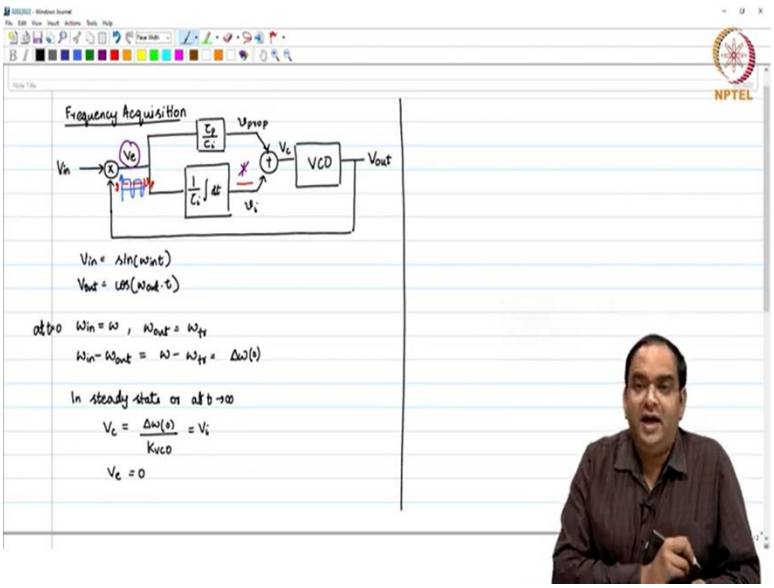

Welcome to this session everyone. In the previous session, we looked at frequency acquisition in PLLs and figured out that in Type-I PLL, we could not acquire the frequency beyond a certain range. So, we introduced an integrator in the loop. I will show you the block diagram of the PLL which we discussed in the previous session. At one place, we have a proportional gain which is $\frac{\tau_p}{\tau_i}$, and in the other path, we have an integrator which has a gain $\frac{1}{\tau_i}\int dt$, and these two things are summed up like this and it goes to the VCO.

So, the loop filter is now replaced by the proportional and integral paths. And at the end of the last session, we looked at some simulated results where we saw that having only one path, either proportional or integral, does not help. So, this is V_e, this is the control voltage, the voltage which you see at the output of the integrator is termed as V_i, and this is V_{prop}.

So, in this particular example, we have,

$$V_{in} = \sin(\omega_{in} t)$$

$$V_{out} = \cos(\omega_{out} t)$$

At $t = 0$, $\omega_{in} = \omega$, $\omega_{out} = \omega_{fr}$

The frequency error at the beginning is given by,

$$\omega_{in} - \omega_{out} = \omega - \omega_{fr} = \Delta\omega(0)$$

At time instant $t = 0$, when this frequency error is large, then the Type-I PLL was unable to acquire the frequency. What do we mean by acquiring the frequency? We mean that the control voltage develops in such a way that the output frequency is finally equal to the input frequency, and the phase error is also settled and it does not change with respect to time.

So, the things which we also discussed earlier were that initially V_e develops, it has some kind of asymmetric beat note like this, which has an effective DC voltage which I called as pull-in voltage. This voltage was pull-in voltage, V_P, and the DC part of V_P voltage was actually integrated by this integrator. At the very end, it develops a DC voltage here.

In steady state or at $t \to \infty$, we have,

$$V_c = \frac{\Delta\omega(0)}{K_{VCO}}$$

Also, when there is no frequency error in the loop and you have this integrator, the error voltage is going to be equal to zero. So, $V_e = 0$.

So, the error voltage will be zero, and the integrated output will be equal to whatever DC voltage is required for the oscillator to compensate for the frequency error. So, we have,

$$V_c = \frac{\Delta\omega(0)}{K_{VCO}} = V_i$$

This is because if you have any non-zero DC value at V_e, then this integrator will just keep on increasing. So, the oscillator will not be locked. So, this is not possible. So, this is what we figured out and we have seen the waveforms at different locations also.

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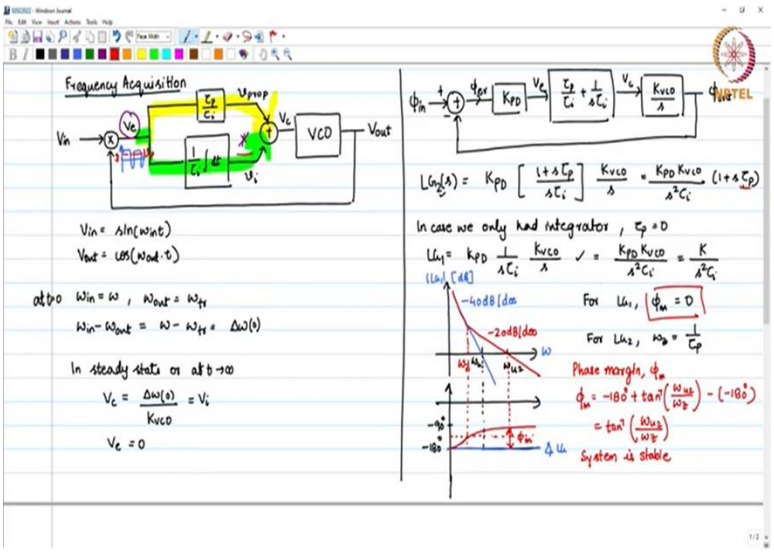

Now, one important thing here is that without the proportional path, you do not have asymmetric beat note, and without the integral path, you do not have large gain. So, both the things are required. If we happen to just analyze this PLL using its small signal model, then also you will see it is very important to have both the integral and the proportional path.

By the way, just to highlight it, what is the integral path and what is the proportional path? This path is proportional path and this particular path is integral path. So, to have no confusion here, the yellow one is the proportional path, and the other one is the integral path. Now, I am drawing the small signal model of the PLL. You have the phase error detector with gain K_{PD}. This is the input phase, you have the output phase and this particular block diagram actually can be used as such, but I will just write the transfer function here. This transfer function is $\frac{\tau_p}{\tau_i} + \frac{1}{s\,\tau_i}$, and it goes to the VCO which has a gain $\frac{K_{VCO}}{s}$. So, this is the small signal model of the PLL. So, in this small signal model of the PLL, this is phase error, this is voltage error, and this is control voltage.

The loop gain of this small signal model of the PLL is given by,

$$LG(s) = K_{PD}\left[\frac{1+s\tau_p}{s\tau_i}\right]\frac{K_{VCO}}{s} = \frac{K_{PD}\,K_{VCO}}{s^2\tau_i}\left(1+s\tau_p\right)$$

So, to understand the need of the proportional path in this particular PLL, we can see that from the loop gain analysis also, in case we only had integrator, which in turn means $\tau_p = 0$, the loop gain will be given by,

$$LG_1(s) = K_{PD}\frac{1}{s\tau_i}\frac{K_{VCO}}{s} = \frac{K_{PD}\,K_{VCO}}{s^2\tau_i} = \frac{K}{s^2\tau_i}$$

For this particular loop gain, let me call this as LG_1 and this one is LG_2. So, we have,

$$LG_2(s) = K_{PD}\left[\frac{1+s\tau_p}{s\tau_i}\right]\frac{K_{VCO}}{s} = \frac{K_{PD}\,K_{VCO}}{s^2\tau_i}\left(1+s\tau_p\right)$$

For LG_1, you will find that this particular loop is unstable. Why is it unstable? You can plot the magnitude of the loop gain. So, I will plot the magnitude of the loop gain. You are having $\frac{K_{PD}\,K_{VCO}}{s^2\tau_i}$. So, I will write this as $\frac{K}{s^2\tau_i}$. So, LG_1 is having a fall of -40 dB/dec. This is ω, this is $|LG_1|$ in dB. If you look at the corresponding phase for the same loop gain, what you have is it is always -180°. So, I will just start here, let us say this is -90°, and this is -180°. So, this is the $\angle LG_1$. Let me just put this in blue.

So, what do you see here as the phase margin? For LG_1, the phase margin is actually zero. So, we have,

$$\text{For } LG_1,\ \varphi_m = 0$$

How do we look at the phase margin? We look at the phase margin at the unity gain frequency. How far is the phase from 180° at the unity gain frequency, that is how we measure the phase margin. The phase is always 180°, hence, the phase margin is zero. In the other case, for LG_2, you see that this is $\frac{K_{PD}\,K_{VCO}}{s^2\tau_i}\left(1+s\tau_p\right)$. So, you have a zero at $\frac{1}{\tau_p}$. So, in case we place $\frac{1}{\tau_p}$ lesser than the unity gain frequency, LG_2 will be something like this. It will start with -40 dB/dec and after the zero frequency, it will be -20 dB/dec. So, this is ω_z for LG_2. So, we have,

$$\omega_z = \frac{1}{\tau_p}$$

The unity gain frequency will also change.

The phase for the corresponding loop gain will start with -180°, it will go to -135° because a zero will give you 45° heads up, and then finally in the end, it will reach to -90° asymptotically. So, the phase margin for the new loop gain or LG_2 is given by,

$$\varphi_m = -180° + \tan^{-1}\left(\frac{\omega_{u2}}{\omega_z}\right) - (-180°)$$

$$\varphi_m = \tan^{-1}\left(\frac{\omega_{u2}}{\omega_z}\right)$$

So, you have a positive phase margin, thus, your system is stable. This system is stable whereas LG_1 was not stable. Why was it not stable? Well, the phase margin is zero. So, from your basic system level analysis, you would know that in order a closed loop system is stable, you need to have a positive phase margin.

So, coming back to this small signal analysis and how we related it to the large signal frequency acquisition. We will make two statements here. First, to acquire the frequency when you have a large frequency error in the beginning, you need both proportional and integral paths, you cannot do with only proportional path or only integral path. Second, from the stability point of view, the small signal analysis tells us that you cannot have a stable system with two integrators, you need to have a proportional path for sure.

So, both these analyses are telling you that you need both proportional and integral paths for frequency acquisition and from stability point of view. Now, once we know that the system is stable and the PLL can acquire any frequency, the question arises that how much can be the frequency error which means how large can $\Delta\omega(0)$ be in the first place?

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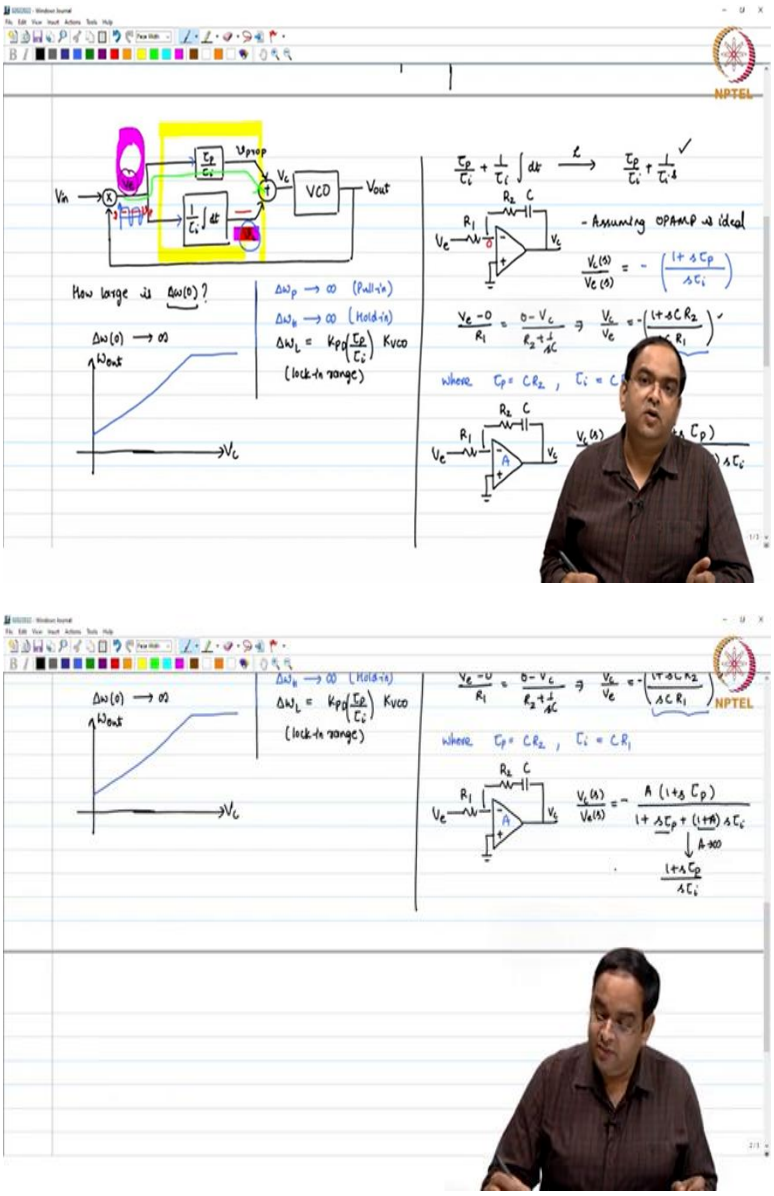

So, the question which we are asking is that how large is $\Delta\omega(0)$? For answering this question, you can do rigorous mathematical analysis but before doing the mathematical analysis, we will just try to see what is limiting here. The way this particular PLL works is that it can generate any voltage V_i because it is just like an integrator, even if you give a very small input to an integrator, over a given period of time, it is going to generate whatever voltage you need. You give more time to an integrator, it will integrate a larger value. So, it can generate any voltage. And in steady state, this loop filter can have any voltage which you want at your output without having a non-zero input voltage. So, having a zero here and a non-zero V_i, whatever value you need, that is practical, you

can always get it. If that is the case, then it does not matter what is the initial frequency error. At the end, if this loop is in closed loop, it is going to acquire any frequency which you need.

So, there is no limit on $\Delta\omega(0)$. Actually, $\Delta\omega(0) \to \infty$, and the pull-in range $\Delta\omega_P \to \infty$, there is no limit. In practice, what you will see here is that there is a limit on the VCO, so what do we mean by that? So, in case if you are looking at the VCO characteristics, you may find that ω_{out} frequency versus the control voltage has an upper limit. We do not know how much. You cannot just keep on increasing the frequency of the oscillator as you want. It may saturate at some point. At the end of the day, you will design these oscillators and all these blocks in a given technology, you know that you cannot increase the voltage beyond a certain value in a given CMOS or BiCMOS technology. So, your frequency is always going to be limited by that, at least. So, this loop itself does not put any restriction on the output frequency. Mostly the output frequency restrictions are added by the VCO or the loop filter or any other block.

So, the pull-in range and the hold-in range are given by,

$$\Delta\omega_P \to \infty$$

$$\Delta\omega_H \to \infty$$

The other one was the lock-in range. So, for this particular PLL, we have seen that the lock-in range requires the phase error to be limited within two 2π and acquire the lock. So, for lock-in range, what you need to do is that you need to find out the frequency range to which the PLL locks without the phase error exceeding 2π. And we have seen that the PLL locks without the phase error exceeding 2π, it can do that only through the proportional path. If the integral path does not require to develop any voltage, the proportional path acquires the lock which we have seen earlier, then you will not exceed the phase error of 2π. So, that limit will come from the proportional path and the lock-in range is given by,

$$\Delta\omega_L = K_{PD}\left(\frac{\tau_p}{\tau_i}\right)K_{VCO}$$

This is the lock-in range. Does it matter that the PLL has a lesser lock-in range and greater pull-in range? Well, if you are only looking for the frequency acquisition, it does not matter whether it is

doing a cycle slipping or not. If you are looking for some other characteristics during the settling of the PLL where some other block depends on this PLL frequency acquisition, then it may matter whether you are doing cycle slipping during frequency acquisition or not. Otherwise, when you run the PLL, if it acquires the lock, that is good enough. So now, if it is so simple, then well, the PLL is done, but that is not the case.

So, what happens is, when you go ahead and you try to implement this loop filter $\frac{\tau_p}{\tau_i} + \frac{1}{\tau_i}\int dt$, this is the transfer function in time domain. In Laplace domain, it translates to $\frac{\tau_p}{\tau_i} + \frac{1}{\tau_i s}$. So, we have,

$$\frac{\tau_p}{\tau_i} + \frac{1}{\tau_i}\int dt \xrightarrow{L} \frac{\tau_p}{\tau_i} + \frac{1}{\tau_i s}$$

This transfer function can be easily implemented by using an active integrator as shown to you like this, where I have this R and C providing me the integration here, this is you can say is V_e, and this is V_c. This particular resistance happens to be R_1, this is R_2 and this is C. So, assuming the amplifier is ideal, assuming that the OPAMP is ideal, and this OPAMP with integrator is used in the PLL loop, there will be overall negative feedback for this loop filter and I can assume that this node will also be incrementally grounded.

So, you will have,

$$\frac{V_e - 0}{R_1} = \frac{0 - V_c}{R_2 + \frac{1}{sC}}$$

$$\frac{V_c}{V_e} = -\left(\frac{1 + sCR_2}{sCR_1}\right)$$

Well, now you can say that previously this loop filter did not have any negative sign but now I have a negative sign. If you have a negative sign, do not worry about it. You can adjust this negative sign in the way by which you are going to connect to the VCO. So, what is important right now is only this part. So, we have,

$$\frac{V_c(s)}{V_e(s)} = -\left(\frac{1 + s\tau_p}{s\tau_i}\right)$$

where, $\tau_p = CR_2$, $\tau_i = CR_1$.

So, given this loop filter, you can very well implement it and everything seems to work.

The problem arises because this loop filter which you are seeing here does not find an ideal amplifier. The amplifier happens to be non-ideal. So, we will introduce only one order of non-linearity here that this has a gain A. So, this is a very simple non-linearity that the gain is fixed across the frequencies and the gain is equal to A. If you have this, then, we have,

$$\frac{V_c(s)}{V_e(s)} = -\frac{A\left(1 + s\tau_p\right)}{1 + s\tau_p + (1 + A)s\tau_i}$$

If you want to do a sanity check, what you can do is that you apply $A \to \infty$, then in that case what you will see here is that it should translate back to the previous one. So, we get,

$$\text{If } A \to \infty, \frac{V_c(s)}{V_e(s)} = \frac{1+s\tau_p}{s\tau_i}$$

So, it does translate to the previous transfer function.

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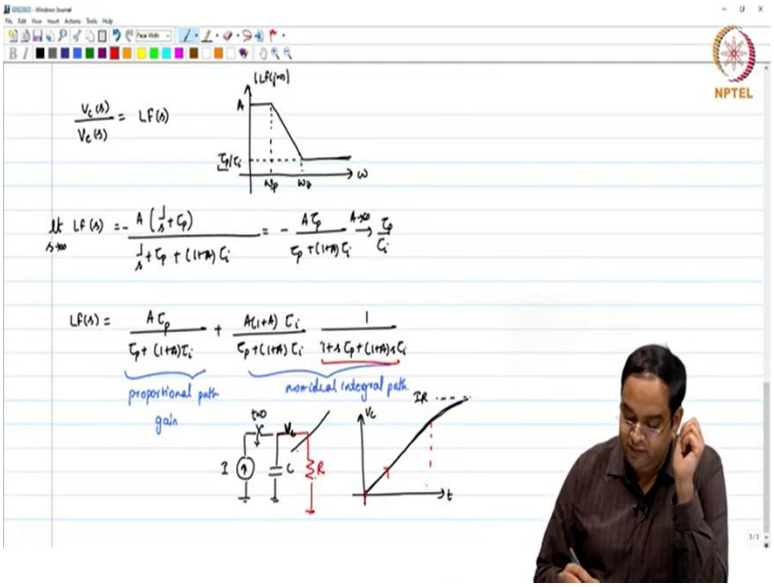

Now, in the presence of this new transfer function which you see, $\frac{V_c(s)}{V_e(s)}$ which has some DC gain, I am just writing this loop filter transfer function as,

$$\frac{V_c(s)}{V_e(s)} = LF(s)$$

It is not so simple to define the pull-in range and the hold-in range. Well, if I want to draw this loop filter, I can very well draw this loop filter here, $|LF(jw)|$, the DC gain of this loop filter happens to be A. So, the pole for this loop filter transfer function happens to be at $\frac{1}{\tau_p+(1+A)\tau_i}$. So, you will have a pole here and then you have a zero and the zero happens to be at $\frac{1}{\tau_p}$, which is going to be much farther away, and after the zero, it will be flat. So, you will have at zero, after the zero location, you will see a flat response, this is ω_p. And what is this value? You can find this value as $s \to \infty$. You can substitute $s \to \infty$ in the loop filter transfer function. So, we get,

$$\lim_{s\to\infty} LF(s) = -\frac{A\left(\frac{1}{s}+\tau_p\right)}{\frac{1}{s}+\tau_p+(1+A)\tau_i} = -\frac{A\tau_p}{\tau_p+(1+A)\tau_i}$$

Under the fact that $A \to \infty$, this is given by,

$$\lim_{A\to\infty} -\frac{A\tau_p}{\tau_p+(1+A)\tau_i} = -\frac{\tau_p}{\tau_i}$$

So, this is what I have here approximately if A is assumed to be very large, because for amplifier, A is in general pretty large. So, what you see here is that you do not have an ideal integration path, you have an integration path, but it happens to be non-ideal and then you have a proportional path with a constant gain like this.

So, the transfer function of the loop filter can be written as given below.

$$LF(s) = \underbrace{\frac{A\,\tau_p}{\tau_p+(1+A)\tau_i}}_{\text{proportional path}} + \underbrace{\frac{A(1+A)\tau_i}{\tau_p+(1+A)\tau_i}\,\frac{1}{1+s\tau_p+(1+A)s\tau_i}}_{\text{non-ideal integral path}}$$

See, doing all this math is just to help you understand that when you have a non-ideal OPAMP, because of the gain of the non-ideal OPAMP, your actual loop filter gain changes, and then effectively, I can say that this is a proportional path gain and this is for a non-ideal integral path.

As $A \to \infty$, the gain of the integral path actually goes to infinity, but here the problem is A does not go to infinity.

So, you have some kind of non-ideal integration, and what is actually non-ideal integration? To understand that, you can think, if I have a current source and I pass it through a capacitor, I have this current source I, I pass it through the capacitor, the voltage V_c keeps on increasing. If I add a resistor in parallel, let this resistor be very large, if I apply this current source using a switch at time $t = 0$, you will see that depending on the resistor which you are having in parallel, this will keep on increasing. At the end, well, it will approach some value which is IR. As R is large, the largest value which can be achieved as $t \to \infty$ is pretty large. Over a period of time, it behaves like an integrator only. So, this is a non-ideal integrator which is mimicked by having such kind of transfer function. Well, you can also see that from here, $\frac{V_c}{I}$, in this case, is nothing but R in parallel with C, which is $\frac{R}{1+sRC}$ which is similar to what you are having here. So, there is no difference.

So now, given this non-ideal integrator, what are the pull-in and hold-in ranges? That is a very extensive mathematical exercise which I will avoid here. If you want, you can always refer to the books. What I can tell you here is the pull-in range having a loop filter which does not have an infinite DC gain.

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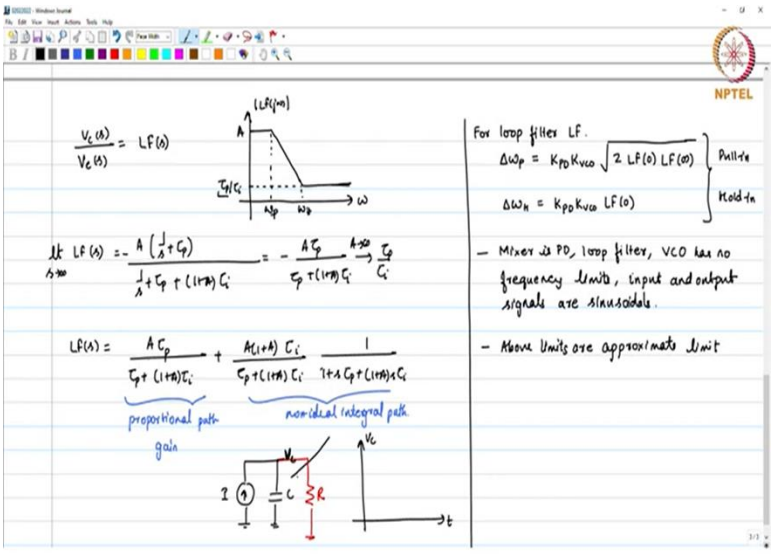

For loop filters with non-ideal amplifiers or with DC gain which is not infinity, we have to understand that how this pull-in range is defined. This pull-in range, under many approximations, is given by,

$$\Delta\omega_P = K_{PD}K_{VCO}\sqrt{2\ LF(0)LF(\infty)}$$

The hold-in range is given by,

$$\Delta\omega_H = K_{PD}K_{VCO}LF(0)$$

If $LF(0)$ is infinity, then you see that both the pull-in and hold-in ranges are actually infinite. I have not gone into the mathematical analysis of this because it is quite intensive and it will be a sheer Maths exercise. So, we can ignore that right now. But you see that you have the pull-in and hold-in ranges depending on the loop filter transfer function values at 0 and infinity.

So now, one of the loop filters which we have seen is an active loop filter, you can have a passive loop filter also. We will see in due course of time that which kind of loop filter is used in general, depending on the application. So, your application is quite important to decide what kind of loop filter you want.

So, the pull-in, hold-in and lock-in ranges depend on our analysis where we make some assumptions to simplify our analysis. Also, these limits are specific to the PLL which we are considering where mixer is phase detector, loop filter implements the specific transfer function which we have, and VCO has no frequency limits.

So, please do not use the same expressions for a different kind of PLL. It completely depends on where we are looking at or what is the exact PLL. Also, our input and output signals are sinusoidal. This is important to understand because later you are going to see that the input and output signals are square waves for some of the PLLs, and if you apply the same thing for them, it is incorrect. The other thing here is that if you think that whatever value we have here for this particular $\Delta\omega_P$, this particular value is the limit and the moment you cross this, the PLL cannot pull-in, well, these limits are approximate limits. So, whenever you simulate the PLL and you find that the PLL is not pulling-in even for the frequency errors lesser than $\Delta\omega_P$, well, that is fine, do not worry about it. This is just an extreme limit based on many assumptions. So, please keep that in mind. Thank you.